Final Call for Papers
ASP-DAC 2000

Asia and South Pacific Design Automation Conference 2000 with EDA TechnoFair 2000

January 25–28, 2000
Pacifico Yokohama, Yokohama, JAPAN

Aims of the Conference:
The goal of the meeting of ASP-DAC 2000 is to provide a forum for presentation, discussion, and observation of the state-of-the-art of Design Automation (DA) and LSI Design of electronic systems. The format of the meeting intends to cultivate and promote an instructive and productive interchange among not only DA researchers and developers but also system and circuit designers. A variety of those scientists, engineers, and students who are interested in theoretical issues on DA are also welcome.

Background:
ASP-DAC 2000 is the fifth in a series of annual international conferences on Design Automation. Asia and South Pacific Region is one of the hottest silicon areas in the world, in the sense that the amount of VLSI production is rapidly growing. Thus the conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of basing leading edge research not only on specific design concepts but also on new aspects of approaches to integrated design concepts.

Areas of Interest:
Original papers on, but not limited to, the following areas are invited.

[I] LSI Development: System LSI, Application specific memory and memory blocks, Microprocessor, Multimedia DSP, Analog/mixed signal LSI, Low power/low voltage LSI, Wireless/wired communications LSI, Field-programmable/reconfigurable LSI, Neuro LSI.

[II] Design and Environment: High performance/low power/deep submicron design, Rapid prototyping system and emulation, Asynchronous design, Application specific design flows, Language issues, Chart-based design, Design reuse, VSI and IP issues, Library, Database, Design management, Tool integration, Human factors in DA, Design experience using DA tools, Reconfigurable system.

[III] System DA: Theory for system/behavioral synthesis, System synthesis, HW/SW codesign, Behavioral synthesis, Architecture/system level estimation, Synthesis for low power/testability/fault tolerance, System definition language.

[IV] Logic DA: Logic function and switching theory, Combinational/sequential/asynchronous synthesis, Mapping and technology dependent optimization, Analysis and estimation, Theory for testing, Fault modeling, Test pattern generation, Design for testability, Fault tolerance, Formal verification and simulation.

[V] Physical DA and TCAD: Partitioning, Floorplanning, Placement and routing, Clock and power/ground distribution, Module generation, Layout verification, PCB and MCM design, Interaction between logic and layout design, Deep submicron DA, Analog circuit analysis, Mixed signal synthesis/simulation, Device modeling/optimization/simulation, Interconnect modeling/simulation, CAD tools for new devices, EMI (Electromagnetic Interference) modeling and simulation, Process simulation.

Submission of Papers:

Deadline for submission:	**July**	**9, 1999**
Notification of acceptance:	**October**	**8, 1999**
Deadline for final version:	**November**	**12, 1999**

Prospective authors are invited to submit to the Conference Secretariat **8 copies of a complete paper in camera-ready format** in English, with a cover page specifying:

[i] title of paper,
[ii] authors and affiliation,
[iii] speaker,
[iv] mailing address, phone No., FAX No., and e-mail address of the contact author,
[v] brief abstract describing the work,
[vi] list of area numbers (e.g. III), ordered by relevancy, most clearly matching the content of the paper.

Specification of the camera-ready format is available at our WEB site `http://www.jesa.or.jp/ASPDAC/`.

The paper should be **between 3 to 6 pages in length including all figures, tables and references**. The technical expositions should be directed to a specialist and should include an introduction for a nonspecialist that describes the problem and the achieved results, focusing on the important ideas and their significance. Any paper that deviates significantly from these guidances, or is not received by the deadline, risks rejection without consideration of its merits.

All accepted papers are requested to be presented at the conference.

Panels, Special Sessions and Tutorials:
Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat no later than **June 1, 1999.**

The deadline is extended to July 9, 1999.
(added June 14, 1999)

Exhibition:
An exhibition, EDA TechnoFair 2000, sponsored by Electronic Industries Association of Japan, will be opened free of charge to all attendees. Over 50 exhibitors are expected to participate with specializing CAD/DA/CAE systems, hardware platform related products, publications and services.

Tutorials:
Chargeable tutorial sessions will be provided in conjunction with the conference. There will be full-day or half-day sessions to introduce state-of-the-art and future technologies that will focus on fabrication and process, system and circuit design, EDA, and new applications.

Award:
Best paper awards will be given to a few excellent technical papers.

Travel Grant:
Limited travel assistance will be provided for worthy conference participants. Priority will be given to technical paper presenters, design contest participants, and panelists who belong to academic institutions.

Call for Designs

ASP-DAC 2000 University LSI Design Contest

Aims of the Contest:
As a unique feature of ASP-DAC 2000, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on LSI design and implementation at universities, and other educational organizations.

Original LSI circuit designs that meet all the following conditions are highly solicited for submission:
(1) Designed, and actually implemented on chips,
(2) at universities, or other educational organizations, and
(3) during the last two years.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Awards will be given to a few number of outstanding designs, selected from those presented at the conference.

Areas of Design:
Application areas, or types of circuits, include (but are not limited to):
(1) Analog and Mixed-Signal Circuits,
(2) Digital Signal Processing,
(3) Microprocessors,
(4) Custom Application Specific Circuits.

Methods, or technology, used for implementation include:
(a) Full Custom and Cell-Based LSIs,
(b) Gate Arrays,
(c) Field Programmable Devices, including FPGA/PLDs.

Submission of Design Descriptions:
It is requested to send to the Conference Secretariat, **10 copies of the summary in camera-ready format** in English, that satisfy the following conditions:
(1) The cover page should include (i) indication that it is an application for University LSI Design Contest, (ii) title of the design, (iii) authors and affiliations, (iv) speaker, (v) mailing address, phone No., FAX No., and e-mail address of the contact author, (vi) area of the application and implementation method, expressed using the codes shown in the above Areas of Design (e.g. "3-a" for a full custom microprocessor), (vii) clear and brief description on the application, originality, and other features of the design, (viii) contribution of each author, if the LSI is jointly developed with non-academic parties.
(2) The summary is requested to be written within **2 pages, including figures, tables, and references.** *Specification of the camera-ready format is available at our WEB site* `http://www.jesa.or.jp/ASPDAC/`.
(3) It is strongly recommended that measured experimental results and a chip micrograph should be included. If the experimental results and the chip micrograph have not been prepared before the deadline of submission, the authors can send the revised paper including them later.

Deadline for summary:	**July 24, 1999**
Deadline for experimental results and chip micrograph:	**September 4, 1999**
Notification of acceptance:	**October 31, 1999**
Deadline for camera-ready:	**November 12, 1999**

Review:
Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs: (1) Reliability of design and implementation, (2) Quality of implementation, (3) Performance of the design, (4) Novelty of application, algorithm, architecture, (5) Others.

Interesting or excellent designs selected will be presented at a special session of the conference. Also, the following awards will be given to a few number of outstanding designs, selected from those presented at the conference:
(1) Outstanding design award, and
(2) Special feature awards.

Presentation:
An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2000. A digest of each design to be presented will be included in the conference proceedings.

ASP-DAC 2000 Organizing Committee:

General Chair:	Kenji Yoshida (Toshiba)
Steering Comm. Chair:	Tatsuo Ohtsuki (Waseda Univ.)
Technical Program Co-Chairs:	Hiroaki Kunieda (Tokyo Inst. of Tech.)
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Design Contest Co-Chairs:	Ryota Kasai (NTT)
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Hon-Wai Leong (National Univ. of Singapore)
Youn-Long Lin (Tsing Hua Univ., Hsin-Chu)
Sunil D. Sherlekar (Silicon Automation Systems)
David Skellern (Macquarie Univ.)
Qianling Zhang (Fudan Univ.)

Conference Secretariat:
For submission of papers, application for design contest, proposals and inquiries, contact the Conference Secretariat:

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