Wednesday, January 31, 9:30 – 12:15

Wednesday, January 31
Time : 9:30 - 10:30 Room : 303/304
Keynote Address I :

Role of the Semiconductor Industry in the 21st Century = Human Talent Is the Heart of the Information Society =

H. Sasaki - Chairman, NEC Corporation, Japan

Wednesday, January 31
Time : 10:45 - 12:15 Room: 303/304
Executive Panel Discussion: Secrets to Success in a Start-Up EDA Business

Organizer : *T. Kozawa* - STARC, Japan
Moderator : *J. Goodsel* - Simplex Solutions and CoWare
Panelists : *S. S. Wang* - NAssda Corp.
B. Rosenthal - Tensilica
D. Fairbairn - Simutech Corp.
M. Tsai - Axis
H. Hasegawa - HD Lab.

Wednesday, January 31, 13:30 – 15:30

Wednesday, January 31
Time : 13:30 - 15:30 Room : 301
Session A1 : (Special Session) University LSI Design Contest

Co-Chairs : *H. Onodera* - Kyoto Univ., Japan
S. K. Nandy - Indian Institute of Science, India
T. Kuroda - Keio Univ., Japan

Short Presentations and Poster Discussions

A1.1 A Vector-Pipeline DSP for Low-Rate Videophones

K. Kobayashi, M. Eguchi, T. Iwahashi, T. Shibayama, X. Li, K. Takai, H. Onodera - Kyoto Univ., Japan

A1.2 A High-Speed PLA Using Array Logic Circuits with Latch Sense Amplifiers and a Charge Sharing Scheme

H. Yamaoka, M. Ikeda, K. Asada - Univ. of Tokyo, Japan

A1.3 Multi-Hit Time-to-Digital Converter VLSI for High-Energy Physics Experiments

Y. Arai - National High Energy Accelerator Research Organization, Japan

A1.4 High-Speed FIR Digital Filter with CSD Coefficients Implemented on FPGA

M. Yamada, A. Nishihara- Tokyo Institute of Technology, Japan

A1.5 Single Chip 3D Rendering Engine Integrating Embedded DRAM Frame Buffer and Hierarchical Octet Tree (HOT) Array Processor with Bandwidth Amplification

Y. -H. Park, S.-H. Han, H.-J. Yoo - Korea Advanced Institute of Science and Technology, Korea

A1.6 A Dynamically Reconfigurable Hardware-based Cipher Chip

Y. Mitsuyama, Z. Andales - Osaka Univ., Japan
T. Onoye - Kyoto Univ., Japan
I. Shirakawa - Osaka Univ., Japan

A1.7 Test Circuits for Substrate Noise Evaluation in CMOS Digital ICs

M. Nagata, T. Ohmoto, J. Nagai, T. Morie, A. Iwata - Hiroshima Univ., Japan

A1.8 Realtime Wavelet Video Coder Based on Reduced Memory Accessing

R. Y. Omaki, Y. Dong, M. H. Miki, M. Furuie, D. Taki, M. Tarui, G. Fujita - Osaka Univ., Japan
T. Onoye - Kyoto Univ., Japan
I. Shirakawa - Osaka Univ., Japan

A1.9 A Prototype Chip of Multicontext FPGA with DRAM for Virtual Hardware

D. Kawakami, Y. Shibata, H. Amano - Keio Univ., Japan

A1.10 A Single-Inductor Dual-Output Integrated DC/DC Boost Converter for Variable Voltage Scheduling

D. Ma, W. -H. Ki, C.-Y. Tsui, P. K. T. Mok - The Hong Kong Univ. of Science and Technology, Hong Kong

A1.11 A Smart Position Sensor for 3-D Measurement

T. Nezuka, M. Hoshino, M. Ikeda, K. Asada - Univ. of Tokyo, Japan

A1.12 Parameterized MAC Unit Implementation

M.-C. Chen, I. -J. Huang - National Sun Yat-Sen Univ., Taiwan
C. -H. Chen - National Cheng Kung Univ., Taiwan

A1.13 A Parallel Vector Quantization Processor Featuring an Efficient Search Algorithm for Real-time Motion Picture Compression

T. Nozawa, M. Imai, M. Fujibayashi, *T. Ohmi* - Tohoku Univ., Japan

A1.14 An 8-b nRERL Microprocessor for Ultra-Low-Energy Applications

S. Kim, J.-H. Kwon, S.-I. Chae - SNU, Korea

A1.15 Design and Implementation of JPEG Encoder IP Core

C.-J. Lian, L.-G. Chen, H.-C. Chang, Y.-C. Chang - National Taiwan Univ., Taiwan

A1.16 A Real-Time 64-Monosyllable Recognition LSI with Learning Mechanism

K. Nakamura - Nara Institute of Science and Technology, Japan
Q. Zhu - Fujitsu Labs Ltd., Japan
S. Maruoka - Hitachi Ltd., Japan
T. Horiyama, S. Kimura, K. Watanabe - Nara Institute of Science and Technology, Japan

A1.17 Reusable Embedded In-Circuit Emulator

I.-J. Huang, H. M. Chen, C.-F. Kao - National Sun Yat-Sen Univ., Taiwan

A1.18 Flexible Processor Based on Full-Adder / D-Flip-Flop Merged Module

S. Sakaidani, N. Miyamoto, T. Ohmi - Tohoku Univ., Japan

A1.19 Development of Referential PPRAM-Link Interface (PLIF) IP Core for High-Speed Inter-SOC Communication

T. Okuma, K. Hashimoto, K. Murakami - Kyushu Univ., Japan

Wednesday, January 31
Time : 13:30 - 15:30 Room : 302
Session B1 : Device/Circuit Co-designing for Advanced Technologies

Co-Chairs : ***S. Nassif –*** IBM Austin Research Lab. USA
M. Miyama - Hitachi Corp, Japan

B1.1 Correlation Method of Circuit-Performance and Technology Fluctuations for Improved Design Reliability

D. Miyawaki, S. Matsumoto, S. Ooshiro, M. Miura-Mattausch, H. J. Mattausch - Hiroshima Univ., Japan
S. Kumashiro, T. Yamaguchi, K. Yamashita, N. Nakayama - Nakayama Semiconductor Technology Academic Research Center, Japan

B1.2 Realization of Semiconductor Device Synthesis with the Parallel Genetic Algorithm

Z. Li, X. Xie, W. Zhang, Z. Yang - Institute of Microelectronics, Tsing Hua Univ., China

B1.3 (Invited Talk) : Precise Extraction of Ultra Deep Submicron Interconnect Parasitics with Parametrizable 3D - Modeling

M. Frerichs - Infineon Technologies, Germany

Wednesday, January 31
Time : 13:30 - 15:30 Room : 311/312
Session C1 : System Level Specification and Simulation

Co-Chairs : *S. Vernalde* - IMEC, Belgium
T. Ishii - Toshiba Corp, Japan

C1.1 Compiling SpecC for Simulation

J. Zhu - Univ. of Toronto, Canada
D. D. Gajski - Univ. of California Irvine, USA

C1.2 Scalable and Flexible Cosimulation of SoC Designs with Heterogeneous Multi-Processor Target Architectures

P. Gerin, S. Yoo, G. Nicolescu, A. A. Jerraya - TIMA Laboratory, France

C1.3 A Higher Level System Communication Model for Object-Oriented Specification and Design of Embedded Systems

K. Svarstad, N. Ben-Fredj, G. Nicolescu, A. A. Jerraya - TIMA Laboratory, France

C1.4 Dataflow Specification for System Level Synthesis of 3D Graphics Applications

C. Park, S. Kim, S. Ha - Seoul National Univ., Korea

Wednesday, January 31
Time : 13:30 - 15:30 Room : 313/314
Session D1 : Issues in BDD and Sequential Verification

Co-Chair : *S. Minato* - NTT, Japan

D1.1 The Multiple Variable Order Problem for Binary Decision Diagrams: Theory and Practical Application

C. Scholl, B. Becker, A. Brogle - Albert-Ludwigs-Univ., Germany

D1.2 Application of Linearly Transformed BDDs in Sequential Verification

A. Hett, W. Gnther, B. Becker - Univ. of Freiburg, Germany

D1.3 A New Partitioning Scheme for Improvement of Image Computation

C. Meinel , C. Stangier - Univ. of Trier, Germany

D1.4 An Efficient Design-for-Verification Technique for HDLs

C.-N. J. Liu, I-L. Chen, J.-Y. Jou - National Chiao Tung Univ., Taiwan

Wednesday, January 31, 16:00 – 18:00

Wednesday, January 31
Time : 16:00 - 18:00 Room : 301
Session A2 : Interconnect Design Optimization (I)

Co-Chair : *T. Okamoto* - NEC Corp, Japan

A2.1 Reducing Bus Delay in Submicron Technology Using Coding

P. P. Sotiradis, A.Chandrakasan - MIT, USA

A2.2 Optimal Spacing and Capacitance Padding for General Clock Structures

C. C. Chen, H. Y. Lai - Univ. of Wisconsin at Madison, USA

A2.3 Provably Good Global Buffering by Multiterminal Multicommodity Flow Approximation

F. Dragan, A. B. Kahng - UCLA, USA
S. Muddu - Silicon Graphics Instrument, USA
A. Zelikovsky - Georgia State Univ., USA

A2.4 Construction of Minimal Delay Steiner Tree Using Two-Pole Delay Model

L. Lin, T. T. Hwang – Tsing Hua Univ., China

Wednesday, January 31
Time : 16:00 - 18:00 Room : 302
Session B2 : Design for Manufacturability

Co-Chairs : *M. Frerichs* – Infineon Technologies, Germany
M. Miura-Mattausch – Hiroshima Univ., Japan

B2.1 New Graph Bipartizations for Double-Exposure, Bright Field Alternating Phase-Shift Mask Layout

S. Vaya - UCLA, USA
A. Zelikovsky - Georgia State Univ., USA

B2.2 Hierarchical Dummy Fill for Process Uniformity

Y. Chen - UCLA, USA
G. Robins - Univ. of Virginia, USA

B2.3 (Embedded Tutorial) : To be Announced

S. Nassif - IBM Austin Research Lab., USA

Wednesday, January 31
Time : 16:00 – 18:00 Room : 311/312
Session C2 : System Level Design

Co-Chairs : *R. Guputa* - Univ. of California Irvine, USA
Y. Takeuchi - Osaka Univ., Japan

C2.1 (Invited Talk) : A C-based Synthesis System, Bach, and Its Application

T. Kambe, A. Yamada, K. Nishida, K. Okada, M. Ohnishi, A. Kay, V. Zammit, P. Boca, T. Nomura - Sharp Corp., Japan

C2.2 Area/Delay Estimation for Digital Signal Processor Cores

N. Togawa, Y. Kataoka, M. Yanagisawa, T. Ohtsuki - Waseda Univ., Japan

C2.3 An RTL Design-Space Exploration Method for High-Level Applications

P. -C. Kao, C.-K. Hsieh, A. C.-H. Wu - Tsing Hua Univ., Taiwan

Wednesday, January 31
Time : 16:00 - 17:30 Room : 313/314
Session D2 : Important Problems in Equivalence Checking

Co-Chairs : *H. Eveking* - Technical Univ. of Darmstadt, Germany
Y. Matsunaga - Fujitsu Labs, Japan

D2.1 Equivalence Checking of Integer Multipliers

Y.-A. Chen, J.-C. Chen - National Chiao Tung Univ., Taiwan

D2.2 Addressing Verification Bottlenecks of Fully Synthesized Processor Cores Using Equivalence Checkers

S. C. Govindarajan, V. Sethuraman - Texas Instruments India Ltd., India

D2.3 An Efficient Solution to the Storage Correspondence Problem for Large Sequential Circuits

W. Cao, D. M. H. Walker - Texas A-M Univ., USA
R. Mukherjee - Fujitsu Labs of America, USA

Thursday, February 1, 9:00 – 12:15

Thursday, February 1
Time : 9:00 - 10:00 Room : 303/304
Keynote Address II :

Market and Technology in PC Products

M.-J. Chien - Chairman, First International Computer, Taiwan

Thursday, February 1
Time : 10:30 - 12:00 Room : 301
Session A3 : Interconnect Design Optimization (II)

Co-Chairs : *D. F. Wong* - Univ. of Texas, USA
I. Harada - ATR, Japan

A3.1 A 3-Step Approach for Performance-Driven Whole Chip Routing

Y. C. Chou, Y. L. Lin - Tsing Hua Univ., China

A3.2 Efficient Minimum Spanning Tree Construction without Delaunay Triangulation

H. Zhou, N. Shenoy, W. Nicholls - Synopsys Inc., USA

A3.3 Memory-Efficient Interconnect Optimization

M. Lai, D. F. Wong - Univ. of Texas, USA

Thursday, February 1
Time : 10:30 - 12:00 Room : 302
Session B3 : Parasitic Extraction and Reduced Order Model

Co-Chairs : *R. Shi* - Univ. of Washington, USA
P. M. Lee - Hitachi Ltd., Japan

B3.1 Balanced Truncation with Spectral Shaping for RLC Interconnects

P. Heydari, M. Pedram - Univ. of Southern California, USA

B3.2 **An Optimum Fitting Algorithm for Generation of Reduced-Order Models**

M. M. Gourary, S. G. Rusakov, S. L. Ulyanov, M. M. Zharov – IPPM, Russia
B. J. Mulvaney - Motorola Inc., Russia

B3.3 **A Virtual 3-D Multipole Accelerated Extractor for VLSI Parasitic Interconnect Capacitance**

Z. Yang, Z. Wang, S. Fang – Tsing Hua Univ., China

Thursday, February 1
Time : 10:30 - 12:00 Room : 311/312
Session C3 : Functional Decomposition and PLA-based Logic Synthesis

Co-Chairs : *R. Murgai* - Fujitsu Labs of America, USA
T. Sasao - Kyushu Inst. of Tech., Japan

C3.1 **On the Minimization of SOP's for Bi-Decomposable Functions**

T. Sasao - Kyushu Inst. of Technology, Japan
J. T. Butler - Naval Postgraduate School, USA

C3.2 **Finding a Good Functional Decomposition for LUT-based FPGA Synthesis**

J. Qiao, M. Ikeda, K. Asada - Univ. of Tokyo., Japan

C3.3s **Logic Synthesis for CPLDs and FPGAs with PLA-Style Logic Blocks**

K. Yan - Sun Microsystems, USA

C3.4s **A New Technology Mapping for CPLD Under Time Constraint**

J.-J. Kim - Chongju Univ., Korea
C.-H. Lin - Semyung Univ., Korea
H.-S. Kim - Chongju Univ., Korea

Thursday, February 1
Time : 10:30 - 12:00 Room : 313/314
Session D3 : Low Power Techniques for Embedded Software

Co-Chairs : *To be Announced*

D3.1 **(Embedded Tutorial) : To be Announced**

To be Announced

D3.2 **Low Power Techniques for Address Encoding and Memory Allocation**

W.-C. Cheng, M. Pedram - Univ. of Southern California, USA

D3.3s **Investigating the Effect of Voltage-Switching on Low-Energy Task Scheduling in Hard Real-Time Systems**

V. Swaminathan, K. Chakrabarty - Duke Univ., USA

Thursday, February 1
Time : 10:45 - 12:15 Room : 303
Session E3 : (Special Session) Asynchronous System Design : Architecture and Low-Power Design

Co-Chairs : *T. Yoneda* – Tokyo Institute of Technology, Japan
D. -I. Lee - Kwangju Institute of Science and Technology, Korea

E3.1 **(Embedded Tutorial) : Asynchronous Technologies for Low Power Design Using Tangram Framework**

J. Kessels - Philips, Netherlands

E3.2 **Imprecise Data Computation for High Performance Asynchronous Processors**

J.-G. Lee, E. Kim, D.-I. Lee - Kwangju Institute of Science and Technology, Korea

Thursday, February 1, 13:30 – 15:30

Thursday, February 1
Time : 13:30 - 15:30 Room : 301
Session A4 : (panel) To be Announced

Moderator : *To be Announced*

Thursday, February 1
Time : 13:30 - 15:30 Room : 302
Session B4 : Analog Design Methodology

Co-Chair : *H. Asai* - Shizuoka Univ., Japan

B4.1 A Pipelined ADC Macro Design for Multiple Applications

K. Tani, N. Nikai, A. Wada, T. Sawai - SANYO Electric Co.,Ltd, Japan

B4.2 A Dynamically Phase Adjusting PLL with a Variable Delay

T. Yasuda, H. Fujita, H. Onodera - Kyoto Univ., Japan

B4.3 Device-Level Placement for Analog Layout: an Opportunity for Non-Slicing Topological Representations

F. Balasa - Univ. of Illinois at Chicago, USA

B4.4 (Embedded Tutorial) : A Mixed-Signal Simulator for VHDL-AMS

X. Liyi, L. Bin, Y. Yizheng - Harbin Institute of Technology, China
H. Guoyong, G. Jinjun, Z. P. Hua - Da IC Design Center, China

Thursday, February 1
Time : 13:30 - 15:30 Room : 311/312
Session C4 : Low Power Design Methodology

Co-Chairs : *M. Yamashina* - NEC Corp., Japan
H. Mizuno - Hitachi Ltd, Japan

C4.1 (Invited Talk) : Low Power Circuit Design

S. Borkar - Intel, USA

C4.2 **An On-Chip 96.5% Current Efficiency CMOS Linear Regulator**

K. Sunaga, T. Endoh, H. Sakuraba ,F. Masuoka - Tohoku Univ., Japan

C4.3s **Reducing Cache Energy through Dual Voltage Supply**

V. Moshnyaga - Fukuoka Univ., Japan

C4.4s **Trace-Driven System-Level Power Evaluation of System-On-a-Chip Peripheral Cores**

T. D. Givargis, F. Vahid - Univ. of California, USA
J. Henkel - NEC, USA

Thursday, February 1
Time : 13:30 - 15:30 Room : 313/314
Session D4 : Advanced BIST : Methodology and Applications

Co-Chairs : *K. Chakrabarty* - Duke Univ., USA
K. Hatayama - Hitachi Ltd., Japan

D4.1 **(Embedded Tutorial) : Towards the Logical Defect Diagnosis for Partial-Scan Designs**

S. -Y. Huang - Tsing Hua Univ., Taiwan

D4.2 **GF(2^p) Cellular Automata as a Built In Self Test Structure**

B. K. Sikdar - Bengal Engineering College, India
D. K. Das - Jadavpur Univ., India
V. Boppana - Fujitsu Labs of America, USA
C. Yang, S. Mukherjee - Fujitsu World Wide System LSI Tech. Ltd., USA
P. P. Chaudhuri - Bengal Eng. College, India

D4.3 **Processor-Programmable Memory BIST for Bus-Connected Embedded Memories**

C.-H. Tsai, C.-W. Wu - National Tsing Hua Univ., Taiwan

D4.4s **A DFT Method for RTL Circuits to Achieve Complete Fault Efficiency Based on Fixed-Control Testability**

S. Ohtake, S. Nagai, H. Wada, H. Fujiwara - Nara Institute of Science and Technology, Japan

Thursday, February 1
Time : 13:30 - 15:30 Room : 303

Session E4 : (Special Session) Asynchronous System Design : Verification

Co-Chairs : *T. Nanya* - Univ. of Tokyo, Japan
J. Kessels - Philips Research, Netherlands

E4.1 (Embedded Tutorial) Timed Circuits: A New Paradigm for High-Speed Design

C. Myrs - Univ. of Utah, USA

E4.2 Conformance and Mirroring for Timed Asynchronous Circuits

B. Zhou, T. Yoneda - Tokyo Institute of Technology, Japan

E4.3 Formal Verification of Pulse-Mode Circuits

X. Kong, R. Negulescu - McGill Univ., Canada

Thursday, February 1, 16:00 – 17:30

Thursday, February 1
Time : 16:00 - 17:30 Room : 301
Session A5 : DSM Design and Analysis

Co-Chair : *T. Akino* - Kinki Univ., Japan

A5.1 A Statical Static Timing Analysis Considering Correlation Between Delays

S. Tsukiyama - Chuo Univ., Japan
M. Tanaka, M. Fukui - Matsushita Corp., Japan

A5.2 Post-Layout Transistor Sizing for Power Reduction in Cell-based Design

M. Hashimoto, H. Onodera - Kyoto Univ., Japan

A5.3 An Efficient Quasi-Multiple Medium Algorithms for Capacitance Extraction of Actual 3-D VLSI Interconnects

W. Yu, Z. Wang – Tsing Hua Univ., China

Thursday, February 1
Time : 16:00 - 17:30 Room : 302
Session B5 : Signal Integrity and Analysis

Co-Chairs : *To be Announced*

B5.1 Improved Crosstalk Modeling for Noise Constrained Interconnect Optimization

J. Cong, D. Z. Pan - Univ. of California, Los Angeles, USA
P. V. Srinivas - Magma Design Automation, Inc., USA

B5.2 KSim: A Stable and Efficient RKC Simulator for Capturing On-Chip Inductance Effect

H. Ji - Univ. of California Santa Cruz,USA
A. Devgan - IBM Corp., USA
W. Dai - Univ. of California Santa Cruz, USA

B5.3 An Efficient Analysis Model of Coupled On-Chip RLC Interconnects

L. Yin, L. He - Univ. of Wisconsin at Madison, USA

Thursday, February 1
Time : 16:00 - 17:30 Room : 311/312
Session C5 : Design Experiments for Mobile Applications

Co-Chairs : *S. Borkar* - Intel Corp., USA
S. Matsushita - NEC Corp., Japan

C5.1 RSA Cryptosystem Design Based on the Chinese Remainder Theorem

C. -H. Wu, J. -H. Hong, C. -W. Wu - National Tsing Hua Univ., Taiwan

C5.2s Speech Recognition Chip for Monosyllables

K. Nakamura - Nara Institute of Science and Technology, Japan
Q. Zhu - Fujitsu Labs Ltd., Japan
S. Maruoka - Hitachi Ltd., Japan
T. Horiyama, S. Kimura, K. Watanabe - Nara Institute of Science and Technology, Japan

C5.3s Low Power Implementation of a Turbo-Decoder on Programmable Architectures

F. Gilbert, A. Worm, N. Wehn - Univ. of Kaiserslautern, Germany

C5.4s Area-Efficient and Reusable VLSI Architecture of Decision Feedback Equalizer for QAM Modem

H. -S Yu, B. W. Kim, Y. G. Cho, J. D. Cho - Sung Kyun Kwan Univ., Korea
J. W. Kim, J. K. Lee, H. C. Park, K. W. Lee - Samsung electronic, Korea

Thursday, February 1
Time : 16:00 - 17:30 Room : 313/314
Session D5 : Compilation Techniques for Embedded Software

Co-Chairs : *To be Announced*

D5.1 (Embedded Tutorial) : To be Announced

To be Announced

D5.2 Optimized Address Assignment for DSPs with SIMD Memory Accesses

M. Lorenz, D. Kottmann, S. Bashford, R. Leupers, P. Marwedel - Univ. of Dortmund, Germany

D5.3s A Formal Approach to Component Based Development of Synchronous Programs

P. Roop, A. Sowmya - The Univ. of New South Wales, Australia
S. Ramesh - Indian Institute of Technology, India

Thursday, February 1
Time : 16:00 - 17:30 Room : 303
Session E5 : (Special Session) Asynchronous System Design : Synthesis

Co-Chairs : *C. Myers* - Univ. of Utah, USA
Y. Sato - Okayama Prefectural Univ., Japan

E5.1 Synthesis of Two-Phase Asynchronous Control Circuits from Pipeline Dependency Graphs

H. Kagotani, T. Okamoto - Okayama Univ., Japan
T. Nanya - Univ. of Tokyo, Japan

E5.2 High-Level Design for Asynchronous Logic

R. Smith, M. Lighart - Theseus Logic, USA

E5.3 Eliminating Isochronic-Fork Constraints in Quasi-Delay-Insensitive Circuits

N. Sretasereekul, T. Nanya - Univ. of Tokyo, Japan

Friday, February 2, 9:00 – 12:00

Friday, February 2
Time : 9:00 - 10:00 Room : 303/304
Keynote Address III :

EDA Must Deliver System-on-Chip Design Solutions

R. Camposano – Technical Officer, Synopsys, Inc., USA

Friday, February 2
Time : 10:30 - 12:00 Room : 301
Session A6 : (Invited Talk) : To be Announced

Speaker: *To be Announced*

Friday, February 2
Time : 10:30 - 12:00 Room : 302
Session B6 : System Level Power Optimization

Co-Chairs : *M. Pedram* - Univ. of Southern California, USA
T. Sato - Kyushu Institute of Technology, Japan

B6.1 **LEneS: Task Scheduling for Low-Energy Systems Using Variable Supply Voltage Processors**
F. Gruian - Lund Institute of Technology, Sweden

B6.2 **A System Level Memory Power Optimization Technique Using Multiple Supply and Threshold Voltages**
T. Ishihara, K. Asada - Univ. of Tokyo, Japan

B6.3 **Low Power High Level Synthesis Using Latches**
W. Yang, I. -C. Park, C.-M. Kyung - KAIST, Korea

Friday, February 2
Time : 10:30 - 12:00 Room : 311/312
Session C6 : Multi-level Logic Optimization for Logic Circuits

Co-Chairs : *S. -Y. Huang* - National Tsing Hua Univ., Taiwan
H. Sawada - NTT, Japan

C6.1 Functional Extension of Structural Logic Optimization Techniques

J. A. Espejo, E. S. Millan, L. Entrena - Univ. Carlos III de Madrid, Spain

C6.2 Improved Alternative Wiring Scheme Applying Dominator Relationship

C. N. Sze, D. Y. L. Wu - The Chinese Univ. of Hong Kong, Hong Kong

C6.3 Design Rewiring Based on Diagnosis Techniques

A. Veneris - Univ. of Toronto, Canada
M. S. Abadir - Motorola Inc., Canada
T. I. Ting - Univ. of Toronto, Canada

Friday, February 2
Time : 10:30 - 12:00 Room : 313/314
Session D6 : Practical and High Level DFT

Co-Chairs : *C. -W. Wu* - National Tsing Hua Univ., Taiwan
T. Inoue - Hiroshima City Univ., Japan

D6.1 Design for Testability Strategies Using Full/Partial Scan Designs and Test Point Insertions to Reduce Test Application Time

T. Hosokawa, M. Yoshimura, M. Ohta - Matsushita Electric Industrial Co., Ltd., Japan

D6.2 A Computer Aided Engineering System for Memory BIST

C. Su - National Central Univ., Taiwan

D6.3 Synthesis of Single-Output Space Compactors with Application to Scan-based IP Cores

B. B. Bhattacharya - Indian Statistical Institute, India
A. Dmitriev, M. Goessel - Univ. of Potsdam, Germany
K. Chakrabarty - Duke Univ., USA

Friday, February 2, 13:30 – 15:30

Friday, February 2
Time : 13:30 - 15:30 Room : 301
Session A7 : Performance Driven Floorplaning and Placement (I)

Co-Chairs : *W. M. Dai* - Univ. of Santa Cruz, USA
H. Murata - Microark Corp., Japan

A7.1 Slicing Floorplans with Clustering Constraints

W. S. Yuen, E. F. Y. Young - Chinese Univ. of Hong Kong, Hong Kong

A7.2 VLSI Floorplanning with Boundary Constraints Based on Corner Block List

Y. Ma, S. Dong, X. Hong, Y. Cai – Tsing Hua Univ., China
C. K. Cheng - Univ. of California, San Diego, USA
J. Gu - Univ. of Hong Kong, Hong Kong

A7.3 Module Placement with Boundary Constraints Using the Sequence-Pair Representation

J. Lai, M. S. Lin - Chung Yuan Christian Univ., Taiwan
T. C. Wang, L. C. Wang - Taxas A-M Univ., USA

A7.4 FAST-SP: A Fast Algorithm for Block Placement Based on Sequence Pair

X. Tang, D. F. Wong - Univ. of Texas, USA

Friday, February 2
Time : 13:30 - 15:30 Room : 302
Session B7 : Improving Delay and Power Estimation

Co-Chairs : *H. Onodera* - Kyoto Univ., Japan
W. Roething - NEC Electronics, Inc., USA

B7.1 Toward Better Wireload Models in the Presence of Obstacles

C. -K. Cheng - Univ. of California San Diego, USA
A. B. Kahng - Univ. of California Los Angeles, USA
B. Liu - Univ. of California San Diego, USA
D. Stroobandt - Gent Univ., Belgium

B7.2 A Fast and Accurate Delay Estimation Method for Buffered Interconnects

Y. Gao, D.F. Wong - Univ. of Texas at Austin, USA

B7.3 **On-Chip Interconnections : Impact of Adjacent Lines on Timing**

D. Deschacht, G. Servel – LIRM/CNRS, France

B7.4 **Short Circuit Power Estimation of Static CMOS Circuits**

S. -H. Jung, J.-H. Baek, S.-Y. Kim - Soongsil Univ., Korea

Friday, February 2
Time : 13:30 - 15:30 Room : 311/312
Session C7 : Networked Reconfiguration and Systems

Co-Chairs : *A. C.-H. Wu* - Tsing Hua Univ., Taiwan
T. Miyazaki - NTT, Japan

C7.1 **A Novel Network Node Architecture for High Performance and Function Flexibility**

T. Murooka, A. Takahara, T. Miyazaki - NTT Network Innovation Lab., Japan

C7.2 **Virtual Java/FPGA Interface for Networked Reconfiguration**

Y. Ha, G. Vanmeerbeeck, P. Schaumont, S. Vernalde, M. Engels - IMEC, Belgium
R. Lauwereins, H. D. Man – Katholieke Universiteit Leuven, Belgium

C7.3 **(Embedded Tutorial) : Coarse Grain Reconfigurable Computing Architecture**

R. Hartenstein - Univ. of Kaiseslautern, Germany

Friday, February 2
Time : 13:30 - 15:30 Room : 313/314
Session D7 : Advances in Timing Optimization of Logic Circuits

Co-Chair : *Y. Tamiya* – Fujitsu Labs, Japan

D7.1 **Efficient Global Fanout Optimization Algorithms**

R. Murgai - Fujitsu Labs of America, Inc., USA

D7.2 **Timing Driven Gate Duplication in Technology Independent Phase**

A. Srivastava, C. Chen, M. Sarrafzadeh - Northwestern Univ., USA

D7.3 **On Speeding Up Extended Finite State Machines Using Catalyst**

S.-Y. Huang - National Tsing Hua Univ., Taiwan

Friday, February 2
Time : 16:00 - 17:30 Room : 301
Session A8 : Performance Driven Floorplaning and Placement (II)

Co-Chairs : *D. F. Wang* - Texas A-M Univ., USA
T. Koide - Univ. of Tokyo, Japan

A8.1 Integrated Power Supply Planning and Floorplanning

I. Lie, H. Chen, A. Aziz, D. F. Wong - Univ. of Texas, USA

A8.2 Post-Layout Timing-Driven Cell Placement Using an Accurate Net Length Model with Movable Steiner Points

A. H. Ajami, M. Pedram - Univ. of Southern California, USA

A8.3s VLSI Block Placement Using Less Flexibility First Principles

S. Dong, Y. Lin, X. Hong – Tsing Hua Univ., China
Y. Wu - The Chinese Univ. of Hong Kong, Hong Kong
J. Gu - Univ. of Hong Kong, Hong Kong

A8.4s A New Congestion-Driven Placement Algorithm Based on Cell Inflation

W. Hou, H. Yu, Y. Cai - Univ. of Hong Kong, Hong Kong
W. H. Kao - Arcadia Design System Inc., Hong Kong
J. Gu - Univ. of Hong Kong, Hong Kong

Friday, February 2
Time : 16:00 - 17:30 Room : 302
Session B8 : Logic Synthesis for Low Power and Design Space Exploration

Co-Chairs : *S. Chakraborty* - Indian Institute of Technology, India
M. Ikeda - Univ. of Tokyo, Japan

B8.1 Cell Selection from Technology Libraries for Minimizing Power

Y. Zhang - Synopsys, Inc., USA
X. Hu, D. Z. Chen - Univ. of Notre Dame, France

B8.2 Low Power Optimization Technique for BDD Mapped Circuits

P. Lindgren, M. Kerttu - Lulea Univ. of Technology, Sweden
M. Thornton - Mississippi State Univ., USA
R. Drechsler - Freiburg Univ., Germany

B8.3 An Accurate Design Exploration of Arithmetic Circuits using Carry-Save-Adder Cells

Y.-T. Kim, T. Kim - KAIST, Korea

Friday, February 2
Time : 16:00 - 17:30 Room : 311/312
Session C8 : Optimization Technique for FPGAs

Co-Chairs : *R. Hartenstein* - Kaiserslautern Univ., Germany
T. Hironaka - Hiroshima City Univ., Japan

C8.1 RPack: Routability-Driven Packing for Cluster-based FPGAs

E. Bozorgzadeh, F. S. Ogrenci, M. Sarrafzadeh - Northwestern Univ., USA

C8.2 Power Minimization in LUT-based FPGA Technology Mapping

Z. -H. Wang, E.-C. Liu, J. Lai - Chun Yuan Christian Univ., Taiwan
T.-C. Wang - Texas A-M Univ., USA

C8.3s Combinatorial Routing Analysis and Design of Universal Switch Blocks

H. Fan - Univ. of Victorial, Canada
J. Liu - The Univ. of Lethbridge, Canada
Y.-L. Wu - The Chinese Univ. of Hong Kong, Hong Kong

C8.4s Automated Synthesis of Pipelined Designs on FPGAs for Signal and Image Processing Applications Described in MATLAB

M. Haldar, A. Nayak, A. Choudhary, P. Banerjee - Northwestern Univ., USA

Friday, February 2
Time : 16:00 - 17:30 Room : 313/314
Session D8 : Processor Synthesis

Co-Chairs : *A. C.-H. Wu* - Tsing Hua Univ., Taiwan
N. Ishiura - Osaka Univ., Japan

D8.1 Effectiveness of the ASIP Design System PEAS-III in Design of Pipelined Processors

A. Kitajima, M. Itoh - Osaka Univ., Japan
J. Sato - Tsuruoka National College of Technology, Japan
A. Shiomi - Sizuoka Univ., Japan
Y. Takeuchi, M. Imai - Osaka Univ., Japan

D8.2 High-Level Specification and Efficient Implementation of Pipelined Circuits

M. C. Marinescu, M. Rinard - MIT, USA

D8.3 High-Level Synthesis under Multi-Cycle Interconnect Delay

J. Jeon, D. Kim, D. Shin, K. Choi - Seoul National Univ., Korea

TUESDAY, JANUARY 30

FULL-DAY Tutorials

TUTORIAL 1 (9:30 – 17:00) Room 311/312
SpecC: Specification Language and Design Methodology
TUTORIAL 2 (9:30 – 17:00) Room 313/314
Software Development Methods for Embedded Systems
TUTORIAL 3 (9:30 – 17:00) Room 411/412
Timing Closure for Ultra Deep Submicron Designs
TUTORIAL 4 (9:30 – 17:00) Room 414/415
IP Authoring and SOC Integration, Verification, and Testing
TUTORIAL 5 (9:30 – 17:00) Room 416/417
Design and Tools for Networked System-on-Chip

ASP-DAC 2001 AT A GLANCE

WEDNESDAY, JANUARY 31

	Room 301	Room 302	Room 311/312	Room 313/314	
9:00	Opening Session (Room 303/304)				
9:30	Keynote Address I (Room 303/304)				
10:30	Coffee Break				
10:45	Executive Panel Discussion : (Room 303/304) Secrets to Success in a Start-Up EDA Business				
12:15	Lunch				
13:30	A1 University LSI Design Contest	B1 Device/ Circuit Co-design -ing for Advanced Techno-logies	C1 System Level Specifi-cation and Simula-tion	D1 Issues in BDD and Sequen-tial Verifica-tion	
15:30	Coffee Break				
16:00	A2 Inter-connect Design Optimiza-tion(I)	B2 Design for Manufact-urability	C2 System Level Design	D2 Important Problems in Equiva-lence Checking	
18:00					

ASP-DAC 2001 AT A GLANCE

THURSDAY, FEBRUARY 1

	Room 301	Room 302	Room 311/312	Room 313/314	Room 303
9:00	Keynote Address II (Room 303/304)				
10:00	Coffee Break				
10:30					
10:45	A3 Inter-connect Design Optimiza-tion(II)	B3 Parasitic Extraction and Reduced Order Model	C3 Functional Decompo-sition and PLA-based Logic Synthesis	D3 Low Power Techni-ques for Embed-ded Software	E3 Asynchronous System Design Architec-ture and Low-Power Design
12:00					
12:15	Lunch				
13:30	A4 (Panel) To Be Announ-Ced	B4 Analog Design Methodo-logy	C4 Low Power Design Methodo-logy	D4 Advanced BIST : Methodo-logy and Applica-tions	E4 Asynchronous System Design Verification
15:30	Coffee Break				
16:00	A5 DSM Design and Analysis	B5 Signal Integrity and Analysis	C5 Design Experi-ments for Mobile Applica-tions	D5 Compila-tion Techni-ques for Embed-ded Software	E5 Asynchronous System Design Synthesis
17:30					
18:30	Banquet				
20:30					

ASP-DAC 2001 AT A GLANCE

FRIDAY, FEBRUARY 2

	Room 301	Room 302	Room 311/312	Room 313/314	
9:00	Keynote Address III (Room 303/304)				
10:00					
10:30	Coffee Break				
	A6 (Invited Talk) To Be Announced	B6 System Level Power Optimization	C6 Multi-level Logic Optimization for Logic Circuits	D6 Practical and High Level DFT	
12:00					
13:30	Lunch				
	A7 Performance Driven Floorplanning and Placement(I)	B7 Improving Delay and Power Estimation	C7 Networked Reconfiguration and Systems	D7 Advances in Timing Optimization of Logic Circuits	
15:30	Coffee Break				
16:00	A8 Performance Driven Floorplanning and Placement(II)	B8 Logic Synthesis for Low Power and Design Space Exploration	C8 Optimization Technique for FPGAs	D8 Processor Synthesis	
17:30					