

ASP-DAC 2004

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Highlights

Keynote Addresses

Wednesday, January 28, 9:00-10:00

“CITRIS: The Center for Information Technology Research in the Interest of Society at the University of California”

Dr. Gary L. Baldwin - Executive Director, CITRIS, University of California, Berkeley, USA

Friday, January 30, 9:00-10:00

“System Level Design Technology for Realizing an Ambient Intelligent Environment”

Dr. Rudy Lauwereins - Vice President, IMEC, Belgium

Special Sessions

1A: Wednesday, January 28, 10:15-12:15, Room 411/412

“Invited Talks: Selected European Activities in SoC Low Power Design Methodologies and Research Networking”

2A: Wednesday, January 28, 13:30-15:30, Room 411/412

“Embedded Tutorial + Regular Session: Embedded System Applications”

3E: Wednesday, January 28, 16:00-18:00, Room 419

“Panel Discussion: Opportunities with the Open Architecture Test System”

Organizers: **K. Hatayama** -Renesas Technology
R. Rajsuman -Advantest America R&D Center

Moderator: **C. Wu** -National Tsing Hua University

Panelists: **R. Rajsuman** -Advantest America R&D Center

Y. Nishimura -Renesas Technology

S. Chakradhar -NEC Laboratories of America

A. Merschon -Guide Technologies

D. Petrich -Wavecrest

T. Tada -Tokushima Bunri University

Firing Lines: **K. Cheng** -University of California Santa Barbara

Y. Okuda -ITC Asian Subcommittee member, Sony

4A: Thursday, January 29, 9:00-10:30, Room 411/412

“Invited Talks: C-Based Design Examples”

6A: Thursday, January 29, 13:30-15:30, Room 411/412
“Embedded Tutorial: RF Modeling and Design Methodology”

6C: Thursday, January 29, 13:30-15:30, Room 414/415
“Presentation + Poster Discussion: University Design Contest”

7A: Thursday, January 29, 16:30-18:00, Room 411/412
“Invited Talks: Future of ITS Technologies in the Ubiquitous Society”

7A-1: The Integration of Vehicles Into a Ubiquitous Computing Environment –Computing and Networking Technologies for Vehicles–

N. Tokitsu (Internet ITS Consortium, Japan)

9A: Friday, January 30, 13:30-15:30, Room 411/412

“Embedded Tutorial: DFM in nm-Process Generation”

9C: Friday, January 30, 13:30-15:30, Room 414/415

“Panel Discussion: Future Reconfigurable Computing System”

Organizers: **M. Kawamura** -Toshiba

H. Amano -Keio University

Moderator: **S. Goto** -Waseda University

Panelists: **M. Motomura** -NEC

T. Sato -IP Flex

S. Trimberger -Xilinx

B. Plunkett -Quick Silver

R. Lauwereins -IMEC

Embedded Invited Talks

1A-1: Wednesday, January 28, 10:15-10:55

Fast, Predictable, and Low-energy Memory References through Architecture-aware Compilation

P. Marwedel, M. Verma, L. Wehmeyer (Univ. of Dortmund, Germany), S. Steinke (KOSTAL GmbH & Co. KG, Luedenscheid, Germany), U. Helmig (Univ. of Dortmund, Germany)

1A-2: Wednesday, January 28, 10:55-11:35

Predictable Design of Low Power Systems by Pre-Implementation Estimation and Optimization

W. H. Nebel (Oldenburg Univ. and OFFIS, Germany)

1A-3: Wednesday, January 28, 11:35-12:15

EuroSoC: Towards a Joint University/Industry Research Infrastructure for System on Chip and System in Package

A. A. Jerraya (TIMA Laboratory, France)

4A-1: Thursday, January 29, 9:10-9:50

C-based Behavioral Synthesis and Verification Analysis on Industrial Design Examples

K. Wakabayashi (NEC, Japan)

4A-2: Thursday, January 29, 9:50-10:30

Using C Based Logic Synthesis to Bridge the Productivity Gap

C. Sullivan, A. Wilson, S. Chappell (Celoxica Ltd, England, UK)

Embedded Tutorials

2A-1: Wednesday, January 28, 13:30-14:30

Toward Mobile Phone Linux

Y. Nakamoto (NEC, Japan)

6A-1: Thursday, January 29, 13:30-14:30

MOSFET Modeling for RF-CMOS Design

M. Miura-Mattausch (Hiroshima Univ., Japan)

6A-2: Thursday, January 29, 14:30-15:30

RF Design Methodologies Bridging System-IC-Module Design

R. A. Mullen (Cadence Design Systems, Inc., USA)

9A-1: Friday, January 30, 13:30-14:10

Toward Stochastic Design for Digital Circuits – Statistical Static Timing Analysis –

S. Tsukiyama (Chuo Univ., Japan)

9A-2: Friday, January 30, 14:10-14:50

Physical CAD Changes to Incorporate Design for Lithography and Manufacturability

L. Scheffer (Cadence Design System, USA)

9A-3: Friday, January 30, 14:50-15:30

Design-Manufacturing Interface for .13 um and Below

A. J. Strojwas (CCMU and PDF Solutions, USA)

Three Full-Day and Two Half-Day Tutorials

FULL-DAY Tutorials:

Tuesday, January 27, 2004, 9:00-17:00

- 1 Recent Advances and Future Challenges in Design Verification

Organizer: **D. Pradhan** -Univ. of Bristol, UK

Speakers: **D. Pradhan** -Univ. of Bristol , **M. Abadir** -Motorola , **R. Drechsler** -Univ. of Bremen

- 2 Design and Runtime Techniques for Leakage Control and Minimization of CMOS VLSI Circuits in Active and Sleep Modes

Organizer: **M. Pedram** , -USC

Speakers: **F. Fallah** -FLA, Fujitsu , **M. Pedram** -USC

- 3 System-Level Design Methodology for SoC Design

Organizer: **D. Gajski** -UCI

Speakers: **M. Fujita** -Univ. of Tokyo , **D. Gajski** -UCI , **T. Hasegawa** -Fujitsu Ltd. , **T. Imai** -Renesas Technology.

HALF-DAY Tutorials:

Tuesday, January 27, 2004, 9:00-12:00

- 4.1 Low Power Design Techniques and Tools

Organizer: **S. Chattoopadhyay** -Intel Corp.

Speakers: **Subhomoy Chattoopadhyay** -Intel Corp. , **R. Patel** -Intel Corp.

Tuesday, January 27, 2004, 13:30-16:30

- 4.2 Energy, Fault-tolerance, and Scalability Issues in Designing Networks-on-chip

Organizer: **R. Marculescu** -Carnegie Mellon University, USA

Speaker: **R. Marculescu** -Carnegie Mellon University

Welcome to ASP-DAC 2004

It is my pleasure and honor, on behalf of the Organizing Committee, to welcome you to the Asia and South Pacific Design Automation Conference 2004 (ASP-DAC 2004), a sister conference of DAC, DATE, and ICCAD. ASP-DAC 2004 will be held at Pacifico Yokohama, Kanagawa Prefecture, Japan from January 27 through 30, 2004. This year's ASP-DAC will be held again in the Pacifico Yokohama, Japan, jointly with Electronic Design and Solution Fair 2004. Because Yokohama area has many electronics industries and EDA companies, and many conferences and exhibitions are held here, Pacifico Yokohama is a familiar place for many of us.

The goal of the ASP-DAC is to provide the researchers and engineers working in the area of SoC/ VLSI/Embedded System design and EDA/CAD technologies, with the access to global level leading edge information and opportunities for discussion and information exchange on these topics.

We are preparing outstanding Keynote Addresses on ubiquitous computing, ITS (Intelligent Transport Systems), and future electronic systems and EDA Technologies, by the authorities of these areas. The details will be announced soon.

The Technical Program Committee, under the leadership of Prof's. Hidekazu Terai, Nikil Dutt, Xianlong Hong, and Masahiro Fujita, have reviewed 291 papers from 28 countries to organize the outstanding program. After careful selection, 148 papers are selected for presentation in the Conference. The selected papers cover the wide variety of hot topics from system level design to physical design including embedded systems, reconfigurable systems, analog circuits, and TCAD.

The program also includes a session for design examples and panel discussions. The University LSI Design Contest is also an important event of ASP-DAC, which focuses on a real chip design in academia. The Design Contest Committee, chaired by Prof's Makoto Ikeda and Xiaoyang Zeng, selected excellent designs for presentation.

On Tuesday, tutorials are scheduled to give complete introductions to the state-of-the-art SoC design and CAD topics.

ASP-DAC 2004 will be a precious opportunity for you to find valuable information by exchanging ideas with researchers and engineers working on SoC/VLSI design technologies.

We would be more than happy if we could provide you with a valuable and enjoyable experience in this conference. We look forward to meeting with you in Yokohama.



Masaharu Imai
General Chair
ASP-DAC 2004

Sponsorship

Sponsored by:



IEEE Circuits and Systems Society
<http://www.ieee-cas.org>



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<http://www.sigda.org>



IEICE ESS (Institute of Electronics, Information and Communication Engineers - Engineering Sciences Society)
<http://www.ieice.org>



IPJS SIGSLDM (Information Processing Society of Japan - SIG System LSI Design Methodology)
<http://www.ipsj.or.jp>

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Organizing Committee

General Chair

Masaharu Imai

Osaka University

1-3 Machikane-yama, Toyonaka, Osaka, 560-8531 Japan
Phone: 06-6850-6625 FAX: 06-6850-6627
imai@ist.osaka-u.ac.jp

Past Chair/ SC Chair

Hiroto Yasuura
Kyushu University

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Yoshinori Takeuchi
Osaka University

Kazuhito Ito

Saitama University

Hiroyuki Tomiyama

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Ritsumeikan University

Nikil Dutt

University of California, Irvine

Xianlong Hong

Tsinghua University

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Masahiro Fujita
University of Tokyo

TPC Secretaries

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Osaka University

Keishi Sakanushi
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Masahiro Fukui
Ritsumeikan University

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University of Tokyo

Zeng Xiaoyang

Fudan University

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Sanyo Electric Co.

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Tokyo Institute of Technology

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Tokyo Institute of Technology

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Tokyo University of Agriculture and Technology

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Kyushu University

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Hiromitsu Fujii
Nihon Synopsys Co., Ltd.

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Tokinori Kozawa
STARC

Kenji Yoshida

Cadence Design Systems, Japan

ASP-DAC Rep. at DAC

Hidetoshi Onodera
Kyoto University

ASP-DAC Rep. at DATE

Masaharu Imai
Osaka University

IEICE/CAS Rep.

Tokinori Kozawa
STARC

IEICE/ICD Rep.

Michitaka Kameyama
Tohoku University

IEICE/VLD Rep.

Masao Yanagisawa
Waseda University

IPSJ/SLDM Rep.

Hidekazu Terai
Ritsumeikan University

JIEP Rep.

Akinori Kanasugi
Tokyo Denki University

IWCM Rep.

Mitiko Miura-Mattausch
Hiroshima University, Japan

JEITA/EDA TC Rep.

Mitsuru Nadaoka
Oki Electric Industry

EDSF Chair

Masaki Hayashi
Sharp

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Japan Electronics Show Association

Yoshinori Ishizaki

Japan Electronics Show Association

Mieko Mori

Japan Electronics Show Association

Kohei Torikai

Japan Electronics Show Association

Yuka Arikawa

Japan Electronics Show Association

Technical Program Committee

Co-Chairs

Hidekazu Terai
Ritsumeikan University
terai@se.ritsumeai.ac.jp

Nikil Dutt
University of California, Irvine
dutt@uci.edu

Xianlong Hong
Tsinghua University
hxl-dcs@tsinghua.edu.cn

Vice Chair
Masahiro Fujita
University of Tokyo
fujita@ee.t.u-tokyo.ac.jp

Secretaries

Keishi Sakanushi
Osaka University
sakanusi@ist.osaka-u.ac.jp

Kiyoharu Hamaguchi
Osaka University
hama@ics.es.osaka-u.ac.jp

Masahiro Fukui
Ritsumeikan University
mfukui@se.ritsumeai.ac.jp

Subcommittees

(* / † indicate the subcommittee chair/vice-chair.)

[1] System Level Design Methodology

* **Kazutoshi Wakabayashi**
NEC

† **Dai Araki**
InterDesign Technologies, Inc.

Jun-Dong Cho
SungKyunKwan University

Tony Givargis
University of California, Irvine

Joerg Henkel
NEC Lab.

Tohru Ishihara
Fujitsu Laboratories of America, Inc.

Nagisa Ishiura
Kwansei Gakuin University

Akira Kawaguchi
GAIA System

Wayne Luk
Imperial College

Radu Marculescu
Carnegie Mellon University

Hiroshi Nakamura
University of Tokyo

Loganath Ramachandran
Synopsys

Wolfgang Rosenstiel
University Tubingen

Katsuharu Suzuki
NEC Corp.

Wayne Wolf
Princeton University

Allen C. -H. Wu
Tsing Hua University

Qiang Zhu
Fujitsu Labs.

[2] Embedded and Real-Time Systems

* **Hiroaki Takada**
Nagoya University

† **Hiroyuki Tomiyama**
Nagoya University

Naehyuck Chang
Seoul National University

Pai Chou
University of California, Irvine

Xiaobo Sharon Hu
University of Notre Dame

Ing-Jer Huang
National Sun Yat-Sen University

Akihiko Inoue
Matsushita Electric Industrial Co. Ltd.

Ahmed Amine Jerraya
TIMA/INPG

Tatsuo Nakajima
Waseda University

Preeti Ranjan Panda
Indian Institute of Technology, Delhi

[3] Behavioral/Logic Synthesis and Optimization

* **Yusuke Matsunaga**
Kyushu University

Rolf Drechsler
University of Bremen

Hiroyuki Higuchi
Fujitsu Laboratories

Yuji Kukimoto
Cadence Design Systems

Wolfgang Kunz
University of Kaiserslautern

Shin-ichi Minato
NTT

Rajeev Murgai
Fujitsu Laboratories of America

Hiroyuki Ochi
Hiroshima City University

Tsutomu Sasao
Kyushu Institute of Technology

Shigeru Yamashita
NAIST

[4] Validation and Verification for Behavioral/Logic Design

* **Kazuhiko Eguchi**
Aichi Institute of Technology

† **Masahiko Toyonaga**
Kochi University

Stephen P. G. Chappell
Celoxica Ltd.

Atsuo Hotta
Aichi Institute of Technology

Minoru Inamori
NTT Cyber Space Laboratories

Satoshi Kojima
Mentor Graphics Japan Co. Ltd

Tsu-wei Ku
Apex Design Systems, Inc.

Yuichiro Mori
Kochi University

Kouichi Nagami
Network Innovation Laboratories

S. K. Nandy
Indian Institute of Science

Goro Suzuki
The University of Kitakyushu

Chang Joseph Sylvester
Nanyang Technological University

Kazuyoshi Takagi
Nagoya University

Atsushi Takahara
NTT BizLink, Inc.

Tomohiro Yoneda
Tokyo Institute of Technology

[5] Optimization and Verification in Circuit and Chip

* **Masanori Hashimoto**
Kyoto University
Charlie Chung-ping Chen
National Taiwan University
Chung-kuan Cheng
University of California, San Diego
Atsushi Kurokawa
STARC
David Z. Pan
The University of Texas at Austin

Sachin Sapatnekar
University of Minnesota
Takashi Sato
Renesas Technology Corp.
Masaaki Yamada
Toshiba Microelectronics
Ryuichi Yamaguchi
Matsushita Electric Industrial Co. Ltd.
Janet Meling Wang
University of Arizona at Tucson

[6] Performance Driven Physical Design

* **Takahiro Watanabe**
Waseda University
† **Kazuhiro Takamizawa**
Euphonic Technologies, Inc.
Wayne Dai
UC Santa Cruz
Toshihiro Hattori
SuperH (Japan), Ltd.
Xianlong Hong
Tsinghua University
Mineo Kaneko
JAIST
Kaoru Kawamura
Fujitsu lab.
Hitoshi Kitazawa
Tokyo University of Agriculture and Technology
Cheng-kok Koh
Purdue University
Tetsushi Koide
Hiroshima University
Shigetoshi Nakatake
The University of Kitakyushu
Michiroh Ohmura
Hiroshima Institute of Technology

Nobuto Ono
SII EDA Technologies Inc.
Shunji Saika
Matsushita Electric Industrial Co. Ltd.
Youichi Shiraishi
Gunma University
Atsushi Takahashi
Tokyo Institute of Technology
Yasuhiro Takashima
FAIS
Shuji Tsukiyama
Chuo University
Masahiko Toyonaga
Kochi University
Shin'ichi Wakabayashi
Hiroshima City University
Masaaki Yamada
Toshiba Microelectronics
Yan Zhang
University of California, Los Angeles
Takeshi Yoshimura
Waseda University

[7] Test Technology and Design for Testability

* **Terumine Hayashi**
Mie University
† **Koji Nakamae**
Osaka University
Takashi Aikyo
Fujitsu Ltd.
Kazumi Hatayama
Renesas Technology Corp.
Toshinori Hosokawa
Nihon University
Michiko Inoue
NAIST
Kuen-Jong Lee
National Cheng Kung University

Yukiya Miura
Tokyo Metropolitan University
Alex Orailoglu
University of California, San Diego
Rochit Rajsuman
Advantest America R&D Center, Inc.
Yasuo Sato
STARC
Chauchin Su
National Chiao Tung University
Hiroshi Takahashi
Ehime University
Masaaki Yoshida
NEC electronics corporation

[8] Analog and RF Circuit Design

* **Koichiro Mashiko**
STARC
† **Shoji Kawahito**
Shizuoka University
Akira Hyogo
Tokyo University of Science
Masao Ito
Renesas Technology Corp.
Wing-Hung Ki
HKUST

Haruo Kobayashi
Gunma University
Seiji Mori
Innotech Corporation
Makoto Nagata
Kobe University
Sri Parameswaran
University of New South Wales

[9] Design for Manufacturability (TCAD)

* **Hiroo Masuda**
STARC
Uwe Feldmann
Infineon Technologies
Yasunori Iwatsu
Toshiba Microelectronics Center
Kenji Nishi
Kinki University Tech. College

Kenichiro Sonoda
Renesas Technology Corp.
Albert Wang
ILLINOIS INSTITUTE OF TECHNOLOGY
Masaharu Yamamoto
STARC
Zhiping Yu
Tsinghua University

[10] Reconfigurable Systems

* **Masahiko Kawamura**
Toshiba Corp.
† **Hideharu Amano**
Keio University
Yao-wen Chang
National Taiwan University
Kamal Chaudhary
Xilinx Corp.
Kiyoung Choi
Seoul National University
Andre' DeHon
Caltech
Thomas Huang
Aptix Corp.

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University of Kaiserslautern
Nobuki Kajihara
NEC
Majid Sarrafzadeh
University of California, Los Angeles
Gary Spivey
George Fox University
Joshua Walstrom
Altera Corp.
Takashi Yokota
Utsunomiya University

[11] Leading-Edge Design Experiments

* **Takao Onoye**
Osaka University
† **Hiroyuki Okuhata**
Synthesis Corporation
Hideki Ando
Nagoya University
Seongsoo Lee
Soongsil University

Satoshi Matsushita
NEC Corporation
Takashi Miyamori
Toshiba Corporation
Yulu Yang
Nankai University

University LSI Design Contest Committee

Co-Chairs

Makoto Ikeda
University of Tokyo
ikeda@silicon.u-tokyo.ac.jp

Zeng Xiaoyang
Fudan University
xyzeng@fudan.edu.cn

Vice Chair

Hideki Yamauchi
Sanyo Electric Co.
yamauchi@ul.rd.sanyo.co.jp

Chi-Ying Tsui
The Hong Kong University of
Science and technology
Hideharu Amano
Keio Univ.
Hideo Owada
Fujitsu Lab.
Hidetoshi Onodera
Kyoto University
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Toshiro Tsukada
STARC
Vojin G Oklobdzija
University of California

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Chair

Hiroto Yasuura
Kyusyu University
yasuura@c.csce.kyushu-u.ac.jp

Vice Chair

Takeshi Yoshimura
Waseda University
E-mail: t-yoshimura@waseda.jp

Secretary

Toshihiro Hattori
SuperH Japan, Ltd.
toshihiro.hattori@superh.com

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Tata Consultancy Services

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Waseda University

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search Center

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Secretary

Kazutoshi Wakabayashi
NEC Corporation
wakaba@ccm.ci.nec.co.jp

IEICE TGICD Chair
Mihcitaka Kameyama
Tohoku University

IPSJ SIG SLDM Chair
Hidekazu Terai
Ritsumeikan University

STARC Rep.
Tokinori Kozawa
Semiconductor Technology Academic Re-
search Center

JIEP Rep.
Akinori Kanasugi
Tokyo Denki University

International Members

Richard M.M. Chen
City University of Hong Kong
Graham R. Hellestrand
VaST Systems Technology Corporation

Xian-Long Hong
Tsinghua University, Beijing

Chong-Min Kyung
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Technology

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Genentech
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Nara Institute of Science and Technology

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Cadence Design Systems, Japan

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Takashi Kambe
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Hiroaki Kunieda
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Hidetoshi Onodera
Kyoto University

Isao Shirakawa
Professor Emeritus of Osaka University

Kenji Yoshida
Cadence Design Systems, Japan

University LSI Design Contest

The University LSI Design Contest was conceived as a unique program of ASP-DAC Conference. The purpose of the Contest is to encourage education and research in LSI design, and its realization on chips at universities, and other educational organizations by providing opportunities to present and discuss innovative and state-of-the-art designs at the conference. Application areas and types of circuits include (1) Analog and Mixed-Signal Circuits, (2) Digital Signal processing, (3) Microprocessors, and (4) Custom Application Specific Circuits. Methods or technology used for implementation include (a) Full Custom and Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices, including FPGA/PLDs.

This year, twenty-eight selected designs from seven countries/areas will be disclosed in Session 6C with a short presentations followed by live discussions in front of posters. Submitted designs were reviewed by the members of the University Design Contest Committee based on the following criteria: Reliability of design and implementation, Quality of implementation, Performance of the design, Novelty, and Additional special features. In the selection process, emphasis was placed more on reliability, quality, and performance. As a result, the twenty-eight designs were selected. Also, we have instituted one outstanding design award.

It is with great pleasure that we acknowledge the contributions to the Design Contest, and it is our earnest belief that it will promote and enhance research and education in LSI design in academic organizations. It is also our hope that many people not only in academia but in industry will attend the contest and enjoy the stimulating discussions.

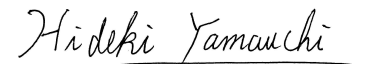
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Electronic Design and Solution Fair 2004

Broadband communications are propelling our society toward an age in which anyone anywhere will be able to easily relay and receive information of all kinds. In the home, electronic equipment will be linked together into far-reaching digital networks. Semiconductors are at the heart of this "digital revolution." Semiconductors must rapidly improve in performance and energy efficiency, breaking through the boundaries of what is possible today to reach new heights. Japan's Semiconductor MIRAI Project-a national R&D project for next-generation technologies-and a variety of other research and development efforts are being promoted to establish process and design technologies for SoC (Systems-on-Chip). In line with these efforts, needs are growing for higher-level electronic circuit design technologies, and solutions technologies such as software. In its 4th year, Electronic Design and Solution Fair 2004 (EDSFair2004) is Asia's Leading Exhibition of Essential Design Solution for SoC Technologies. Here, you will find new design and solutions technologies combining cutting-edge electronic design automation (EDA), device and IP (intellectual property) design service technologies. Since 2001, when a cooperative partnership was launched with the Electronic Design Automation Consortium (EDAC) of the United States, EDSFair has risen to prominence as an international convention on a par with the Design Automation Conference (DAC) in America and Design, Automation and Test in Europe (DATE). EDSFair has also won strong global acclaim as the largest exhibition of its kind in Asia. EDSFair2004 will be held on January 29 and 30, 2004, in Pacifico Yokohama. Simultaneous events, such as the FPGA/PLD Design Conference, University Plaza and ASP-DAC (Asia and South Pacific Design Automation Conference), will enrich and enhance the EDSFair's effectiveness as a place for technological interchange between industry, academia and government organizations. I am confident that this event will provide exhibitors and visitors alike with unique opportunities for information exchange and new business development. All of us involved with the Fair look forward to your active participation.

General Information

Name:

Electronic Design and Solution Fair 2004

Period:

Thursday, January 29 - Friday, January 30, 2004
(2 days)

Place:

Pacifico Yokohama
1-1-1, Minato Mirai, Nishi-ku, Yokohama 220-0012, Japan

Hours:

10:00 a.m. to 6:00 p.m.

Admission Fees:

Exhibition: Free (registration required at show entrance)
Conferences: Fees will be charged for some conferences

Sponsor:

Japan Electronics and Information Technology Industries Association (JEITA)

Cooperation:

Electronic Design Automation Consortium (EDAC)

Support (expected) :

Ministry of Economy, Trade and Industry, Japan
Embassy of the United States of America in Japan
U.S. Semiconductor Industry Association (SIA)
Distributors Association of Foreign Semiconductors (DAFS)

Assistance (expected) :

Institute of Electronics, Information and Communication Engineers (IEICE)
Information Processing Society of Japan (IPSJ)
Japan Printed Circuit Association (JPCA)

Management:

Japan Electronics Show Association (JESA)

URL:

<http://www.edsfair.com>

Invitation to ASP-DAC 2005


On behalf of the Organizing Committee, it is my great pleasure and honor to invite all of you to ASP-DAC 2005, which is the 10th event of this conference series. The conference will be held from January 18 to 21, 2005 at Hotel Equatorial, Shanghai, China. This time, TPC Co-chairs of the Conference are Professor Xianlong Hong from Tsinghua Univ., Beijing; Professor Hidekazu Terai from Ritsumeikan University, Japan; Professor C.K.Cheng from UCSD, U.S.A and Professor Youn-Long Lin from Tsinghua Univ., Hsinchu. Their research fields cover almost all the main technical aspects of IC design from system level design methodology to physical design of System LSI or SoC. In order to make this conference more attractive and successful, we do need your help and cooperation. The conference has traditionally a strong impact on both industries and academia. We hope the excellent tradition can be deepened and carried forward through this conference.

As you know, Shanghai is becoming one of the most important microelectronic industrial bases in China, even in the world several years later. Now, a lot of worldwide famous corporations enter and be stationed in Shanghai and nearby area. Those enterprises involved IC manufacturing; design, testing and packaging have sprung up like mushroom. A complete IC industry chain is being grown up in Yangtze River Delta region of China. Taking the opportunity of ASP-DAC 2005, we sincerely welcome the attendees from various countries and regions to visit our universities, institutes and enterprises to further carry out technology and academic exchange. It will certainly promote the development of IC industry in China and collaboration between us. By the way, Shanghai is also a good place for sightseeing. You can go to those scenery points as the Bund, Yu Garden, Shanghai Museum, Shanghai Grand Theater, Xintiandi and so on.

ASP-DAC 2005 is waiting for you!

Shanghai is waiting for you!

Wish you have a good time in China!



Ting-Ao Tang
General Chair,
ASP-DAC 2005

Keynote Addresses

Keynote Address I

Wednesday, January 28, 9:00-10:00
**“CITRIS: The Center for Information
Technology Research in the Interest
of Society at the University of California”**
Dr. Gary L. Baldwin

Executive Director, CITRIS, University of
California, Berkeley, USA



This talk will give an overview of CITRIS and the unique approach to its research, interaction with industry, and the implications of its education programs.

The Center for Information Technology in the Interest of Society (CITRIS) was founded on July 1, 2001, as a collaboration among the University of California at Berkeley (UCB), Davis (UCD), Merced (UCM) and Santa Cruz (UCSC). The CITRIS mission is to sponsor and house collaborative information technology (IT) research to provide solutions to grand-challenge social and commercial problems affecting the quality of life of individuals and organizations. CITRIS is one of four California Institutes of Science and Innovation established by Governor Gray Davis to create a partnership between the University of California and state's leading-edge businesses to lay the foundation for the "next New Economy."

The CITRIS research agenda now embraces more than 200 faculty members from over 50 departments among the four participating U.C. campuses. It encompasses over 150 separate research activities, sponsored both by external funding agencies as well as through CITRIS seed funds. CITRIS has identified Societal-Scale Information Systems (SISs) as core research vehicles for addressing many of the societal problems of large scale that we face today and anticipate in the future. In this context, "societal"; refers both to the size and impact of the proposed system, as well as one of our most important metrics of success - it must improve people's lives and the lives of organizations.

Whether it involves

- the simple act of buying an energy-efficient refrigerator or source of illumination, or monitoring buildings, bridges, and highways for structural integrity during an earthquake, or
 - monitoring the status and delivering medications in home health care devices for the elderly, or
 - delivering educational course materials over diverse geographies, or
 - aiding fire and rescue teams in navigating safely through smoke-filled buildings, or
 - guarding the quality of our food and water,
- an SIS can be applied to collect, understand, and help people with the vast quantities of information needed to address these problems. This partial list of societal-scale applications is being addressed by an extensive, evolving, and diverse set of research projects within CITRIS, all linked by their relevance to societal impact.

Our initial vision for one of the most important SISs is that it will integrate vast numbers of tiny wireless sensors, hand-held information devices, large computing clusters, and large data sets into systems that make it easy for all citizens to monitor and gather data. The sensors themselves must be very cheap and operate without batteries so that they become widely used and require no maintenance. There must be a reliable network to connect the sensors to monitoring systems in a way that requires no action on the part of the user to install, activate or maintain. The network must be secure, so that privacy is respected and malicious use cannot occur. By thinking through these system requirements, from the highest user interface to basic device and algorithmic structures, the CITRIS project portfolio is embracing all of these challenges and more.

CITRIS is a public-private partnership whose long-term success depends upon fostering an open and collaborative relationship between the State of California and the federal government (through grants and contracts), CITRIS industrial partners, and CITRIS University partners.

This is a dangerous number to quote. I'm sure we wouldn't be precise. Does it include the CITRIS seeded projects as well as federal and state funded? We'd never get this right. I suggest leaving it out. GLB

Keynote Address II
Friday, January 30, 9:00-10:00
**“System Level Design Technology
for Realizing an Ambient
Intelligent Environment”**

Dr. Rudy Lauwereins
Vice President, IMEC, Belgium



The advent of the intelligent environment or "ambient intelligence" is a serious challenge for the systems designer. The systems of the future are small, complex, flexible and consume little energy. These conflicting requirements require new ways of designing that differ radically from conventional methods. This keynote presentation presents a vision towards the ambient intelligent environment, describes the properties of the systems we need to build and derives the design challenges we are facing.

Technical Program

Posters are exhibited in Room 418 if * after the paper ID

Wednesday, January 28, 8:30-10:00

Wednesday, January 28, 8:30-9:00 Small Auditorium
Opening Session:

Wednesday, January 28, 9:00-10:00 Small Auditorium
Keynote Address I:

CITRIS: The Center for Information Technology Research in the Interest of Society at the University of California

Dr. Gary L. Baldwin - Executive Director, CITRIS, University of California, Berkeley, USA

Wednesday, January 28, 10:15-12:15

Wednesday, January 28, 10:15-12:15 Room 411/412
Session 1A: (Special Session) Selected European Activities in SoC Low Power Design Methodologies and Research Networking

Co Chairs: **W. Rosenstiel** – Univ. of Tuebingen, Germany
M. Fujita – Univ. of Tokyo, Japan

1A-1 (Embedded Invited Talk): Fast, Predictable, and Low-energy Memory References through Architecture-aware Compilation

P. Marwedel, M. Verma, L. Wehmeyer (Univ. of Dortmund, Germany), S. Steinke (KOSTAL GmbH & Co. KG, Luedenscheid, Germany), U. Helmig (Univ. of Dortmund, Germany)

1A-2 (Embedded Invited Talk): Predictable Design of Low Power Systems by Pre-Implementation Estimation and Optimization

W. H. Nebel (Oldenburg Univ. and OFFIS, Germany)

1A-3 (Embedded Invited Talk): EuroSoC: Towards a Joint University/Industry Research Infrastructure for System on Chip and System in Package

A. A. Jerraya (TIMA Laboratory, France)

Wednesday, January 28, 10:15-12:15 Room 413
Session 1B: Floorplanning

Co Chairs: **X. Hong** – Tsinghua Univ., China
K. Takamizawa – Euphonic Technologies, Inc., Japan

1B-1 Abstraction and Optimization of Consistent Floorplanning with Pillar Block Constraints

N. Fu, S. Nakatake, Y. Takashima, Y. Kajitani (Univ. of Kiatakyushu, Japan)

1B-2 Space Planning: Placement of Modules with Controlled Empty Area by Single Sequence

X. Zhang (SII EDA Technologies Inc., Japan), Y. Kajitani (The Univ. of Kitakyushu, Japan)

1B-3 Layer Assignment for Reliable System-on-Package

J. R. Minz, S. K. Lim (Georgia Inst. of Tech., Atlanta, USA)

1B-4s On Handling Arbitrary Rectilinear Shape Constraint

X. Tang (Cadence, USA), M. Wong (Univ. of Illinois, USA)

1B-5s Robust Fixed-outline Floorplanning through Evolutionary Search

C. Lin, D. Chen, Y. Wang (Feng-Chia Univ., Taiwan)

Wednesday, January 28, 10:15-12:15 Room 414/415
Session 1C: Modeling for Analog Circuits

Co Chairs: **Y. Huang** – National Chiao Tung Univ., Taiwan
M. Nagata – Kobe Univ., Japan

1C-1 Analog Circuit Behavioral Modeling via Wavelet Collocation Method with Auto-Companding

J. Wang, J. Tao, X. Zeng (Fudan Univ., China), C. Chiang (Synopsys Inc., USA), D. Zhou (Univ. of Texas at Dallas, USA)

1C-2 High-level Modeling of Continuous-Time $\Delta\Sigma$ A/D-Converters Using Formal Models

E. S. Martens, G. Gielen (KU Leuven, Belgium)

1C-3 High-Frequency Noise in RF Active CMOS Mixers

P. Heydari (Univ. of California, Irvine, USA)

1C-4 On Mismatch in the Deep Sub-Micron Era - from Physics to Circuits

R. O. Topaloglu, A. Orailoglu (UCSD, USA)

Wednesday, January 28, 10:15-12:15 Room 416/417
Session 1D: Behavioral Synthesis

Co Chairs: **P. Chou** – Univ. of California, Irvine, USA
A. Yamada – Sharp, Japan

1D-1 Register Binding and Port Assignment for Multiplexer Optimization

D. Chen, J. Cong (UCLA, USA)

1D-2 A Thread Partitioning Algorithm in Low Power High-Level Synthesis

J. Uchida (Waseda Univ., Japan), N. Togawa (The Univ. of Kitakyushu, Waseda Univ., Japan), M. Yanagisawa, T. Ohtsuki (Waseda Univ., Japan)

1D-3 Minimization of Fractional Wordlength on Fixed-Point Conversion for High-Level Synthesis

N. Doi (Waseda Univ., Japan), T. Horiyama (Kyoto University, Japan), M. Nakanishi (NAIST, Japan), S. Kimura (Waseda Univ., Japan)

1D-4 A Procedure for Obtaining a Behavioral Description for the Control Logic of a Non-linear Pipeline

H. H. Najaf-abadi (Sharif Univ. of Tech., Iran)

Wednesday, January 28, 10:15-12:15 Room 419
Session 1E: Delay Test and BIST

Co Chairs: **S. Chakradhar** – NEC Labs. America, USA
H. Takahashi – Ehime Univ., Japan

1E-1 TranGen: A SAT-Based ATPG for Path-Oriented Transition Faults

K. Yang, K. Cheng, L. Wang (UC-Santa Barbara, USA)

1E-2 Longest Path Selection for Delay Test under Process Variation

X. Lu, Z. Li, W. Qiu, D. M. Walker, W. Shi (Texas A&M Univ., USA)

1E-3 SRAM Delay Fault Modeling and Test Algorithm Development

R. Huang, Y. Lai, Y. Chou, C. Wu (National Tsing Hua Univ., Taiwan)

1E-4s An Efficient Design of Non-linear CA Based PRPG for VLSI Circuit Testing

S. Das, D. Dey, B. K. Sikdar, P. Pal Chaudhuri (B E College, India)

1E-5s Combinatorial Group Testing Methods for the BIST Diagnosis Problem
A. B. Kahng, S. Reda (UCSD, USA)

Wednesday, January 28, 13:30-15:30

Wednesday, January 28, 13:30-15:30 Room 411/412
Session 2A: (Special Session) Embedded System Applications

Co Chairs: **H. Tomiyama** – Nagoya Univ., Japan
A. A. Jerraya – TIMA Laboratory, France

- 2A-1 (Embedded Tutorial): Toward Mobile Phone Linux**
Y. Nakamoto (NEC, Japan)
- 2A-2 Power Control of CDMA Systems with Successive Interference Cancellation Using the Knowledge of Battery Power Capacity**
Y. Wang (ASTRI, Hong Kong), C. Tsui, S. R. Cheng, W. Mow (The Hong Kong Univ. of Science and Tech., Hong Kong)
- 2A-3 Rate Analysis for Streaming Applications with On-Chip Buffer Constraints**
A. Maxiaguine, S. Kuenzli (ETH Zurich, Switzerland), S. Chakraborty (NUS Singapore, Singapore), L. Thiele (ETH Zurich, Switzerland)

Wednesday, January 28, 13:30-15:30 Room 413
Session 2B: Placement

Co Chairs: **M. Wong** – Univ. of Illinois, USA
T. Sato – Renesas Tech. Corp., Japan

- 2B-1 Performance-driven Global Placement via Adaptive Network Characterization**
M. Ekpanyapong, S. K. Lim (Georgia Inst. of Tech., USA)
- 2B-2 Temperature-Aware Global Placement**
B. Obermeier, F. Johannes (Technical Univ. of Munich, Germany)
- 2B-3 High Speed Layout Synthesis for Minimum-Width CMOS Logic Cells via Boolean Satisfiability**
T. Iizuka, M. Ikeda, K. Asada (Univ. of Tokyo, Japan)
- 2B-4s An Integrated Approach to Timing-Driven Synthesis and Placement of Arithmetic Circuits**
K. Shin, T. Kim (KAIST, South Korea)

2B-5s Layer Assignment for Crosstalk Risk Minimization
D. Wu, J. Hu, R. N. Mahapatra (Texas A&M Univ., USA), M. Zhao (Motorola Inc., USA)

Wednesday, January 28, 13:30-15:30 Room 414/415
Session 2C: RF Design Methodology

Co Chairs: **W. Ki** – HKUST, Hong Kong
A. Matsuzawa – Tokyo Inst. Tech., Japan

- 2C-1 CrtSmile: A CAD Tool for CMOS RF Transistor Substrate Modeling Incorporating Layout Effects**
Z. Li (Univ. of Washington, USA), R. Suravarapu (Oregon State Univ., USA), R. Hartono, S. Bhattacharya (Univ. of Washington, USA), K. Mayaram (Oregon State Univ., USA), R. Shi (Univ. of Washington, USA)
- 2C-2* NSGA-Based Parasitic-Aware Optimization of a 5GHz Low-Noise VCO**
M. Chu, D. J. Allstot (Univ. of Washington, USA), J. M. Huard, K. Y. Wong (National Semiconductor Corp., USA)
- 2C-3 Analytical Expressions for Phase Noise Eigenfunctions of LC Oscillators**
P. Ghanta (Univ. of Arizona, USA), Z. Li, J. Roychowdhury (Univ. of Minnesota, USA)
- 2C-4 Analysis of MOS Cross-Coupled LC-Tank Oscillators Using Short-Channel Device Equations**
M. M. Mansour (Berkeley Design Automation, USA), M. M. Mansour (American Univ. of Beirut, Lebanon), A. Mehrotra (Univ. of Illinois at Urbana-Champaign, USA)

Wednesday, January 28, 13:30-15:30 Room 416/417
Session 2D: Practical Issues in Logic Synthesis

Co Chairs: **Y. Kukimoto** – Cadence, USA
Y. Matsunaga – Kyushu Univ., Japan

- 2D-1 Timing Optimization by Replacing Flip-Flops to Latches**
K. Yoshikawa, K. Kanamaru, Y. Hagihara, S. Inui, Y. Nakamura (NEC Corp., Japan), T. Yoshimura (Waseda Univ., Japan)
- 2D-2 Enhancing the Performance of Multi-Cycle Path Analysis in an Industrial Setting**
H. Higuchi (Fujitsu Laboratories Ltd, Japan), Y. Matsunaga (Kyushu Univ., Japan)

2D-3 An Approach for Reducing Dynamic Power Consumption in Synchronous Sequential Digital Designs

N. Chabini (Royal Military College of Canada, Canada), W. Wolf (Princeton Univ., USA)

2D-4s Low Power Design Using Dual Threshold Voltage
Y. Ho, T. Hwang (Tsing Hua Univ., Taiwan)

2D-5s Technology Mapping and Packing for Coarse-grained Anti-fuse Based FPGAs
C. Kang, A. Iranli, M. Pedram (Univ. of Southern California, USA)

Wednesday, January 28, 13:30-15:30 Room 419
Session 2E: Effective Test and Diagnosis

Co Chairs: **K. Cheng** – Univ. of California, Santa Barbara, USA
T. Inoue – Hiroshima City Univ., Japan

- 2E-1 Efficient RT-level Fault Diagnosis Methodology**
O. Sinanoglu, A. Orailoglu (UC San Diego, USA)
- 2E-2* Design Diagnosis Using Boolean Satisfiability**
A. Smith, A. Veneris, A. Viglas (Univ. of Toronto, Canada)
- 2E-3 Testable Design of GRM Networks with EXOR Tree for Detecting Stuck-at and Bridging Faults**
H. Rahaman (B.E.College (D.U.), India), D. K. Das (Jadavpur Univ., India), B. B. Bhattacharya (Indian Statistical Inst., India)
- 2E-4s Test Data Compression Technique Using Selective Don't-Care Identification**
T. Hayashi, H. Yoshioka, T. Shinogi, H. Kita, H. Takase (Mie Univ., Japan)
- 2E-5s Re-configurable Embedded Core Test Protocol**
S. Wang, S. T. Chakradhar (NEC Labs., America, USA), K. J. Balakrishnan (Univ. of Texas at Austin, USA)

Wednesday, January 28, 16:00-18:00

Wednesday, January 28, 16:00-18:00 Room 411/412

Session 3A: System-Level Design Methodology

Co Chairs: **V. Mooney** – Georgia Inst. of Tech., USA
D. Araki – Inter Design Technologies, Japan

- 3A-1* Object-Oriented Modeling and Synthesis of SystemC Specifications**
C. Schulz-Key, M. Winterholer, T. Schweizer, T. Kuhn, W. Rosenstiel (Univ. of Tuebingen, Germany)
- 3A-2 Application of UML for Hardware Design Based on Design Process Model**
R. Damasevicius, V. Stuikeys (Kaunas Univ. of Tech., Lithuania)
- 3A-3 A Cosynthesis Algorithm for Application Specific Processors with Heterogeneous Datapaths**
Y. Miyaoka (Waseda Univ., Japan), N. Togawa (The Univ. of Kitakyushu, Japan), M. Yanagisawa, T. Ohtsuki (Waseda Univ., Japan)
- 3A-4 Design Methodology for SoC Architectures Based on Reusable Virtual Cores**
M. Muraoka, H. Nishi, R. K. Morizawa, H. Yokota, H. Hamada (STARC, Japan)

Wednesday, January 28, 16:00-18:00 Room 413

Session 3B: Advanced Design and Modeling Techniques

Co Chairs: **L. Scheffer** – Cadence, USA
F. Minami – Toshiba, Japan

- 3B-1 A Multiple Level Network Approach for Clock Skew Minimization with Process Variations**
M. Mori, H. Chen, B. Yao, C. Cheng (UCSD, USA)
- 3B-2 Layout Techniques for On-Chip Interconnect Inductance Reduction**
S. Tu, J. Jou (National Chiao-Tung Univ., Taiwan), Y. Chang (National Taiwan Univ., Taiwan)
- 3B-3 Piecewise Quadratic Waveform Matching with Successive Chord Iteration**
Z. Wang, J. Zhu (Univ. of Toronto, Canada)
- 3B-4s Optimal Design of High Fan-In Multiplexers via Mixed-Integer Nonlinear Programming**
H. Huang, C. Wang, J. Jou (National Chiao Tung Univ., Taiwan)

3B-5s Adaptive Supply Voltage Technique for Low Swing Interconnects

W. Jeong, B. C. Paul, K. Roy (Purdue Univ., USA)

Wednesday, January 28, 16:00-18:00 Room 414/415

Session 3C: Analog Design and Evaluation

Co Chairs: **S. Kawahito** – Shizuoka Univ., Japan
T. Tsukada – STARC, Japan

- 3C-1 A Large-Current-Output Boosted Voltage Generator with Non-Overlapping Clock Control for Sub-1-V Memory Applications**
K. Min (Kookmin Univ., South Korea), Y. Kim (Changwon National Univ., South Korea), D. Kim, D. Kim (Kookmin Univ., South Korea), J. Ahn (Hynix Semiconductor Inc., South Korea)
- 3C-2 Effects of Noise and Nonlinearity on the Calibration of a Non-Binary Capacitor Array in a Successive Approximation Analog-to-Digital Converter**
J. Gan (Cirrus Logic, Inc., USA), S. Yan, J. Abraham (The Univ. of Texas at Austin, USA)
- 3C-3* Jitter Spectral Extraction for Multi-gigahertz Signal**
C. Ong, D. Hong, K. Cheng, L. -C. Wang (Univ. of California Santa Barbara, USA)
- 3C-4s A 35 dB-Linear Exponential Function Generator for VGA and AGC Applications**
H. Q. Duong (Information and Communication Univ., South Korea)
- 3C-5s A High Efficiency 0.5W BTL Class-D Audio Amplifier with RWDM Technique**
S. C. Li (National Yunlin Univ. of Science and Tech., Taiwan)

Wednesday, January 28, 16:00-18:00 Room 416/417

Session 3D: System Design Verification

Co Chairs: **K. Eguchi** – Aichi Inst. of Tech., Japan
M. Toyonaga – Kochi Univ., Japan

- 3D-1 Efficient Translation of Boolean Formulas to CNF in Formal Verification of Microprocessors**
M. N. Velev (Carnegie Mellon Univ., USA)
- 3D-2 Using Positive Equality to Prove Liveness for Pipelined Microprocessors**
M. N. Velev (Carnegie Mellon Univ., USA)

3D-3 On Deriving Equivalent Architecture Model from System Specification

S. Abdi, D. Gajski (Univ. of California, Irvine, USA)

3D-4 On Compliance Test of On-Chip Bus for SOC

H. Lin, C. Yen, C. Shih, J. Jou (National Chiao Tung Univ., Taiwan)

Wednesday, January 28, 16:00-18:00 Room 419

Session 3E: (Special Session) Panel Discussion: Opportunities with the Open Architecture Test System

Organizers: **K. Hatayama** – Renesas Tech., Japan
R. Rajsuman – Advantest America R&D Center, USA

Moderator: **C. Wu** – National Tsing Hua Univ., Taiwan
Panelists: **R. Rajsuman** – Advantest America R&D Center, USA

Y. Nishimura – Renesas Tech., Japan
S. Chakradhar – NEC Laboratories of America, USA

A. Merschon – Guide Technologies, USA
D. Petrich – Wavecrest, USA
T. Tada – Tokushima Bunri Univ., Japan

Firing Lines: **K. Cheng** – Univ. of California Santa Barbara, USA
Y. Okuda – ITC Asian Subcommittee Member, Sony, Japan

Thursday, January 29, 9:00-10:30

Thursday, January 29, 9:00-10:30 Room 411/412

Session 4A: (Special Session) C-Based Design Examples

Chair: **H. Yasuura** – Kyushu Univ., Japan

- 4A-1 (Embedded Invited Talk): C-based Behavioral Synthesis and Verification Analysis on Industrial Design Examples**
K. Wakabayashi (NEC, Japan)
- 4A-2 (Embedded Invited Talk): Using C Based Logic Synthesis to Bridge the Productivity Gap**
C. Sullivan, A. Wilson, S. Chappell (Celoxica Ltd, England, UK)

Thursday, January 29, 9:00-10:30 Room 413
Session 4B: Buffered Tree Construction

Co Chairs: **C. Koh** – Purdue Univ., USA
T. Okamoto – NEC, Japan

- 4B-1 A Place and Route Aware Buffered Steiner Tree Construction**
C. Sze, J. Hu (Texas A&M Univ., USA), C. J. Alpert (IBM Austin Research Laboratory, USA)
- 4B-2 An Efficient Routing Tree Construction Algorithm with Buffer Insertion, Wire Sizing and Obstacle Considerations**
S. Dechu (Micron, Inc., USA), Z. C. Shen, C. Chu (Iowa State Univ., USA)
- 4B-3 Modeling of Coplanar Waveguide for Buffered Clock Tree**
J. Chen, L. He (Univ. of California, Los Angeles, USA)

Thursday, January 29, 9:00-10:30 Room 414/415
Session 4C: Power-Aware Approach for Microprocessor Design

Co Chairs: **C. Wu** – National Tsing Hua Univ., Taiwan
T. Miyamori – Toshiba, Japan

- 4C-1 Decode Filter Cache for Energy Efficient Instruction Cache Hierarchy in Super Scalar Architectures**
K. Vivekanandarajah, T. Srikanthan, S. Bhatlacharya (Nanyang Technological Univ., Singapore)
- 4C-2s* Mixed-Clock Issue Queue Design for Energy Aware, High-Performance Cores**
V. S. Rapaka (Mentor Graphics Corp., USA), E. Talpes, D. Marculescu (Carnegie Mellon Univ., USA)
- 4C-3s Power-Performance Trade-off Using Pipeline Delays**
G. Surendra, S. Banerjee, S. Nandy (Indian Inst. of Science, India)
- 4C-4s Exploiting Program Execution Phases to Trade Power and Performance for Media Workload**
S. Banerjee, G. Surendra, S. K. Nandy (Indian Inst. of Science, India)
- 4C-5s* LPRAM: A Low Power RAM Design with Testability**
D. K. Pradhan (Univ. of Bristol, England, UK)

Thursday, January 29, 9:00-10:30 Room 416/417
Session 4D: Analog Layout Techniques

Co Chairs: **J. Roychowdhury** – Univ. of Minnesota, USA
H. Onodera – Kyoto Univ., Japan

- 4D-1 Multiple Specifications Radio-Frequency Integrated Circuit Design with Automatic Template-Driven Layout Retargeting**
N. Jangkrarjng, S. Bhattacharya, R. Hartono, C. Shi (Univ. of Washington, USA)
- 4D-2 Hierarchical Extraction and Verification of Symmetry Constraints for Analog Layout Automation**
S. Bhattacharya, N. Jangkrarjng, R. Hartono, R. Shi (Univ. of Washington, USA)
- 4D-3 Multi-Level Placement with Circuit Schema Based Clustering in Analog IC Layouts**
T. Nojima, X. Zhu (SII EDA Technologies Inc., Japan), Y. Takashima, S. Nakatake, Y. Kajitani (The Univ. of Kitakyushu, Japan)

Thursday, January 29, 10:45-12:15

Thursday, January 29, 10:45-12:15 Room 411/412
Session 5A: Formal Verification

Co Chairs: **F. Tao** – Univ. of California, Santa Barbara, USA
K. Takagi – Nagoya Univ., Japan

- 5A-1 Model Checking on State Transition Diagram**
B. Das, D. Sarkar (CSE Deptt., IIT Kharagpur, 721302, India, India), S. Chattopadhyay (CSE Deptt., IIT Guwahati, India, India)
- 5A-2 Efficient Reachability Checking Using Sequential SAT**
G. Parthasarathy, M. K. Iyer, K. Cheng, L. C. Wang (UC-Santa Barbara, USA)
- 5A-3 Exploiting State Encoding for Invariant Generation in Induction-based Property Checking**
M. Wedler, D. Stoffel, W. Kunz (Univ. of Kaiserslautern, Germany)

Thursday, January 29, 10:45-12:15 Room 413
Session 5B: Routing Methodology

Co Chairs: **T. Kim** – KAIST, Korea
S. Saika – Matsushita Electric Industrial Co.,Ltd., Japan

- 5B-1s Tradeoff Routing Resource, Runtime and Quality in Buffered Routing**
X. Tang (Cadence, USA), M. Wong (Univ. of Illinois, USA)
- 5B-2s* Practical Methodology of Post-layout Gate Sizing for 15 % More Power Saving**
N. Miura (Keio Univ., Japan), N. Kato (Hitachi, Ltd., Japan), T. Kuroda (Keio Univ., Japan)
- 5B-3 Interconnect Design Methods for Memory Design**
C. Hwang, M. Pedram (Univ. of Southern California, USA)
- 5B-4 Optimal Planning for Mesh-Based Power Distribution**
C. Cheng, H. Chen, A. B. Kahng (UCSD, USA), M. Mori (Fujitsu Limited, Japan), Q. Wang (UCSD, USA)

Thursday, January 29, 10:45-12:15 Room 414/415
Session 5C: Exploration for Advanced SoC Design

Co Chairs: **S. Lee** – Soongsil Univ., Korea
H. Okuhata – Synthesis Corp., Japan

- 5C-1 2.5D System Integration: A Design Driven System Implementation Schema**
Y. Deng, W. Maly (Carnegie Mellon Univ., USA)
- 5C-2 Canceled**
- 5C-3s An HMAC Processor with Integrated SHA-1 and MD5 Algorithms**
M. Wang, C. Su, C. Huang, C. Wu (National Tsing Hua Univ., Taiwan)
- 5C-4s Design Methodology for IRA Codes**
F. Kienle, N. Wehn (Univ. of Kaiserslautern, Germany)

Thursday, January 29, 10:45-12:15 Room 416/417

Session 5D: Embedded Software

Co Chairs: **P. Chou** – Univ. of California, Irvine, USA
A. Fukuda – Kyushu Univ., Japan

5D-1 Embedded Software Generation from System Level Design Languages

H. Yu, R. Doemer, D. Gajski (UC Irvine, USA)

5D-2 Fast and Accurate Timed Execution of High Level Embedded Software Using HW/SW Interface Simulation Model

A. Bouchhima, S. Yoo, A. A. Jerraya (TIMA Laboratory, France)

5D-3s* Energy Efficient Code Generation Exploiting Reduced Bit-width Instruction Set Architectures (rISA)

A. Shrivastava, N. Dutt (Univ. of California, Irvine, USA)

5D-4s Memory Access Driven Storage Assignment for Variables in Embedded System Design

Y. Choi, T. Kim (KAIST, South Korea)

Thursday, January 29, 13:30-15:30

Thursday, January 29, 13:30-15:30 Room 411/412

Session 6A: (Special Session) RF Modeling and Design Methodology

Chair: **S. Moriyama** – Innotech Corp., Japan

6A-1 (Embedded Tutorial): MOSFET Modeling for RF-CMOS Design

M. Miura-Mattausch (Hiroshima Univ., Japan)

6A-2 (Embedded Tutorial): RF Design Methodologies Bridging System-IC-Module Design

R. A. Mullen (Cadence Design Systems, Inc., USA)

Thursday, January 29, 13:30-15:30 Room 413

Session 6B: Power Grid Analysis and Design

Co Chairs: **C. Chen** – National Taiwan Univ., Taiwan
M. Yamada – Toshiba Microelectronics, Japan

6B-1* Hierarchical Random-walk Algorithms for Power Grid Analysis

H. Qian, S. S. Sapatnekar (Univ. of Minnesota, USA)

6B-2 A Fast Decoupling Capacitor Budgeting Algorithm for Robust On-Chip Power Delivery

J. Fu, Z. Luo, X. Hong, Y. Cai (Tsinghua Univ., China), S. Tan (UC Riverside, USA), Z. Pan (Tsinghua Univ., China)

6B-3* Large-scale Linear Circuit Simulation with an Inversed Inductance Matrix

C. Mizuta, J. Iwai, K. Machida (Mathematical Systems Inc., Japan), T. Kage, H. Masuda (STARC, Japan)

6B-4 DEPOGIT: Dense Power-Ground Interconnect Architecture for Physical Design Integrity

A. Kurokawa (STARC, Japan), N. Ono (SII Technologies, Japan), T. Kage, H. Masuda (STARC, Japan)

Thursday, January 29, 13:30-15:30 Room 414/415

Session 6C: (Special Session) University Design Contest

Co Chairs: **X. Zeng** – Fudan Univ., China
M. Ikeda – Univ. of Tokyo, Japan

6C-1 Design of Real-Time VGA 3-D Image Sensor Using Mixed-Signal Techniques

Y. Oike, M. Ikeda, K. Asada (Univ. of Tokyo, Japan)

6C-2 A Bandwidth and Memory Efficient MPEG-4 Shape Encoder

K. Lee, N. Y. Chang, H. Chin, H. Hsu, C. Jen (National Chiao Tung Univ., Taiwan)

6C-3 A Sub-mW MPEG-4 Motion Estimation Processor Core for Mobile Video Application

Y. Kuroda, J. Miyakoshi, M. Miyama, K. Imamura, H. Hashimoto, M. Yoshimoto (Kanazawa Univ., Japan)

6C-4 Analog LSI for Motion Detection of Approaching Object with Simple-Shape Recognition Based on Lower Animal Vision

K. Nishio, H. Yonezu, S. Sawa, Y. Furukawa (Toyoashi Univ. of Tech., Japan)

6C-5 350nm CMOS Test-Chip for Architecture Verification of Real-Time QVGA Color-Video Segmentation at the 90nm Technology Node

T. Morimoto, Y. Harada, T. Koide, H. J. Mattausch (Hiroshima Univ., Japan)

6C-6 A Low-Power Graphics LSI Integrating 29Mb Embedded DRAM for Mobile Multimedia Applications

R. Woo, S. Choi, J. Sohn, S. Song, Y. Bae, H. Yoo (KAIST, South Korea)

6C-7 A High Efficiency 0.5W BTL Class-D Audio Amplifier with RWDM Technique

S. C. Li (National Yunlin Univ. of Science and Tech., Taiwan)

6C-8 A Small-Area High-Performance 512-Point 2-Dimensional FFT Single-Chip Processor

N. Miyamoto, L. Karnan (Tohoku Univ., Japan), K. Maruo (Advantest Laboratories Ltd., Japan), K. Kotani, T. Ohmi (Tohoku Univ., Japan)

6C-9 Fast Adaptive DC-DC Conversion Using Dual-Loop One-Cycle Control in Standard Digital CMOS Process

D. Ma, W. Ki, C. Tsui (HKUST, Hong Kong)

6C-10 A Dual-band Image-reject Mixer for GPS with 64dB Image Rejection

Y. Utsurogi, M. Haruoka, T. Matsuoka, K. Taniguchi (Osaka Univ., Japan)

6C-11 Associative Memory with Fully Parallel Nearest-Manhattan-Distance Search for Low-Power Real-Time Single-Chip Applications

Y. Yano, T. Koide, H. Mattausch (Hiroshima Univ., Japan)

6C-12 A Performance Comparison of PLLs for Clock Generation Using Ring Oscillator VCO and LC Oscillator in a Digital CMOS Process

T. Miyazaki, M. Hashimoto, H. Onodera (Kyoto Univ., Japan)

6C-13 A Reliable Low-Power Fast Skew-Compensation Circuit

Y. Wang, J. Wang (Chung-Cheng Univ., Taiwan)

6C-14 A Retinal Prosthetic Device Using a Pulse-frequency-modulation CMOS Image Sensor

J. Ohta, T. Furumiya, D. C. Ng, A. Uehara, K. Kagawa, T. Tokuda, M. Nunoshita (NAIST, Japan)

6C-15 Compact 12-Port Multi-Bank Register File Test-Chip in 0.35 μ m CMOS for Highly Parallel Processors

T. Sueyoshi, H. Uchida (Hiroshima Univ., Japan), Y. Mitani (Hiroshima City Univ., Japan), H. J. Mat-tausch, T. Koide (Hiroshima Univ., Japan), T. Hiron-aka (Hiroshima City Univ., Japan)

6C-16 A Low Power Asynchronous Java Processor for Contactless Smart Card

C. Yu, C. Choy (The Chinese Univ. of Hong Kong, Hong Kong), H. Min (Fudan Univ., China), C. Chan, K. Pun (The Chinese Univ. of Hong Kong, Hong Kong)

6C-17 An Image-sensor-based Optical Receiver Fabricated in a Standard 0.35- μ m CMOS Technology for Free-space Optical Communications

K. Kagawa, T. Kawakami, H. Asazu, T. Ikeuchi, A. Fu-jiuchi, J. Ohta, M. Nunoshita (NAIST, Japan)

6C-18 The Flexible Processor - An Approach for Single-Chip Hardware Emulation by Dynamic Reconfiguration

T. Ohkawa, T. Nozawa, M. Fujibayashi, N. Miyamoto, L. Karnan, S. Kita, K. Kotani, T. Ohmi (Tohoku Univ., Japan)

6C-19 A VDD and Temperature Independent CMOS Voltage Reference Circuit

T. Matsuda, R. Minami, A. Kanamori, H. Iwata (Toyama Prefectural Univ., Japan), T. Ohzone (Okayama Prefectural Univ., Japan), S. Yamamoto, T. Ihara, S. Nakajima (Shikino Hightech Co., Ltd., Japan)

6C-20 A Dual Band Switching Digital Controller for a Buck Converter

Y. M. Chui, W. Ki, C. Tsui (The Hong Kong Univ. of Science and Tech., Hong Kong)

6C-21 Golay and Wavelet Error Control Codes in VLSI

A. Balasundaram, A. Pereira, J. Park, V. J. Mooney III (Georgia Inst. of Tech., USA)

6C-22 Timing Measurement Unit with Multi-Stage TVC for Embedded Memories

K. J. Mo, S. S. Yang, T. Y. Chang (National Tsing Hua Univ., Taiwan)

6C-23 Development of a Waveform Sampling Front-End ASIC for PET

J. Yeom, T. Ishitsu, H. Takahashi (Univ. of Tokyo, Japan)

6C-24 A Dynamic Element Matching Circuit for Multi-bit Delta-Sigma Modulators

R. Katoh, S. Kobayashi, T. Waho (Sophia Univ., Japan)

6C-25 Design of POP11 (PDP-11 on Programmable Chip)

Y. Iida, N. Shimizu (Tokai Univ., Japan)

6C-26 A Closed Caption TV Microcontroller

E. Leelarasmee (Chulalongkorn Univ., Thailand), K. Pengwon (Chiang Mai Univ., Thailand)

6C-27 Improvement of Saturation Characteristics of a Frequency-demodulation CMOS Image Sensor

J. Ohta, K. Yamamoto, Y. Oya, K. Kagawa, T. Tokuda, M. Nunoshita (NAIST, Japan), K. Watanabe (Mi-crosignal Co. Ltd., Japan)

6C-28 Design and Implementation of a Secret Key Steganographic Micro-Architecture Employing FPGA

M. M. Saeb, H. A. Abdul Moneim (Arab Academy for Science, Tech. and Maritime Transport, Egypt)

Thursday, January 29, 13:30-15:30 Room 416/417
Session 6D: Novel Techniques in Logic Synthesis

Co Chairs: **R. Drechsler** – Univ. of Bremen, Germany
H. Higuchi – Fujitsu Labs., Japan

6D-1 Preserving Synchronizing Sequences of Sequential Circuits After Retiming

M. Mneimneh, K. Sakallah (Univ. of Michigan, USA), J. Moondanos (Intel Corp., USA)

6D-2 A Fast Method to Derive Minimum SOPs for Decomposable Functions

T. Sasao (Kyushu Inst. of Tech., Japan), J. T. Butler (Naval Postgraduate School, USA)

6D-3 Efficient Computation of Canonical Form for Boolean Matching in Large Libraries

D. Debnath (Oakland Univ., USA), T. Sasao (Kyushu Inst. of Tech., Japan)

6D-4s Disjoint-Support Boolean Decomposition Combining Functional and Structural Methods

A. Martinelli, R. Krenz, E. Dubrova (KTH, Sweden)

6D-5s Transduction Method for Design of Logic Cell Structure

K. Tanaka, Y. Kambayashi (Kyoto Univ., Japan)

Thursday, January 29, 16:30-18:00

Thursday, January 29, 16:30-18:00 Room 411/412
Session 7A: (Special Session) Future of ITS Technologies in the Ubiquitous Society

Chair: **M. Imai** – Osaka Univ., Japan

7A-1 (Invited Talk): The Integration of Vehicles Into a Ubiquitous Computing Environment –Computing and Networking Technologies for Vehicles–
N. Tokitsu (Internet ITS Consortium, Japan)

Thursday, January 29, 16:30-18:00 Room 413
Session 7B: Buffer Planning

Co Chairs: **J. Hu** – Texas A&M Univ., USA
S. Wakabayashi – Hiroshima City Univ., Japan

7B-1 Complexity Analysis and Speedup Techniques for Optimal Buffer Insertion with Minimum Cost
W. Shi, Z. Li (Texas A&M Univ., USA), C. J. Alpert (IBM Corp., USA)

7B-2 A Buffer Planning Algorithm with Congestion Optimization
S. Chen (Tsinghua Univ., China), X. Hong (Tinghua Univ., China), S. Dong, Y. Ma, Y. Cai (Tsinghua Univ., China), C. Cheng (UCSD, USA), J. Gu (Science and Tech. Univ. of HongKong, Hong Kong)

7B-3s Buffer Allocation Algorithm with Consideration of Routing Congestion
Y. Ma, X. Hong, S. Dong, S. Chen, Y. Cai (Tsinghua Univ., China), C. Cheng (UCSD, USA), J. Gu (Science and Tech. Univ. of HongKong, Hong Kong)

7B-4s Integrating Buffer Planning with Floorplanning for Simultaneous Multi-objective Optimization
Y. Cheng (Synopsis, Taiwan), Y. Chang (National Tai-wan Univ., Taiwan)

Thursday, January 29, 16:30-18:00 Room 414/415

Session 7C: Design Verification and Simulation

Co Chairs: **S. Abdi** – Univ. of California, Irvine, USA
G. Suzuki – The Univ. of Kitakyushu, Japan

7C-1* Verification of Timed Circuits with Symbolic Delays

R. Clariso, J. Cortadella (Universitat Politècnica De Catalunya, Spain)

7C-2 Improved Symbolic Simulation by Functional-Space Decomposition

F. Tao, L. Wang, K. Cheng (UC-Santa Barbara, USA)

7C-3s* Improving Simulation-Based Verification by Means of Formal Methods

G. Fey, R. Drechsler (Univ. of Bremen, Germany)

7C-4s Parallel Verilog Simulation: Architecture and Circuit Partition

T. Li, Y. Guo, S. Li, F. Ao, G. Liu (National Univ. of Defense Tech., China)

Thursday, January 29, 16:30-18:00 Room 416/417

Session 7D: Task Scheduling with DVS

Co Chairs: **R. Marculescu** – Carnegie Mellon Univ., USA
Y. Nakamoto – NEC, Japan

7D-1 Minimizing Energy Consumption of Multiple-Processor-Core Systems with Simultaneous Task Allocation, Scheduling and Voltage Assignment

L. Leung, C. Tsui, W. Ki (The Hong Kong Univ. of Science and Tech., Hong Kong)

7D-2 Dynamic Voltage Scaling of Periodic and Aperiodic Tasks in Priority-Driven Systems

D. Shin, J. Kim (Seoul National Univ., South Korea)

7D-3s Fast and Efficient Voltage Scheduling by Evolutionary Slack Distribution

B. Gorji-ara, P. Chou, N. Bagherzade, M. Reshadi (Univ. of California, Irvine, USA), D. Jensen (Rockwell Collins Inc., USA)

7D-4s Minimizing Energy Consumption of Hard Real-Time Systems with Simultaneous Tasks Scheduling and Voltage Assignment Using Statistical Data

L. Leung, C. Tsui, W. Ki (The Hong Kong Univ. of Science and Tech., Hong Kong)

Friday, January 30, 9:00-10:00

Friday, January 30, 9:00-10:00 Small Auditorium

Keynote Address II:

System Level Design Technology for Realizing an Ambient Intelligent Environment

Dr. Rudy Lauwereins - Vice President, IMEC, Belgium

Friday, January 30, 10:15-12:15

Friday, January 30, 10:15-12:15 Room 411/412

Session 8A: Global Routing

Co Chairs: **C. Cheng** – Univ. of California, San Diego, USA

T. Shibuya – Fujitsu Lab. Ltd., Japan

8A-1 A Fast Congestion Estimator for Routing with Bounded Detours

L. Cheng (Univ. of Colorado at Boulder, USA), X. Song, G. Yang, Z. Tang (Portland State Univ., USA)

8A-2 Accurate and Efficient Flow Based Congestion Estimation in Floorplanning

Z. C. Shen, C. Chu (Iowa State Univ., USA)

8A-3 A Coupling and Crosstalk Considered Timing-Driven Global Routing Algorithm for High Performance Circuit Design

J. Xu, X. Hong, T. Jing, L. Zhang (Tsinghua Univ., China), J. Gu (Hong Kong Univ. of Science and Tech., Hong Kong)

8A-4s Timing-Constrained Congestion-Driven Global Routing

J. Yan, S. Lin (Chung-Hua Univ., Taiwan)

8A-5s Efficient Octilinear Steiner Tree Construction Based on Spanning Graphs

Q. Zhu (Tsinghua Univ., China), H. Zhou (Northwestern Univ., USA), T. Jing, X. Hong, Y. Yang (Tsinghua Univ., China)

Friday, January 30, 10:15-12:15 Room 413

Session 8B: Interconnect and ESD Extraction

Co Chairs: **A. Wang** – Illinois Inst. of Tech., USA
K. Nishi – Kinki Univ. Technical College, Japan

8B-1* Representative Frequency for Interconnect R(f)L(f)C Extraction

A. Tsuchiya, M. Hashimoto, H. Onodera (Kyoto Univ., Japan)

8B-2 A Mixed-mode Extraction Flow for High Performance Microprocessors

T. Jiang, E. Pettus, D. Leither (Motorola Inc., USA)

8B-3 An Efficient Method MEGCR for Solving Systems with Multiple Right-hand Sides in 3-D Parasitic Inductance Extraction

L. Yang, X. Guo, Z. Wang (Tsinghua Univ., China)

8B-4s Fast and Accurate Extraction of 3-D Interconnect Resistance: Improved Quasi-Multiple Medium Accelerated BEM Method

X. Wang (Tsinghua Univ. Beijing, China), D. Liu (UCSC, USA), W. Yu, Z. Wang (Tsinghua Univ. Beijing, China)

8B-5s Concept and Extraction Method of ESD-critical Parameters for Function-Based Layout Level ESD Protection Circuit Design Verification

R. Zhan, H. Feng, Q. Wu, X. Guan, G. Chen, H. Xie, A. Wang (Illinois Inst. of Tech., USA)

Friday, January 30, 10:15-12:15 Room 414/415

Session 8C: Reconfigurable Systems

Co Chairs: **Y. Chang** – National Taiwan Univ., Taiwan
N. Kajihara – NEC, Japan

8C-1 Interconnect Capacitance Estimation for FPGAs

J. H. Anderson, F. N. Najm (Univ. of Toronto, Canada)

8C-2 Area-Minimal Algorithm for LUT-Based FPGA Technology Mapping with Duplication-free Restriction

C. Kao (National Pingtung Inst. of Commerce, Taiwan), Y. Lai (National Cheng Kung Univ., Taiwan)

8C-3 Temporal Floorplanning Using 3D-subTCG

P. Yuh, C. Yang, Y. Chang (National Taiwan Univ., Taiwan), H. Chen (Etron Tech. Inc., Taiwan)

8C-4s ReCSiP: a Reconfigurable Cell Simulation Platform

Y. Osana, T. Fukushima, H. Amano (Keio Univ., Japan)

8C-5s SmartGlue: An Interface Controller with Auto Reconfiguration for Field Programmable Computing Machine

Y. Kim (KAIST, South Korea), B. Park (Dynamith Systems, South Korea), J. Lee, C. Kyung (KAIST, South Korea)

Friday, January 30, 10:15-12:15 Room 416/417

Session 8D: HW/SW Co-Design

Co Chairs: **R. Marculescu** – Carnegie Mellon Univ., USA
N. Ishiura – Kwansei Univ., Japan

8D-1 An SoC Architecture and Its Design Methodology Using Unifunctional Heterogeneous Processor Array

Y. Yuyama, M. Aramoto (Kyoto Univ., Japan), K. Kobayashi (Univ. of Tokyo, Japan), H. Onodera (Kyoto Univ., Japan)

8D-2 Instruction Set and Functional Unit Synthesis for SIMD Processor Cores

N. Togawa (Univ. of Kitakyushu, Japan), K. Tachikake, Y. Miyaoka, M. Yanagisawa, T. Ohtsuki (Waseda Univ., Japan)

8D-3 A High Performance Bus Communication Architecture through Bus Splitting

R. Lu, C. Koh (Purdue Univ., USA)

8D-4s Automatic Generation of Bus Functional Models from Transaction Level Models

D. Shin, S. Abdi, D. Gajski (Univ. of California, Irvine, USA)

8D-5s A Global Bus Power Optimization Methodology for Physical Design of Memory Dominated Systems by Coupling Bus Segmentation and Activity Driven Block Placement

H. Wang (IMEC/Katholieke Universiteit Leuven, Belgium), A. Papanikolaou, M. Miranda (IMEC, Belgium), F. Catthoor (IMEC/Katholieke Universiteit Leuven, Belgium)

Friday, January 30, 13:30-15:30

Friday, January 30, 13:30-15:30 Room 411/412

Session 9A: (Special Session) DFM in nm-Process Generation

Co Chairs: **H. Masuda** – STARC, Japan
K. Yoshida – Cadence, Japan

9A-1 (Embedded Tutorial): Toward Stochastic Design for Digital Circuits – Statistical Static Timing Analysis –

S. Tsukiyama (Chuo Univ., Japan)

9A-2 (Embedded Tutorial): Physical CAD Changes to Incorporate Design for Lithography and Manufacturability

L. Scheffer (Cadence Design System, USA)

9A-3 (Embedded Tutorial): Design-Manufacturing Interface for .13 um and Below

A. J. Strojwas (CCMU and PDF Solutions, USA)

Friday, January 30, 13:30-15:30 Room 413

Session 9B: Advanced Interconnect Analysis

Co Chairs: **L. He** – Univ. of California, Los Angeles, USA
T. Sato – Renesas Tech. Corp., Japan

9B-1 Parametric Reduced Ordering Modeling for Interconnect Analysis

G. Shi, C. R. Shi (Univ. of Washington, USA)

9B-2 Realizable Parasitic Reduction for Distributed Interconnects Using Matrix Pencil Technique

J. Wang, O. Hafiz (Univ. of Arizona, USA)

9B-3 Spice Compatible Circuit Models for Partial Reluctance K

H. Ji (Univ. of California, Santa Cruz, USA), Q. Yu (Cadence Design Systems, Inc., USA), W. W. Dai (Univ. of California, Santa Cruz, USA)

9B-4 Frequency-Dependent Reluctance Extraction

C. Luk, T. Chen (Univ. of Wisconsin-Madison, USA), C. Chen (National Taiwan Univ., Taiwan)

Friday, January 30, 13:30-15:30 Room 414/415
Session 9C: (Special Session) Panel Discussion: Future Reconfigurable Computing System

Organizers: **M. Kawamura** – Toshiba, Japan
H. Amano – Keio Univ., Japan
Moderator: **S. Goto** – Waseda Univ., Japan
Panelists: **M. Motomura** – NEC, Japan
T. Sato – IP Flex, Japan
S. Trimberger – Xilinx, USA
B. Plunkett – Quick Silver, USA
R. Lauwereins – IMEC, Belgium

Friday, January 30, 13:30-15:30 Room 416/417
Session 9D: System-Level Architecture

Co Chairs: **A. Orailoglu** – Univ. of California, San Diego, USA
S. Chakradhar – NEC Labs. America, USA

- 9D-1 Enabling On-Chip Diversity through Architectural Communication Design**
T. Dumitras, S. Kerner, R. Marculescu (Carnegie Mellon Univ, USA)
- 9D-2 Bandwidth Tracing Arbitration Algorithm for Mixed-Clock SoC with Dynamic Priority Adaptation**
Y. Kwon, J. Lee, C. Kyung (KAIST, South Korea)
- 9D-3 A Novel Memory Size Model for Variable-Mapping in System Level Design**
L. Cai, H. Yu, D. Gajski (Univ. of California, Irvine, USA)
- 9D-4* A Compressed Frame Buffer to Reduce Display Power Consumption in Mobile Systems**
H. Shim, N. Chang (Seoul National Univ., South Korea), M. Pedram (Univ. of Southern California, USA)

Friday, January 30, 16:30-18:00

Friday, January 30, 16:30-18:00 Room 411/412
Session 10A: Embedded System Architectures

Co Chairs: **N. Chang** – Seoul National Univ., Korea
A. Inoue – Matsushita Electric Industrial Co., Ltd., Japan

10A-1 Instruction Buffering Exploration for Low Energy VLIWs with Instruction Clusters

T. Vander Aa, M. Jayapala, F. Barat, G. Deconinck (K. U. Leuven, Belgium), R. Lauwereins, F. Catthoor (IMEC, Belgium), H. Corporaal (TU Eindhoven, Netherlands)

10A-2s* A Static and Dynamic Energy Reduction Technique for I-Cache and BTB in Embedded Processors

H. Sato (Kyushu Inst. of Tech., Japan), T. Sato (Japan Science and Tech. Agency, Japan)

10A-3s Resource-Constrained Low-Power Bus Encoding with Crosstalk Delay Elimination

M. Cha, C. Lyuh, T. Kim (KAIST, South Korea)

10A-4s* Compiler Based Exploration of DSP Energy Savings by SIMD Operations

M. Lorenz, P. Marwedel (Univ. of Dortmund, Germany), T. Draeger, G. P. Fettweis (TU Dresden, Germany), R. Leupers (RWTH Aachen, Germany)

10A-5s* Synthesizable HDL Generation Method for Configurable VLIW Processors

Y. Kobayashi, S. Kobayashi, K. Okuda, K. Sakanushi, Y. Takeuchi, M. Imai (Osaka Univ., Japan)

Friday, January 30, 16:30-18:00 Room 413
Session 10B: Crosstalk Noise Analysis

Chair: **M. Hashimoto** – Kyoto Univ., Japan

10B-1 A Non-iterative Model for Switching Window Computation with Crosstalk Noise

J. Wang, O. Hafiz (Univ. of Arizona, USA)

10B-2 Gate Delay Calculation Considering the Crosstalk Capacitances

S. Abbaspour, M. Pedram (Univ. of Southern California, USA)

10B-3 A Simplified Transmission-Line Based Crosstalk Noise Model for On-Chip RLC Wiring

K. B. Agarwal, D. Sylvester, D. Blaauw (Univ. of Michigan, USA)

Friday, January 30, 16:30-18:00 Room 414/415
Session 10C: Expressions for Boolean Functions

Co Chairs: **M. N. Velev** – Carnegie Mellon Univ., USA
M. Muraoka – STARC, Japan

10C-1* Minimization of the Expected Path Length in BDDs Based on Local Changes

R. Ebdendt (Univ. of Bremen, Germany), W. Guenther (Infineon Technologies, Germany), R. Drechsler (Univ. of Bremen, Germany)

10C-2s* Minimization of Memory Size for Heterogeneous MDDs

S. Nagayama, T. Sasao (Kyushu Inst. of Tech., Japan)

10C-3s* Combining Ordered Best-First Search with Branch and Bound for Exact BDD Minimization

R. Ebdendt (Univ. of Bremen, Germany), W. Guenther (Infineon Technologies, Germany), R. Drechsler (Univ. of Bremen, Germany)

10C-4s Satisfiability and Integer Programming as Complementary Tools

R. Li, D. Zhou (Univer of Texas at Dallas, USA), D. Du (Univ. of New Brunswick, Canada)

10C-5s ShatterPB: Symmetry-Breaking for Pseudo-Boolean Formulas

F. A. Aloul (American Univ. in Dubai, United Arab Em), A. Ramani, I. L. Markov, K. A. Sakallah (Univ. of Michigan, USA)

Friday, January 30, 16:30-18:00 Room 416/417
Session 10D: Semi-Custom Techniques in System Design

Co Chairs: **W. Dai** – Univ. of California, Santa Cruz, USA
K. Suzuki – NEC, Japan

10D-1 Automatic Process Migration of Datapath Hard IP Libraries

F. Fang, J. Zhu (Univ. of Toronto, Canada)

10D-2 Priority Assignment Optimization for Minimization of Current Surge in High Performance Power Efficient Clock-gated Microprocessor

Y. Chen, K. Roy, C. Koh (Purdue University, USA)

10D-3 High-Level Area and Power-up Current Estimation Considering Rich Cell Library

F. Li, L. He (Univ. of California, Los Angeles, USA)

Tutorials

Tutorial 1 (FULL DAY)

Tuesday, January 27, 9:00-17:00 Room 411+412

Recent Advances and Future Challenges in Design Verification

Organizer: *D. Pradhan* – Univ. of Bristol, UK

Speakers: *D. Pradhan* – Univ. of Bristol

M. Abadir – Motorola

R. Drechsler – Univ. of Bremen

Design flow, RTL-verification, Simulation-based techniques, basic concepts of equivalence checking, combinatorial equivalence checking, ATPG-based techniques, compare point matching, mitering, don't cares, solver overview (structural verification, BDD-based solvers, SAT-based solvers), Decision Diagrams (BDDs, zBDDs, word-level DDs). Also to be covered are Concepts in SAT solvers (backtrack-search algorithm, effective techniques, including non-chronological backtracking & Boolean constraint propagation), new EDA-related techniques (covering immediate implications, partial-clauses, local decisions & partial clauses). Finally, the Tutorial will give an overview of various commercially available tools, & their applicability. Also to be discussed are future challenges, such as design for verifiability & potential new directions. Intended Audience: Practicing engineers, users, & academics, interested in the basic principles & current state-of-the-art. Tutorial Summary: Providing an overview of recent developments as well as basic principles of equivalence checking, SAT-Solvers and verification. Also to provide perspective of practical industrial experiences in the use and development of the tools.

Tutorial 2 (FULL DAY)

Tuesday, January 27, 9:00-17:00 Room 413

Design and Runtime Techniques for Leakage Control and Minimization of CMOS VLSI Circuits in Active and Sleep Modes

Organizer: *M. Pedram*, – USC

Speakers: *F. Fallah* – FLA, Fujitsu

M. Pedram – USC

In many new designs, the leakage component of power consumption is comparable to the dynamic component. Many reports indicate that 50% or even higher percentage of the total power consumption is due to the leakage of transis-

tors and this percentage will increase with technology scaling unless effective techniques are used to bring leakage under control. This tutorial will focus on circuit techniques and design methods to accomplish this goal.

We will start the tutorial by describing the main sources of leakage in CMOS VLSI circuits and how these sources will scale with technology scaling. Next we will review a number of leakage current scenarios (ACTIVE and SLEEP mode), types of leakage control solutions (DESIGN vs. RUNTIME based solutions) and expected performance impacts. We will then present a few examples of DESIGN-based techniques for subthreshold leakage control. More precisely, we will explain how technology mapping can be modified to reduce the leakage through concurrent assignment of threshold voltages and transistor sizes as well as library cell selection. We will then describe a precomputation-based guarding technique, which reduces both the leakage and dynamic power and show the tool flow that may be used for applying it to an industrial VLIW processor. We will show how the low leakage of combinational gates, Flip Flops and bus drivers found in ASIC cell libraries can be reduced through circuit design and layout optimization techniques. The tutorial will be continued by presenting RUNTIME mechanisms for subthreshold leakage control. More specifically, we will talk about forward and backward biasing techniques and the transistor stacking technique. We will next present an algorithm for finding the minimum leakage vector of a circuit and show how the results can be improved by adding more controllability to a given circuit. One advantage of this method is that it can be applied to a sequential circuit without any delay overhead. We will also describe proven techniques for power gating and how to avoid potential power plane integrity problems. Finally, we will show how the gate-tunneling leakage can be reduced by using high threshold, thick-oxide sleep transistors. Another method for reducing the gate-tunneling leakage is using dual oxide technology. This method is analogous to the dual threshold technique for reducing the sub-threshold leakage. We will discuss how this method can be combined with the dual threshold technique to reduce both sub-threshold and gate-tunneling leakage.

Tutorial 3 (FULL DAY)

Tuesday, January 27, 9:00-17:00 Room 414+415

System-Level Design Methodology for SoC Design

Organizer: *D. Gajski* – UCI

Speakers: *M. Fujita* – Univ. of Tokyo

D. Gajski – UCI

T. Hasegawa – Fujitsu Ltd.

T. Imai – Renesas Technology.

This tutorial will cover basic concepts in system-level design, the design tasks, system-level (transaction-based) modeling, modeling languages, system-level synthesis and verification, and design methodology from specification to cycle-accurate design for systems on board, chip or embedded. Several speakers will define general design methodology, major issues in specification, synthesis and verification, and use of system-level methodology in different applications. The tutorial not only gives basic concepts present and future system-level design methodologies, but also presents and discusses a couple of real industrial design methodologies.

Speakers will be from academia and industry covering both theoretical and practical issues on the design methodology.

Target audience: System-level or SoC designers, system and application SW engineers, IP and HW engineers, system managers, CAD developers and CAD researchers.

Table of content:

1. System-level methodology and design flow
2. Transaction-level modeling and synthesis
3. System-level languages and verification
4. System-level tools
5. Methodology examples
6. Product applications

Tutorial 4.1 (HALF DAY)

Tuesday, January 27, 9:00-12:00 Room 416+417

Low Power Design Techniques and Tools

Organizer: *S. Chattoapdhyay* – Intel Corp.

Speakers: *Subhomoy Chattoapdhyay* – Intel Corp.

R. Patel – Intel Corp.

We propose to deal with some aspects of design for low power (active and well as leakage power), device design basics with focus on the different types of leakage power and implications for a lower leakage device, VLSI CAD tools used in the industry to reduce power at the architectural, gate level (ASIC and Random cell based logic), transistor circuit level, physical design level, physical design (mask) level. Since leakage power is getting to be close to 40 % of the overall power in 90nm and 65nm designs we will emphasize on leakage power reduction.

The followings are list of contents:

- I. Introduction to Low Power Design Techniques
- II. Architectural Level Low Power Design
- III. Device Design and Applications on Low Power Design
- IV. Low Power Memory/SRAM Design
- V. Leakage Reduction Techniques
- VI. Active Power Reduction Techniques
- VII. Low Power Tools and Methodologies for ASIC/Custom designs
- VIII. Concluding Remarks

Intended Audience: VLSI design engineers, CAD tool developers, Design Automation Engineers, PhD research students, Graduate students focussing on Low power VLSI design, EDA tool Application Engineers

Tutorial 4.2 (HALF DAY)
 Tuesday, January 27, 13:30-16:30 Room 416+417
**Energy, Fault-tolerance, and Scalability Issues
 in Designing Networks-on-chip**

Organizer: *R. Marculescu* – Carnegie Mellon University, USA

Speaker: *R. Marculescu* – Carnegie Mellon University

The goal of this tutorial is to present the theoretical foundations and the design implications of using the Network-On-Chip (NOC) approach in designing the communication infrastructure of future Systems-On-Chip (SOCs). Step-by-step, the audience will be introduced to the key elements of this new communication paradigm, ranging from the properties of the underlying graphs, to possible implementations of complex applications via the NOC approach. Such a communication-centric design methodology addresses not only some of the short-term challenges related to IP-reuse and computation-communication separation of concerns, but also provides a robust solution for the long-term challenges imposed by the on-chip integration of mixed-technologies and mixed-design styles in next generation systems.

Besides the mathematical models and basic design issues that are specific to SOCs, this tutorial will address in detail the interplay between the communication infrastructure and the communication paradigm on one side, and between the dissipated energy and the achievable performance, in the presence of complex failure mechanisms, on the other

side. Indeed, as CMOS technology approaches the nanometer domain, the circuit behavior becomes more susceptible to process parameter variation, noise disturbances, high energy particles, etc. thereby necessitating some degree of built-in fault-tolerance during the system-level communication. This is important since a paradigm shift in the way we think about doing communication is really needed in order to build scalable and affordable systems on a single chip. Finally, the tutorial will illustrate the NOC-based communication in a practical setting with emphasis on the design issues that need to be considered for providing performance, scalability, fault-tolerance, and cost effectiveness. Intended Audience: This tutorial is intended for researchers, engineers, students and educators trying to understand and utilize the NOC approach to solve their practical problems. Tutorial Summary: By participating in this tutorial, the attendees will learn what the NOCs are all about and what they have to offer to the designers of future SOCs. Finally, the audience will get exposure to state-of-the-art NOC architectures and their practical implementation.

ASP-DAC 2004 at a Glance

Tuesday, January 27

FULL-DAY Tutorials

TUTORIAL 1	(9:00-17:00)	Room 411+412
Recent Advances and Future Challenges in Design Verification		
TUTORIAL 2	(9:00-17:00)	Room 413
Design and Runtime Techniques for Leakage Control and Minimization of CMOS VLSI Circuits in Active and Sleep Modes		
TUTORIAL 3	(9:00-17:00)	Room 414+415
System-Level Design Methodology for SoC Design		

HALF-DAY Tutorials

TUTORIAL 4.1	(9:00-12:00)	Room 416+417
Low Power Design Techniques and Tools		
TUTORIAL 4.2	(13:30-16:30)	Room 416+417
Energy, Fault-tolerance, and Scalability Issues in Designing Networks-on-chip		

Wednesday, January 28

	A	B	C	D	E
	Room 411+412	Room 413	Room 414+415	Room 416+417	Room 419
8:30	Opening Session				
9:00	Keynote Address I				
10:00	Coffee Break (Room 418)				
10:15	1A Selected European Activities	1B Floorplanning	1C Modeling for Analog Circuits	1D Behavioral Synthesis	1E Delay Test and BIST
12:15	Lunch Break				
13:30	2A Embedded System Applications	2B Placement	2C RF Design Methodology	2D Practical Issues in Logic Synthesis	2E Effective Test and Diagnosis
15:30	Coffee Break (Room 418)				
16:00	3A System-Level Design Methodology	3B Advanced Design and Modeling Techniques	3C Analog Design and Evaluation	3D System Design Verification	3E Opportunities with the Open Architecture Test System
18:00					

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Thursday, January 29

	A	B	C	D
	Room 411+412	Room 413	Room 414+415	Room 416+417
9:00	4A C-Based Design Examples	4B Buffered Tree Construction	4C Power-Aware Approach for Microprocessor Design	4D Analog Layout Techniques
10:30	Coffee Break (Room 418)			
10:45	5A Formal Verification	5B Routing Methodology	5C Exploration for Advanced SoC Design	5D Embedded Software
12:15	Lunch Break			
13:30	6A RF Modeling and Design Methodology	6B Power Grid Analysis and Design	6C University Design Contest	6D Novel Techniques in Logic Synthesis
15:30	Coffee Break at EDSF site / Design Contest Poster Discussion at ASP-DAC site (Room 418)			
16:30	7A Future of ITS Technologies in the Ubiquitous Society	7B Buffer Planning	7C Design Verification and Simulation	7D Task Scheduling with DVS
18:00	Banquet 18:30–20:30 (Room 501+502)			

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Friday, January 30

	A	B	C	D
	Room 411+412	Room 413	Room 414+415	Room 416+417
9:00	Keynote Address II			
10:00	Coffee Break/Design Contest Poster Discussion at ASP-DAC site (Room 418)			
10:15	8A Global Routing	8B Interconnect and ESD Extraction	8C Reconfigurable Systems	8D HW/SW Co-Design
12:15	Lunch Break			
13:30	9A DFM in nm-Process Generation	9B Advanced Interconnect Analysis	9C Future Reconfigurable Computing System	9D System-Level Architecture
15:30	Coffee Break at EDSF site/Design Contest Poster Discussion at ASP-DAC site (Room 418)			
16:30	10A Embedded System Architectures	10B Crosstalk Noise Analysis	10C Expressions for Boolean Functions	10D Semi-Custom Techniques in System Design
18:00				

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Registration

Conference pre-registration is strongly advised. Participants are therefore requested to fill in and return the enclosed registration form together with the appropriate fee to the conference secretariat. Registration will be confirmed only upon receipt of the registration fee. Web-based registration is recommended. Please visit the Online Registration page: (<http://www.aspdac.com/>).

FEES

Category	By Dec. 19, '03	After Dec. 20, '03 and on site
[Conference]		
*Member	38,000 yen	42,000 yen
Non-member	48,000 yen	52,000 yen
Full-time Student	18,000 yen	22,000 yen
One-day ONLY	25,000 yen	27,000 yen
[Tutorial] (Full-Day and two Half-Days)		
*Member	24,000 yen	28,000 yen
Non-member	30,000 yen	34,000 yen
Full-time Student	15,000 yen	17,000 yen
[Tutorial] (Half-Day)		
*Member	15,000 yen	17,000 yen
Non-member	18,000 yen	20,000 yen
Full-time Student	9,000 yen	10,000 yen

(* Member of IEEE, ACM SIGDA, IEICE, IPSJ)

The registration fee includes:

- Admission to all sessions without tutorial
- Banquet (excluding Full-time students and One-day ONLY)
- One refreshment per break
- Congress kit (with a program and a copy of proceedings)

The tutorial fee includes:

- Admission to full-day or half-day tutorial(s)
- One copy of text
- One refreshment per break

PAYMENT

All registration fees must be paid in Japanese yen by bank remittance or credit card(only for residents outside Japan). Please note that personal checks and bank drafts will not be accepted.

Bank Remittance

Please remit the appropriate amount to the following bank account.

Name of Bank: **SUMITOMO MITSUI BANKING CORPORATION (The Mitsui Sumitomo Bank) Marunouchi Branch**
 Account Title: **ASP-DAC2004 MASAHARU IMAI**
 Account No.: **6583544** (Ordinary)

Credit Card (only for residents outside Japan)

Please fill out the appropriate section on the registration form. The following credit cards will be accepted:
 VISA, MasterCard, American Express, Diners Club

CANCELLATION AND REFUND

When written notification of cancellation is received by the conference secretariat by December 19, 2003, 5,000 yen will be deducted from the fees paid to cover administrative costs. No refunds will be made for cancellation requests received after this date.

REGISTRATION HOURS

Tuesday,	January 27:	7:30 – 18:00
Wednesday,	January 28:	7:00 – 17:00
Thursday	January 29:	7:30 – 17:00
Friday	January 30:	7:30 – 17:00

Registration (1/3)

Registration Form

ASP-DAC 2004

January 27 – 30, 2004, Yokohama, Japan

Advance Registration Deadline: Dec. 19th, 2003

Web-based registration is recommended. Please visit the Online Registration page (<http://www.aspdac.com/>).

If web-based registration is not convenient, please complete and make a copy and drop it in the postal mail or fax it to:

ASP-DAC 2004 SECRETARIAT

Japan Electronics Show Association
 Sumitomo Shibadaimon Bldg. 2-gokan,5F
 1-12-16, Shibadaimon, Minato-ku, Tokyo, 105-0012 JAPAN
 Tel: +81-3-5402-7601 Fax: +81-3-5402-7605
 E-mail: aspdac2004@aspdac.com

ASP-DAC 2004 Registration Form

Registrant: ()Prof. ()Dr. ()Mr. ()Ms. (Please choose one.)

Family name: _____ First name: _____

Other name: _____

Affiliation: _____

Mailstop: _____

Dept./Div.: _____

Mailing address: _____ City: _____

State: _____ Zip: _____ Country: _____

Phone: _____ Fax: _____

E-mail: _____

Membership: ()IEICE ()IPSJ ()ACM SIGDA ()IEEE

Member code: _____

Tutorial: (Please choose one Full-Day topic or one/two Half-Day topics.)

()Tutorial 1(Full-Day): Recent Advances and Future Challenges in Design Verification

()Tutorial 2(Full-Day): Design and Runtime Techniques for Leakage Control and Minimization of CMOS VLSI Circuits in Active and Sleep Modes

()Tutorial 3(Full-Day): System-Level Design Methodology for SoC Design

()Tutorial 4.1(Half-Day): Low Power Design Techniques and Tools

()Tutorial 4.2(Half-Day): Energy, Fault-tolerance, and Scalability Issues in Designing Networks-on-chip

Registration (2/3)

Registration Fee & Payment Method

Category	By Dec. 19, '03	After Dec. 20, '03	Total (Official use only) Amount Received	
[Conference]				
Member	38,000 yen	42,000 yen	¥ _____	¥ _____
Non-member	48,000 yen	52,000 yen	¥ _____	¥ _____
Full-time Student	18,000 yen	22,000 yen	¥ _____	¥ _____
One-day ONLY	25,000 yen	27,000 yen	¥ _____	¥ _____
(Please circle a date : 1/28 1/29 1/30)				
[Tutorial] (Full-Day and two Half-Days)				
Member	24,000 yen	28,000 yen	¥ _____	¥ _____
Non-member	30,000 yen	34,000 yen	¥ _____	¥ _____
Full-time Student	15,000 yen	17,000 yen	¥ _____	¥ _____
[Tutorial] (Half-Day)				
Member	15,000 yen	17,000 yen	¥ _____	¥ _____
Non-member	18,000 yen	20,000 yen	¥ _____	¥ _____
Full-time Student	9,000 yen	10,000 yen	¥ _____	¥ _____
		Grand Total	¥ _____	¥ _____

() BANK TRANSFER:

I remitted or will remit a grand total of _____ yen on _____ (date/month/year) through my bank named _____

_____ to the following account:

Name of Bank: **SUMITOMO MITSUI BANKING CORPORATION (The Mitsui Sumitomo Bank) Marunouchi Branch**

Conference Account Title:

ASP-DAC2004 Masaharu Imai

Account No.: **6583544 (Ordinary)**

() CREDIT CARD: (only for residents outside Japan.)

() VISA () MasterCard () American Express () Diners Club

Amount to be paid: _____ yen

Card No.: _____ - _____ - _____ - _____

Exp. Date: ____ / ____ (month/year)

Cardholder's name: _____

Authorized Signature: _____

Date: _____ Signature: _____

Invoices and Receipts

Invoice Required? () Yes () No

If you replied "Yes," and you would like the invoice to be sent to a different address from that of your registration, please input the address below.

Invoice to (name): _____

Address: _____

Receipt Required? () Yes () No

If you replied "Yes," and you would like the receipt to be sent to a different address from that of your registration, please input the address below.

Receipt to (name): _____

Address: _____

Registration (3/3)

Attendee Survey

1) Which category best describes your work? (choose one only)

- () Exec./Senior Mgmt. () CAD Developer
- () Design Eng. Mgmt. () Research/Educator
- () Development Eng. Mgmt. () Marketing/Sales
- () Other Mgmt. () Student
- () Design Engineer () Other

2) What design area(s) are you focused on?

- () Digital ICs () ASICs
- () Digital Systems () PLDs
- () Analog ICs/Mixed Signal ICs () FPGAs
- () Analog Systems/Mixed Signal Systems () PCB Layout

Note:

1. All payments must be in Japanese yen.
2. Bank drafts and personal checks will not be accepted.
3. If paying by credit card, please visit the Online Registration page (<http://www.aspdac.com/>) or send this form by postal mail.
4. The remitter's name should be the same as the registrant's name.
5. If paying by bank transfer using your company's name, please advise us of the ID#, registrant's name, and transfer date (the day you transfer the fees) by e-mail to aspdac2004@aspdac.com or by Fax at +81-3-5402-7605. If you don't advise us above information within a week after you transfer the fee, we can't confirm your payment.
6. Handling fees and other bank transfer fees are to be borne by the registrant.
7. If payment of the registration fee is unremitted, or the credit card charge cannot be authorized, please go to the accounting desk.
8. If registered contents are changed or added, please notify the ASP-DAC 2004 Secretariat by e-mail at aspdac2004@aspdac.com or by Fax at +81-3-5402-7605. (Please be sure to specify your ID#.)

Information

Proceedings:

ASP-DAC 2004 will be producing two versions of the ASP-DAC 2004 Proceedings; a bound paper version and a CD-ROM version. All papers will be included in both versions. Registration in any of the categories will include copies of both versions of the ASP-DAC 2004 Proceedings. Additional Proceedings will be available for purchase at the Conference. Prices are as follows:

Paper Form: ¥5,000; CD-ROM Form: ¥2,000;

Both versions of the proceedings will also be available for purchase after the conference; please contact IEEE for the bound version and ACM SIGDA for the CD-ROM version.

Banquet:

Conference registrants are invited to attend a banquet to be held on January 29, 2004. The banquet will be held from 18:30 to 20:30 at Room 501+502, the fifth floor of the conference center. Regular Member and Non-member registrants receive a ticket to the banquet when they register at the conference. Full-time students and One-day/Tutorial-only registrants wishing to attend the banquet will be required to pay ¥5,000 for a ticket when they register on site.

Visa Application:

Without a legal visa, foreign participants may be denied entry into Japan. Please contact your nearest Japanese embassy in order to ensure entry. Notice that the ASP-DAC 2004 Organizing Committee issues the invitation letters and supports the VISA applications only for presenters of the conference papers. All the other attendees have to apply for VISA through their travel agents or by yourself. In some cases it may take two months to obtain a legal visa. The following Web page of Japanese embassy may be helpful.

<http://www.mofa.go.jp/j.info/visit/visa/index.html>

Customs:

Japanese customs are fairly lenient and allow bringing in items necessary for personal use. Duty-free imports are: 3 bottles of liquor; 400 cigarettes or 100 cigars; 2 ounces of perfume; gifts and souvenirs other than the above whose total market value does not exceed 200,000 yen. Strictly prohibited are firearms, other types of weapons and narcotics.

Insurance:

The organizer cannot accept responsibility for accidents which might occur. Delegates are encouraged to obtain travel

insurance (medical, personal accident, and luggage) in their home country prior to departure.

Climate:

The temperature in Yokohama during the period of the Conference ranges between 5°C and 12°C

Currency Exchange:

Only Japanese Yen(¥) is accepted at ordinary stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can exchange your currency for Japanese Yen at foreign exchange banks and other authorized money exchange offices with your passport.

Electrical Appliances:

Electrical appliances are supplied on 100 volts in Japan. The frequency is 50 Hz in eastern Japan including Tokyo, Yokohama and 60 Hz in western Japan including Kyoto and Osaka.

Shopping:

The business hours of most department stores are from 10:00 to 20:00. They are open on Sundays and national holidays, but may close on some weekday. Business hours of retail shops differ from one another, but most shops operate from 10:00 to 20:00. Shops are open on Sundays and national holidays.

Sightseeing:

<http://www.city.yokohama.jp/ne/info/hotspotE.html>

Participants can get sightseeing information at the Nippon Express Co., Ltd. Travel desk in the Conference site during the Conference period.

Yokohama Bay Sightseeing Cruise

You can ride a cruise boat at Yamashita Park sightseeing Boat Terminal, Minato Mirai Pukarisanbashi Pier (MM21), etc. For more information, reference the home page at:

<http://www.city.yokohama.jp/ne/sights/spot/h/kasen-e.html>

CHINA TOWN

Being the largest Chinese settlement in Japan, Chinatown is always alive with people who come to enjoy Chinese food. It is also a fun place for shopping or just walking around its many streets and alleys lined with colorful restaurants, shops overflowing with Chinese goods and stores that sell exotic ingredients and Chinese medicines.

LANDMARK TOWER

296 meters high with 70 stories above ground and three levels underground. It is Japan's tallest skyscraper. A 40-second ride on the world's fastest elevator skyrockets you

to the 69th floor's Sky Garden, the highest observatory in Japan.

Hours: 10:00-21:00 Admission: ¥1,000

Access: 7min. Walk from Sakuragicho station.

SANKEIEN GARDEN

A purely Japanese-style landscape garden. Accenting the main garden is an impressive three-story pagoda and graceful garden bridges. Inside contains several old houses and farm buildings as well as Important Cultural Properties such as Rinshunkaku Villa and Chosukaku House.

Hours:9:00-16:00 Admission:¥300 for each garden

Access: From Sakuragicho Sta., take Bus NO.8 or No.125 to Honmoku-Sankeien-mae.

MARINE TOWER

106 meters, the tallest inland lighthouse in the world, with an observatory located 100 meters above ground.

Hours: 10:00-21:00 Admission: ¥700

Access: 15min. Walk from JR Ishikawacho sta.

MARITIME MUSEUM

The site of the previous Nippon Maru, the former training ship for Japan's Maritime Defense Force. The Yokohama Maritime Museum, which specializes in ports and ships, is located next to the Nippon Maru.

Hours: 10:00-17:00 (Closed Monday) Admission: ¥600

Access: 7 min. walk from JR Sakuragicho sta.

JOYPOLIS

An amusement theme park developed by Sega Enterprises, a computer game company. Many games are interactive, and featured attractions are VR-I, the world's first virtual reality motion ride, Ghost Hunters, Astronomicon, AS-I, and Indi Formula.

Hours: 10:00-23:00 Admission: ¥500 (1 day pass ¥3,600)

Other Information:

JAPANTOURIST ORGANIZATION

<http://www.jnto.go.jp/>

YOKOHAMA CONVENTION & VISITORS BUREAU

<http://www.welcome.city.yokohama.jp/tourism/>

NARITA AIRPORT

http://www.narita-airport.or.jp/airport_e/index.html

YES! TOKYO

http://www.tcvb.or.jp/en/index_en.htm

Accommodations

OFFICIAL TRAVEL AGENT

Nippon Express Co., Ltd. has been appointed as the official travel agent. Inquiries and applications concerning arrangements should be addressed to:

Nippon Express Co., Ltd.

Foreign Tourist Dept.

Address: 1-5-2 Shimbashi, Minato-ku, Tokyo, 105-0004 Japan

Phone: +81-3-3573-8450

Fax:+81-3-3573-8453

e-mail: tokyo-gaikokujin@trv.nittsu.co.jp

Person in charge: Ken'ichi OMOTO

HOTEL RESERVATION

Nippon Express has reserved blocks of rooms at hotels in Yokohama during the period. Please fill in the Hotel Reservation Form and submit it to Nippon Express by 19th December, 2003. Reservation will be made on a first-come, first-served basis. Please indicate your order of preference in the application form. If your desired hotel is fully booked, Nippon Express will reserve your second choice or a hotel in the same grade. Hotel charge should be paid directly to the hotel at checkout time. When submitting the application, please indicate credit card number, expiry date and card holder's signature. Confirmation of hotel reservation will be sent by fax. Hotel reservation will not be honored without this confirmation.

Cancellation of Hotel Reservation

In the event of cancellation, written notification should be sent to JTB. The following cancellation fees will be charged to your credit card.

Up to 9 days before the first night of stay	2,000yen
8 to 2 days before	20% of daily room charge (minimum 2,000yen)
one day before or after	100% of daily room charge
No notice given	100% of daily room charge

Hotels

#	Name and Address	One Night Stay Fee / Room	Location
A	Yokohama Grand Inter-Continental 1-1-1 Minatomirai, Nishi-ku, Yokohama-shi TEL: +81-45-223-2222 FAX: +81-45-221-0650	Single: ¥14,500 (BB: ¥16,000) Twin: ¥17,000 (BB: ¥20,000)	Adjacent to Pacifico
B	Pan Pacific Hotel Yokohama 2-3-7 Minatomirai, Nishi-ku, Yokohama-shi TEL: +81-45-682-2222 FAX: +81-45-682-2223	Single: ¥14,000 (BB: ¥17,000) Twin: ¥17,000 (BB: 22,000)	2 min. walk to Pacifico
C	Yokohama Royal Park Hotel 2-2-1-3 Minatomirai, Nishi-ku, Yokohama-shi TEL: +81-45-221-1111 FAX: +81-45-224-5153	Single: ¥15,400 (BB: ¥18,260) Twin: ¥22,000 (BB: ¥27,760)	5 min. walk to Pacifico
D	Yokohama Sakuragicho Washington Hotel 1-1-67 Sakuragi-cho, Naka-ku, Yokohama-shi TEL: +81-45-683-3111 FAX: +81-45-683-3112	Single: ¥8,000 (BB: ¥9,000) Twin: ¥13,000 (BB: ¥15,000)	8 min. walk to Pacifico
E	Breeze Bay Hotel 1-22-2 Hanasaka-cho, Naka-ku, Yokohama-shi TEL: +81-45-253-5555 FAX: +81-45-253-5511	Single: ¥8,000 (BB: ¥9,000) Twin: ¥13,000 (BB: ¥15,000)	13 min. walk to Pacifico
F	Yokohama Mandarin Hotel 4-170 Noge, Naka-ku, Yokohama-shi TEL: +81-45-243-3131 FAX: +81-45-243-3139	Single: ¥7,500 (BB: ¥9,000) Twin: ¥13,000 (BB: ¥16,000)	18 min. walk to Pacifico

* BB = with breakfast

Note:
Room charge includes service charge but not including 5% tax.

Hotel Reservation (1/2)

Hotel Reservation Form

ASP-DAC 2004

January 27 - 30, 2004, Yokohama Japan

Please complete and return this form to:
Nippon Express Co., Ltd.
Foreign Tourist Dept.
Address: 1-5-2 Shimbashi, Minato-ku, Tokyo, 105-0004 Japan
Phone: +81-3-3573-8450 Fax: +81-3-3573-8453
e-mail: tokyo-gaikokujin@trv.nittsu.co.jp

Deadline: Dec. 19, 2003

Note: You should send this form by postal mail or fax when you apply.

(Please type or write in block letters.)

Full Name: ()Prof. ()Dr. ()Mr. ()Ms.

Family Name: _____, First Name: _____

Middle Initial: _____

Affiliation: _____

Mail Stop: _____

Dept./Div.: _____

Mailing Address: _____

City: _____ State: _____

Zip: _____ Country: _____

Phone: _____ Fax: _____

E-mail: _____

Please remember to include your country and/or city code for Phone/Fax numbers.

Name of Accompanying Person(s), Family Member(s) if any:
()Mr. ()Ms.

Family Name: _____, First Name: _____

Middle Initial: _____

Arrival Schedule:

Arriving at _____(airport) on _____(date)

by _____(flight number)

Hotel Reservation (2/2)

Hotel Accommodations:

Please select 2 hotels in order of preference and enter the name of the hotel and the hotel number(see hotel list in this program).

1st choice: _____(No.)

2nd choice: _____(No.)

Room Choice: ()Single ()Twin

Breakfast: ()Yes ()No

Period of Stay: Check-in _____ Check-out _____ for __ nights

Guarantee of Booking:

Credit Card: ()AMEX()VISA()Master Card()Diners Club

Card Number: _____- _____- _____- _____

Card Holder's Name : _____

Expiration Date: ____/____(month/year)

Authorized Signature: _____

Access to Pacifico Yokohama

By Train

[From direction of Tokyo]

Tokyo Station	JR Tokaido line, 25min., JR Yokosuka Line, 29 min.	Yokohama Station
	JR Keihin-Tohoku Line, 41 min.	Sakuragicho Station
Shinagawa Station	Keikyū Line express, 15 min.	Yokohama Station
Shibuya Station	Tokyu Toyoko Line, 37 min.	Sakuragicho Station

[From direction of Kansai & Chubu]

Tokaido-Sanyo bullet train	Shin Yokohama Station	Yokohama subway, 15 min.	Sakuragicho Station
		JR Yokohama Line, 15 min.	

● Minato Mirai 21 Line open from February 2004

By Air

[From Narita Airport]

JR Narita Express, 90 min.		Yokohama Station	
Airport Limousine Bus, about 90 min.	YCAT (Yokohama City Air Terminal)	taxi or bus, about 10 min.	Pacifico Yokohama

-Some Airport Limousine Buses go direct to Pacifico Yokohama via YCAT.

[From Haneda Airport]

Tokyo Monorail, 23 min.	Hamamatsucho Station	JR Keihin-Tohoku Line, 38 min.	Sakuragicho Station
Airport Limousine Bus, about 30 min.	YCAT	taxi or bus, about 10 min.	Pacifico Yokohama
Keikyū Airport Line, 6 min.	Keikyū Kamata Station	Keikyū express, 12 min.	Yokohama Station

Driving

[From direction of Tokyo] (About 30min. from Tokyo Station)

Toward Yokohama Park on Shuto Turnpike Yokohama Route	Minato Mirai Ramp, about 1 min.	Pacifico Yokohama
Toward Yokohama (over Bay bridge) on Shuto, Wangan Route	Minato Mirai Ramp, about 1 min.	

[From direction of Kansai or Chubu]

Tomei Turnpike	Yokohama Interchange	Hodogaya Bypass	Kariba Interchange	Shuto, Kariba Route	
Ishikawacho Interchange	Shuto, Yokohama Line	Minato Mirai Ramp, about 1 min.			Pacifico Yokohama

From Sakuragicho st.

[On foot]	About 12 min. via Moving Walkway
[By bus]	From Bus Stop 1 to Pacifico Yokohama, about 7 min.
[By taxi]	About 5 min.

From Yokohama st.

[By Train]	To Sakuragicho Station by JR Keihin-Tohoku Line or Tokyu Toyoko Line, about 3 min.	
[By Bus from terminal on 1st floor of Sogo Department Store, east entrance]	From Bus Stop 14 for Pacifico Yokohama, about 10 min.	Pacifico Yokohama
[By Taxi from stand at 2nd basement of Porta east entrance]	About 10 min.	
[By Sea Buss from Sea Bass stop at Yokohama Sogo Department Store car park on 1st floor]	About 10 min.	

PACIFICO YOKOHAMA Parking Lot

Minato Mirai Public Parking Lot (Underground)	Capacity: 1200 (Standard-sized cars only)	Open 24 hours
Rates: Standard-sized car ¥520/1hour		

Venue Map/ Room Assignment

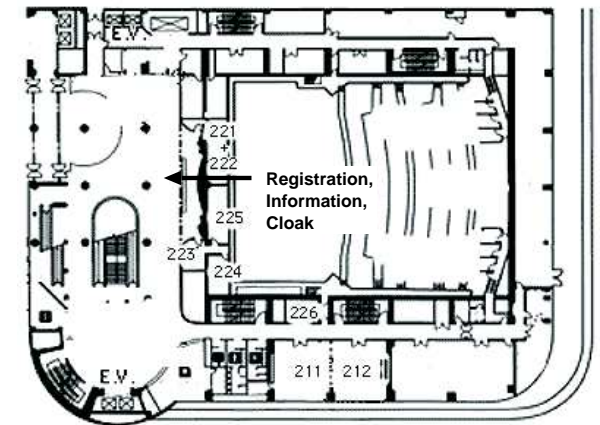
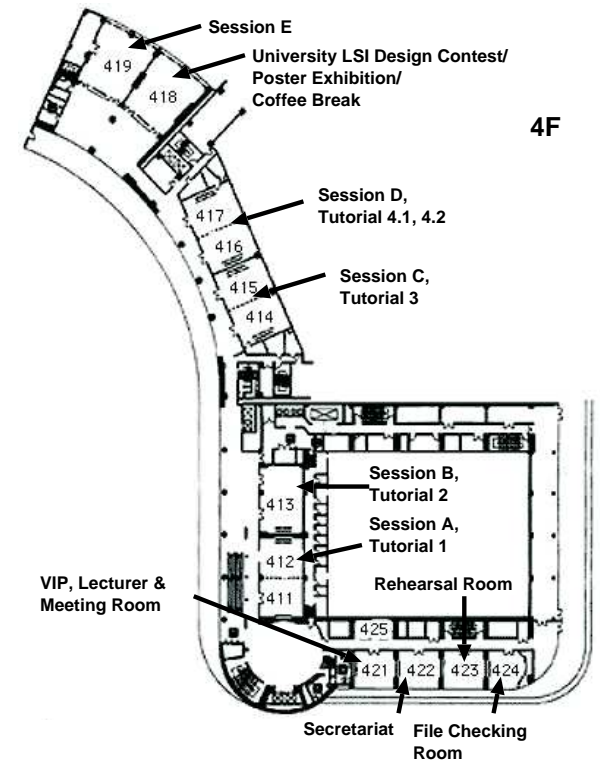
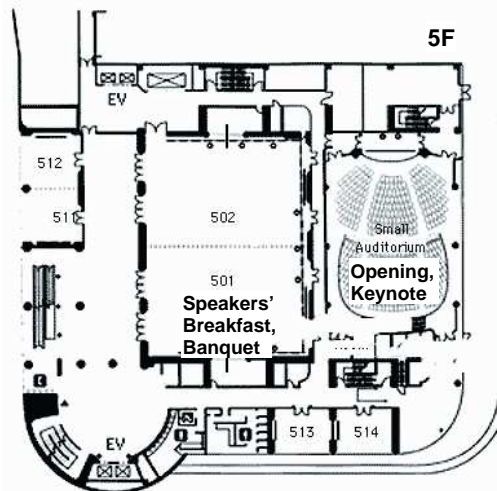
- ASP-DAC Conference is held at "Conference Center."
- EDS Fair & Afternoon Coffee Break on 29th and 30th are held at "Exhibition Hall." (2min. walk from Conference Center.)

EDS Fair / Afternoon Coffee Break on 28th, 29th



Conference Venue Map

Location	Event
Exhibition Hall	EDS Fair & Afternoon Coffee Break on 28th, 29th
Entrance Hall (2F)	Registration, Information, Cloak
Small Auditorium (5F)	Opening, Keynote
411+412(4F)	Session A, Tutorial 1
413(4F)	Session B, Tutorial 2
414+415(4F)	Session C, Tutorial 3
416+417(4F)	Session D, Tutorial 4.1, 4.2
419(4F)	Session E
418(4F)	Poster Discussion, Coffee Break
421(4F)	VIP, Lecturer & Meeting Room
422(2F)	Secretariat
423(5F)	Rehearsal Room
424(5F)	File Checking Room
501(5F)	Speakers' Breakfast
501+502(5F)	Banquet



Conference Center Map

