ASP-DAC 2005

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By Zhenghua Jiang
Thursday, January 20, 9:00-10:00 Imperial Hall 1-2
"Silicon Compilation: The answer to reducing IC development costs"
By Rajeev Madhavan
Friday, January 21, 9:00-10:00 Imperial Hall 1-2
"Design at the End of the Silicon Roadmap"
By Jan M. Rabaey

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"Panel Discussion: Are We Ready for System-Level Synthesis?"
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By Todd Austin, Valeria Bertacco, David Blaauw, and Trevor Mudge
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By Ashok Jagannathan, Hannah Yang, Kris Konigsfeld, Dan Milliron, Mosur Mohan, Michail Romesis, Glenn Reinman, and Jason Cong

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David Greavers, TensionEDA

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Jaijeet Roychowdhury, University of Minnesota

T-5: Current Practices and Future Directions in High-Level Design Verification
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Mukul Prasad, Fujitsu Laboratories of America, Inc.
Rajarshi Mukherjee, Calypto Design Systems
Masahiro Fujita, The University of Tokyo

Tuesday, January 18, 2005, 13:30-16:30

T-4: Intellectual Property Protection in Semiconductor and VLSI Design
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Shauki Elassaad, Rio Design Automation
Zhenhai Zhu, IBM Research Center
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Satellite Workshop

Tuesday, January 18, Time 17:00-21:00
The 3rd Asian University Workshop on Semiconductor Design
Sponsored by City of Kitakyusu

Thursday, January 20, Time 13:30-17:00
The 2nd International Workshop on Compact Modeling (IWCM'05) in Conjunction with ASP-DAC 2005

Welcome to ASP-DAC 2005

It's a great pleasure for me on behalf of the Organizing Committee to welcome you to the tenth Asia and South Pacific Design Automation Conference (ASP-DAC 2005) which is a sister conference of DAC, DATE, and ICCAD. ASP-DAC 2005 will be held in Hotel Equatorial, Shanghai, China during Jan. 18-21, 2005. At the same time, an exhibition about IC design tools, testing technique, and other aspects related microelectronic technology will be held in the same hotel.

The aim of the conference is to provide a forum for the researchers and engineers who are working in the fields of SOC/VLSI Circuits design and EDA/CAD technologies to discuss and exchange the state-of- the- art information on these topics.

We have invited three worldwide experts to give keynote addresses on Development of Chinese IC industry, Silicon Compiler - Back to the Future and Design at the End of the Silicon Roadmap.

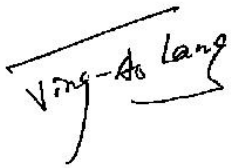
The TPC, led by Professors Xianlong Hong, C.K.Cheng, Hidekazu Terai, Tony Ma and Youn-Long Lin, have reviewed received 692 papers from 32 countries and areas to organize the excellent program. After detail reviewing by the members of 11 TPC sub-session, 99，86 and 95 papers are selected as full papers, short papers and posters, respectively. Those papers cover the wide areas of hot topics on SOC, VLSI design, physical design, testing, TCAD and so on.

The Program includes six tutorial sessions and three panel discussions. The 3rd Asian University Workshop on Semiconductor Design sponsored by City of Kitakyushu, Japan is planned at the first day together with ASP-DAC 2005. A satellite workshop on CM and a Ph.D. Forum are also planned to be held during ASP-DAC.

The program includes also an important event- University VLSI Design Contest. The chairs of Design Contest Committee, Prof. Xiaoyang Zeng, Makoto Ikeda and Lin Yang selected outstanding designs for presentation.

It's the first time for ASP-DAC to be held in Shanghai, China. As the host of the Conference, we'll do our best to make you enjoy your stay in Shanghai.

We sincerely hope you have a good time in Shanghai, in China.



Ting-Ao Tang
General Chair
ASP-DAC 2005

Technical Program Co-Chairs' Message

On behalf of the Technical Program Committee for the Asia and South Pacific Design Automation Conference 2005, we would like to welcome all of you to the conference held from January 18 through 21, 2005 at Hotel Equatorial in Shanghai, China.

We received 692 submissions for the technical papers which is equivalent to 238% of the number last year (291 submissions). The authors span 32 countries/regions in Asia, North America, South America, Europe, Oceania, and Africa.

The Technical Program Committee was composed of 164 experts on EDA, LSI designs, and embedded system designs, and was organized into 11 topic groups. Each topic group selected high quality papers through in-depth and prudent discussions.

Among the submissions, 99, 86, and 95 articles were accepted as regular, short, and poster papers which correspond to the acceptance ratios of the top 14.3%, 26.7%, and 40.5%, respectively. Note that the total acceptance ratio of last year was 50.8%. Accepted papers will be presented in 36 technical sessions spanning 5 parallel tracks.

In addition to the regular technical sessions, we have several keynote speeches and special sessions. The special sessions are composed of three panels, three invited talks, and three embedded tutorials. Panel discussions are scheduled in Sessions 3D-3E, 6D-6E, and 9D-9E. Session 3D-3E, organized by C. K. Cheng and Steve Lin, speculates "Who Is Responsible for the Design for Manufacturability Issues in the Era of Nano-Technologies?" Session 6D-6E, organized by Jason Cong and Tony Ma, is entitled "Are We Ready for System-Level Synthesis?" Session 9D-9E, organized by David Chen, investigates "EDA Market in China."

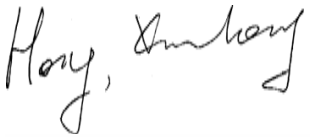
The invited talks are presented by distinguished researchers. Session 4D entitled "CAD for Microarchitecture Designs" covers many emerging topics concerning the CAD for Microarchitecture Designs and related research activities. Three tutorial talks by top researchers are also embedded in the technical sessions. The subjects in these tutorials include recent important progresses in design for manufacturability, leakage power, and designing reliable circuits in the pres-

ence of soft errors.

As Co-Chairs of the Technical Program Committee, we would like to thank all members of the Technical Program Committee; Topic Chairs and their Vice Topic Chairs, David Chen, Soonhoi Ha, S. K. Nandy, Jihua Chen, X. Sharon Hu, Chong-Min Kyung, Jinian Bian, Jianwen Zhu, Jin Yang, Yunshan Zhu, Alan J. Hu, Huazhong Yang, Sheldon X.-D. Tan, Tong Jing, Martin D. F. Wong, Cheng-Kok Koh, Takeshi Yoshimura, Xiao-Wei Li, Terumine Hayashi, Xuan Zeng, Albert Wang, Koichiro Mashiko, Zhiping Yu, Kenji Nishi, Yu-Liang (David) Wu, Yao-Wen Chang, Lei He, Yihe Sun, Hoi-Jun Yoo, Takao Onoye; reviewers of papers; session organizers; and moderators. We would like to express our sincere thanks to authors who submitted papers and speakers who will present their papers at the conference. We are grateful to the Publication Chair, Rongzheng Zhou, and the workgroup, Tong Jing, Yu Hu, Yongqiang Lu, Yin Wang, Jingjing Fu, Jinghong Liang, Qiang Wu, Xiren Wang, for their contributions in preparing the program brochures and the proceedings of the conference. We also thank the webmaster, Zhanguo Xi, for his contribution towards the management of the Web-based paper submitting/reviewing system.

We would be more than happy if you could attend the conference and find something new in the directions of EDA and design technologies during ASP-DAC 2005.

Co-Chairs, Technical Program Committee



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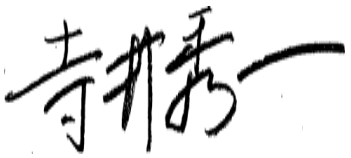
Tsinghua University, Beijing

Chung-Kuan Cheng
UCSD



Hidekazu Terai
Ritsumeikan University

Tony Ma
Synopsys

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General Chair

Ting-Ao Tang
Fudan University
Shanghai, P. R. China
Phone: +86-21-65643761; +86-21-65648267
E-mail: tatang@fudan.edu.cn

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Jason Cong
UCLA

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Synopsys

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IDT Corp.

Soonhoi Ha
Seoul National University

Jihua Chen
National University of Defence Technology

S. K. Nandy
Indian Institute of Science

X. Sharon Hu
University of Notre Dame

Chong-Min Kyung
KAIST

Jinian Bian
Tsinghua University, Beijing

Jianwen Zhu
University of Toronto

Jin Yang
Intel Corp.

Alan J. Hu
University of British Columbia

Yunshan Zhu
Synopsys

Huazhong Yang
Tsinghua University, Beijing

Tong Jing
Tsinghua University, Beijing

Sheldon X.-D. Tan
UCR

Martin D. F. Wong
UIUC

Cheng-Kok Koh
Purdue University

Takeshi Yoshimura
Waseda University

Xiaowei Li
Institute of Computing Technology, Chinese Academy of Sciencess

Xuan Zeng
Fudan University

Terumine Hayashi
Mie University

Albert Wang
Illinois Institute of Technology

Koichiro Mashiko
Semiconductor Technology Academic Research Center (STARC)

Zhiping Yu
Tsinghua University, Beijing

Kenji Nishi
Kinki University Tech. College

Yu-Liang Wu
The Chinese University of Hong-Kong

Yao-Wen Chang
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Lei He
UCLA

Hoi-Jun Yoo
KAIST

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Fudan University

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ASP-DAC 2005 SECRETARAT
Fudan University
Shanghai, P. R. China
E-mail: webmaster@aspdac2005.com

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Co-Chairs

Xianlong Hong
Tsinghua University, Beijing

C.K. Cheng
UCSD

Hidekazu Terai
Ritsumeikan University

Tony Ma
Synopsys

Steve Lin
Tsing Hua University, Hsin-Chu

Sub-Committees

(** / * indicate the subcommittee chair/vice-chair.)

[1] System Level Design Methodology

** **David Chen**
IDT Corp.

Soo-Ik Chae
Seoul National University

* **Soonhoi Ha**
Seoul National University

Ando Ki
Dynalith Systems

* **S. K. Nandy**
Indian Institute of Science

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Indian Institute of Science

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Waseda University

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Tata Consultancy Services

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Philips Research Laboratories Eindhoven

Subhasis Banerjee
Indian Institute of Science

Ed Deprettere
Leiden University

Miroslav Velev
Georgia Institute of Technology

Jun Dong Cho
SungKyunKwan University

[2] Embedded and Real-Time Systems

** **Jihua Chen**
National University of Defence Technology

Mingyan Yu
Haerbin University of Technology

* **X. Sharon Hu**
University of Notre Dame

Haibin Sheng
Zhejiang University

* **Chong-Min Kyung**
KAIST

JoAnn Paul
Carnegie Mellon University

Zebo Peng
Linkoping University

Gang Quan
University of South Carolina

Insup Lee
University of Pennsylvania

Donatella Sciuto
Politecnico di Milano

Luciano Lavagno
Politecnico di Torino, Cadence Labs

In-Cheol Park
KAIST

Chenglian Peng
Fudan University

Youngsoo Shin
KAIST

Shu Han
Peking University

[3] Behavioral/Logic Synthesis and Optimization

** **Jinian Bian**
Tsinghua University, Beijing

Yunjian Jiang
Magma Design Automation

* **Jianwen Zhu**
University of Toronto

Taewhan Kim
Seoul National University

Reinaldo A Bergamaschi
IBM T. J. Watson Research Center

Sikun Li
The National University of Defense Technology

Shih-Chieh Chang
Tsing Hua University, Hsin-Chu

Tsutomu Sasao
Kyushu Institute of Technology

Rolf Drechsler
University of Bremen

Feng Shi
Beijing Institute of Technology

Jungang Han
Xi'an Institute of Posts & Telecoms

Mingcheng Zhu
Shenzhen University

[4] Validation and Verification for Behavioral/Logic Design

** **Jin Yang**
Intel Corp.

Mahesh Iyer
Synopsys

* **Yunshan Zhu**
Synopsys

Robert B Jones
Intel Corp.

* **Alan J. Hu**
University of British Columbia

Yuan Lu
Broadcom

K. C. Chen
Cadence

Yinghua Min
Institute of Computing Technology, Chinese Academy of Sciences

Kwang-Ting (Tim) Cheng
UCSB

Carl Pixley
Synopsys

Ed Clarke
Carnegie Mellon University

Weimin Wu
Tsinghua University, Beijing

Masahiro Fujita
University of Tokyo

Tomohiro Yoneda
National Institute of Informatics

Norris Ip
Jasper

[5] Circuit Optimization and Simulation

** **Huazhong Yang**
Tsinghua University, Beijing

Xiaodong Yang
Synopsys

* **Sheldon X.-D. Tan**
UCR

Anirudh Devgan
IBM Research

Chunhong Chen
University of Windsor

Jaijeet Roychowdhury
University of Minnesota

Zuying Luo
Tsinghua University, Beijing

Zheng Shi
Zhejiang University

Yun Zheng
CED Huada Electronics Design Co., Ltd.

Eli Chiprout
Intel Corp.

Charlie Chung-Ping Chen
Taiwan University

[6] Physical Design and Interconnect Optimization

** **Tong Jing**
Tsinghua University, Beijing

* **Martin D. F. Wong**
UIUC

* **Cheng-Kok Koh**
Purdue University

* **Takeshi Yoshimura**
Waseda University

Evangeline F. Y. Young
The Chinese University of Hong Kong

David Z. Pan
The University of Texas at Austin

Chris Chu
Iowa State University

Dennis Sylvester
University of Michigan

Guoan Zhong
Magma Design Automation

Takumi Okamoto
NEC Corp.

Atsushi Takahashi
Tokyo Institute of Technology

Shigetoshi Nakatake
The University of Kitakyushu

Shin'ichi Wakabayashi
Hiroshima City University

Jinsong Hou
CEC Huada Electronic Design Co., Ltd.

Xiaoping Tang
IBM TJ Watson Research Center

Pushan Tang
Fudan University

Wenting Hou
Cadence Beijing R&D Center

Hai Zhou
Northwestern University

Patrick H. Madden
SUNY Binghamton

Weiping Shi
Texas A&M University

Honghua Hannah Yang
Intel Corp.

Charles Chiang
Synopsys

Kaijian Shi
Synopsys

Jinmei Lai
Fudan University

Sung Kyu Lim
Georgia Institute of Technology Atlanta

[7] Test and Design for Testability

** **Xiaowei Li**
Institute of Computing Technology, Chinese Academy of Sciences

* **Terumine Hayashi**
Mie University

Shi-Yu Huang
Tsing Hua University, Hsin-Chu

Michiko Inoue
Nara Institute of Science and Technology

Tomoo Inoue
Hiroshima City University

Kuen-Jong Lee
Cheng-Kung University

Huawei Li
Institute of Computing Technology, Chinese Academy of Sciences

Hua-Guo Liang
Hefei University of Technology

Alex Orailoglu
UCSD

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Chiao Tung University

Andre Ivanov
University of British Columbia

Kazuhiko Iwasaki
Tokyo Metropolitan University

Xiao-Qing Wen
Kyushu Institute of Technology

Shiyi Xu
Shanghai University

[8] Analog and RF Circuit Design

** **Xuan Zeng**
Fudan University

* **Albert Wang**
Illinois Institute of Technology

* **Koichiro Mashiko**
Semiconductor Technology Academic Research Center (STARC)

Shoji Kawahito
Shizuoka University

Chris Verhoeven
TU Delft

Wing Hung Ki
HKUST

Zhigong Wang
South East University

Baoyong Chi
Tsinghua University, Beijing

Gaofeng Wang
Wuhan University

Jin Liu
University of Texas at Dallas

[9] Design for Manufacturability and TCAD

** **Zhiping Yu**
Tsinghua University, Beijing

* **Kenji Nishi**
Kinki University Tech. College

Changhong Dai
Intel Corp.

Young-Kwan Park
Samsung

Sanford Chu
Chartered Semi

Minchie Jeng
SMIC

Wim Schoenmaker
Magwel

Wenjian Yu
Tsinghua University, Beijing

Masaharu Yamamoto
Semiconductor Technology Academic Research Center (STARC)

[10] Reconfigurable Systems

** **Yu-Liang Wu**
The Chinese University of Hong-Kong

* **Yao-Wen Chang**
Taiwan University

* **Lei He**
UCLA

Kiyoung Choi
Seoul National University

Kia Bazargan
University of Minnesota

Majid Sarrafzadeh
UCLA

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Tsing Hua University, Hsin-Chu

Wai Kei Mak
Tsing Hua University, Hsin-Chu

Kenshu Seto
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Philip Leong
Chinese University of Hong Kong

Wayne Luk
Imperial College

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Tulika Mitra
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Paul Chow
University of Toronto

Oliver Diessel
University of New South Wales

Neil Bergmann
University of Queensland

Stephen D. Brown
University of Toronto

Takeshi Kambe
Kinki University

Stephen Brown
University of Toronto

[11] Leading-Edge Designs

** **Yihe Sun**
Tsinghua University, Beijing

Xuewen Ni
Peking University

* **Hoi-Jun Yoo**
KAIST

* **Takao Onoye**
Osaka University

Minglun Gao
Hefei Technology University and Nanjing University

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Dongnan University

Guican Chen
Xi'an Jiaotong University

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Kyusyu University
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Waseda University
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Secretary
Toshihiro Hattori
SuperH (Japan), Ltd.
toshihiro.hattori@superh.com

Secretary
Kazutoshi Wakabayashi
NEC
wakaba@ccm.cl.nec.co.jp

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Steve Lin
Tsing Hua University, Hsin-Chu
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Russin Academy of Sciences
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Fudan University
Hidetoshi Onodera
Kyoto University
Isao Shirakawa
Professor Emeritus of Osaka University
Kenji Yoshida
Cadence Design Systems (Japan)

University LSI Design Contest

The University VLSI Design Contest is conceived as a unique characteristic of ASP-DAC Conference. The purpose of the Contest is to encourage education and research in VLSI design, and its VLSI implementation at universities, and other educational organizations by providing opportunities to present and discuss innovative and state-of-the-art designs at ASP-DAC conference. The Design Contest will cover at least following fields: (1) Analog, RF and mixed-Signal Circuits, (2) Digital Signal processing Circuits, (3) Microprocessors, and (4) Custom Application Specific Circuits, Methods or technology used for implementation include (a) Full Custom and Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices, including FPGA/PLDs.

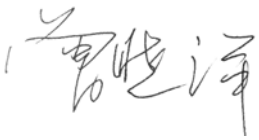
This year, we received total twenty-one designs from eight countries/areas, and twelve selected designs from six countries/areas will be disclosed in Design Contest Session with a short presentations followed by live discussions in front of posters. All the submitted designs were reviewed by the members of the University Design Contest Committee, and which are based on the following criteria: Reliability of design and implementation, Quality of implementation, Performance of the design, Novelty, and Additional special features. In the selection process, emphasis was placed more on reliability, quality, and performance. As a result, the ten designs were selected. Also, we have instituted one outstanding design award.

It is with great pleasure that we acknowledge the contributions to the Design Contest, and it is our earnest belief that it will promote and enhance research and education in VLSI design in academic organizations. It is also our hope that many people not only in academia but also in industry will attend the contest and enjoy the stimulating discussions.

Last but not the least, many thanks to the designs reviewers and other people related to our Design Contest for their hard work and

good cooperation.

Co-Chairs, University LSI Design Contest Committee



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Co-Chair
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Technical Program

Tuesday, January 18, 9:00-17:00

Tuesday, January 18, Time 9:00-17:00
One Day Tutorial Session

T-1
(Full Day)
9:00-17:00
Ming Room1
(FL.2)

T-1: C-Based Design: Industrial Experience
Srimat Chakradhar, NEC
Wakabayashi, NEC
John Correia, CoWare
David Greavers, TensionEDA

T-2
(Full Day)
9:00-17:00
Ming Room2
(FL.2)

T-2: Power Aware Design for Performance: Practical Techniques and Tools to Achieve Custom Like Performance in a Power-Aware ASICs Design Flow
Ruchir Puri, IBM Research
Leon Stok, IBM
Dennis Sylvester, University of Michigan

T-3
(Half Day)
9:00-12:00
Zhong Hua 1
(FL.3)

T-3: Automated Macromodeling Techniques for Design of Complex Analog and Mixed-Signal Integrated Systems
Georges Gielen, Katholieke Universiteit Leuven
Jaijeet Roychowdhury, University of Minnesota

T-4
(Half Day)
13:30-16:30
Zhong Hua 1
(FL.3)

T-4: Intellectual Property Protection in Semiconductor and VLSI Design
Gang Qu, University of Maryland
Ian Mackintosh, Sonics Inc.

T-5
(Half Day)
9:00-12:00
Zhong Hua 2
(FL.3)

T-5: Current Practices and Future Directions in High-Level Design Verification
Indradeep Ghosh, Fujitsu Laboratories of America, Inc.
Mukul Prasad, Fujitsu Laboratories of America, Inc.
Rajarshi Mukherjee, Calypto Design Systems
Masahiro Fujita, The University of Tokyo

T-6
(Half Day)
13:30-16:30
Zhong Hua 2
(FL.3)

T-6: Chip-Package Codesign: Power Integrity Issues, Parasitic Extraction, Parameterized Model Order Reduction, and Design Methodology.
Shauki Elassaad, Rio Design Automation
Zhenhai Zhu, IBM T.J.Watson Research Center
Luca Daniel, Massachusetts Institute of Technology

Tuesday, January 18, Time 18:00-20:00
Welcome Reception

Tuesday, January 18, Time 17:00-21:00
The 3rd Asian University Workshop on Semiconductor Design
Sponsored by City of Kitakyusu

Wednesday, January 19, 8:30-10:00

Wednesday, January 19, Time 8:30-9:15
Opening Session
Room: Imperial Hall 1-3
Moderator: Ting-Ao Tang

Wednesday, January 19, Time 9:15-10:15

Keynote Address I

Room: Imperial Hall 1-3

Moderator: Richard M. M. Chen

K-1
9:15-10:15

The Development of Integrated Circuit Industry in China

Zhenghua Jiang (Professor, Vice Chairman of The National People's Congress, PRC)

Wednesday, January 19, 10:30-12:10

Wednesday, January 19, Time 10:30-12:10

Session 1A: Tree Construction and Buffering

Organizers: Tong Jing, Martin D. F. Wong, Cheng-Kok Koh, Takeshi Yoshimura

Moderators: Patrick H. Madden, Cheng-Kok Koh

Room: Zhong Hua 1 (FL.3)

1A-1
10:30-10:55

The Polygonal Contraction Heuristic for Rectilinear Steiner Tree Construction

Yin Wang, Xianlong Hong, Tong Jing, Yang Yang (Tsinghua University, Beijing), Xiaodong Hu, Guiying Yan (Institute of Applied Mathematics, Chinese Academy of Sciences)

1A-2
10:55-11:20

An-OARSMan: Obstacle-Avoiding Routing Tree Construction with Good Length Performance

Yu Hu , Tong Jing, Xianlong Hong, Zhe Feng (Tsinghua University, Beijing), Xiaodong Hu, Guiying Yan (Institute of Applied Mathematics, Chinese Academy of Sciences)

1A-3
11:20-11:45

Making Fast Buffer Insertion Even Faster Via Approximation Techniques

Zhuo Li, C. N. Sze (Texas A&M University), Charles J. Alpert (IBM Austin Research Lab), Jiang Hu, Weiping Shi (Texas A&M University)

1A-4s
11:45-11:58

Concurrent Flip-flop and Buffer Insertion with Adaptive Blockage Avoidance

Zhong-Ching Lu, Ting-Chi Wang (Tsing Hua University, Hsin-Chu)

1A-5s
11:58-12:10

Buffering Global Interconnects in Structured ASIC Design

Tianpei Zhang, Sachin S. Sapatnekar (University of Minnesota)

Wednesday, January 19, Time 10:30-12:10

Session 1B: System Level Design Methodology for Network-on-Chip

Organizers: David Chen, Soonhoi Ha, S. K. Nandy

Moderators: X. Sharon Hu, Soonhoi Ha

Room: Zhong Hua 2 (FL.3)

1B-1
10:30-10:55

Mapping and Physical Planning of Networks-on-Chip Architectures with Quality-of-Service Guarantees

Srinivasan Murali (Stanford University), Luca Benini (University of Bologna), Giovanni De Micheli (Stanford University)

1B-2
10:55-11:20

Time and Energy Efficient Mapping of Embedded Applications onto NoCs

César Marcon, André Borin, Altamiro Susin, Luigi Carro, Flávio Wagner (UFRGS)

1B-3
11:20-11:45

Communication-driven Task Binding for Multiprocessor with Latency Insensitive Network-on-Chip

Liang-Yu Lin, Cheng-Yeh Wang, Pao-Jui Huang, Chih-Chieh Chou, Jing-Yang Jou (Chiao Tung University)

1B-4s
11:45-11:58

System-Level Communication Modeling for Network-on-Chip Synthesis

Andreas Gerstlauer, Dongwan Shin, Rainer Dömer, Daniel D. Gajski (UCI)

1B-5s
11:58-12:10

MAIA - A Framework for Network on Chip Generation and Verification

Luciano Ost, Aline Mello (FACIN -PUCRS), José Palma (UFRGS), Fernando Moraes, Ney Calazans (FACIN -PUCRS)

Wednesday, January 19, Time 10:30-12:10

Session 1C: Test and DFT (1)

Organizers: Xiaowei Li, Terumine Hayashi

Moderators: Alex Orailoglu, Xiaoqing Wen

Room: Han Room 1 (FL.3)

1C-1
10:30-10:55

Theoretic Analysis and Enhanced X-Tolerance of Test Response Compact based on Convolutional code

Yinhe Han, Yu Hu, Xiaowei Li, Huawei Li (Institute of Computing technology, Chinese Academy of Sciences)

1C-2
10:55-11:20

Test Compression for Scan Circuits Using Scan Polarity Adjustment and Pinpoint Test Relaxation

Yasumi Doi, Seiji Kajihara, Xiaoqing Wen (Kyusyu Institute of Technology), Lei Li, Krishnendu Chakrabarty (Duke University)

1C-3
11:20-11:45

Testing Comparison Faults of Ternary CAMs Based on Comparison Faults of Binary CAMs

Jin-Fu Li (Central University)

1C-4s
11:45-11:58

SPIN-PAC: Test Compaction for Speed-Independent Circuits

Feng Shi, Yiorgos Makris (Yale University)

1C-5s
11:58-12:10

A Huffman-based coding with efficient test application

Michihiro Shintani, Toshihiro Ohara, Hideyuki Ichihara, Tomoo Inoue (Hiroshima City University)

Wednesday, January 19, Time 10:30-12:20

Session 1D: (Special Session) DFM

Room: Han Room 2 (FL.3)

1D-1
10:30-11:43

Embedded Tutorial I

Organizers: Lei He, X. Sharon Hu
Moderators: Anirudh Devgan

Design for Manufacturability

Vijay Pitchumani, Intel Corp.

11:43-12:20

Regular Talks
Organizers: Zhiping Yu, Kenji Nishi
Moderators: Zhiping Yu

1D-2
11:43-12:08

ESDZapper: A New Layout-level Verification Tool for Finding Critical Discharging Path Under ESD Stress

Rouying Zhan, Haolu Xie, Haigang Feng, Albert Wang (Illinois Institute of Technology)

1D-3s
12:08-12:20

A New Dissection Method for Model Based Frugal OPC

Xiaolang Yan, Ye Chen, Zheng Shi, Yue Ma (Zhejiang University)

Wednesday, January 19, Time 10:30-12:10

Session 1E: Clock, Power Grid and Thermal Analysis and Optimization

Organizers: Huazhong Yang, Sheldon X.-D. Tan

Moderators: Xiaodong Yang, Eli Chiprout

Room: Tang Room (FL.2)

1E-1
10:30-10:55

Fast Computation of the Temperature Distribution in VLSI Chips Using the Discrete Cosine Transform and Table Look-up
Yong Zhan, Sachin S. Sapatnekar (University of Minnesota)

1E-2
10:55-11:20

Analysis of Buffered Hybrid Structured Clock Networks
Yi Zou, Qiang Zhou, Yici Cai, Xianlong Hong (Tsinghua University, Beijing), Sheldon X.-D. Tan (UCR)

1E-3s
11:20-11:33

Clock Network Minimization Methodology Based On Incremental Placement
Liang Huang, Yici Cai, Qiang Zhou, Xianlong Hong (Tsinghua University, Beijing), Jiang Hu (Texas A&M University), Yongqiang Lu (Tsinghua University, Beijing)

1E-4s
11:33-11:45

A Multi-Level Transmission Line Network Approach for Multi-Giga Hertz Clock Distribution
Hongyu Chen, C. K. Cheng (UCSD)

1E-5s
11:45-11:58

Gibbs Sampling in Power Grid Analysis
Zhixin Tian, Huazhong Yang, Rong Luo (Tsinghua University, Beijing)

1E-6s
11:58-12:10

A Wideband Hierarchical Circuit Reduction for Massively Coupled Interconnects
Hao Yu, Lei He (UCLA), Zhenyu Qi (UCR), Sheldon X.-D. Tan (UCR)

Wednesday, January 19, Time 10:30-12:10

Poster Session I (25 Boards)

PI-1: Modeling SystemC Design in UML and Automatic Code Generation
Chen Xi, Lu JianHua, Zhou ZuCheng (Tsinghua University, Beijing), Shang YaoHui (Legible Logic Co.Ltd)

PI-2: Enabling RTOS Simulation Modeling in a System Level Design Language
M. AbdElSalam Hassan, Keishi Sakanushi, Yoshinori Takeuchi, Masaharu Imai (Osaka University)

PI-3: A System-level Framework for Evaluating Area/Performance/Power Trade-offs of VLIW-based Embedded Systems
Giuseppe Ascia, Vincenzo Catania, Maurizio Palesi，Davide Patti (University of Catania)

PI-4: Multi-Metric and Multi-Entity Characterization of Applications for Early System Design Exploration
Lukai Cai, Andreas Gerstlauer, Daniel. Gajski (UCI)

PI-5: An Integrated Performance and Power Model For Superscalar Processor Designs
Yongxin Zhu, Weng-Fai Wong, Stefan Andrei (National University of Singapore)

PI-6: Hierarchical Task Scheduler for Interleaving Subtasks on Heterogeneous Multiprocessor Platforms
Zhe Ma, Francky Cathoor, Johan Vounckx (IMEC/DESICS)

PI-7: A Flexible Framework for Communication Evaluation in SoC Design
Praveen G Kalla, X. Sharon Hu (University of Notre Dame), Joerg Henkel (University of Karlsruhe)

PI-8: Feasibility Analysis of Messages for On-chip Networks Using Wormhole Routing
Zhonghai Lu, Axel Jantsch, Ingo Sander (Royal Institute of Technology)

PI-9: A Clustering Technique to Optimize Hardware/Software Synchronization
Junyu Peng, Samar Abdi, Daniel Gajski (UCI)

PI-10: Using Abstract CPU Subsystem Simulation Model for High Level HW/SW Architecture Exploration
Aimen Bouchhima, Iuliana Bacivarov, Wassim Youssef, Marius Bonaciu, Ahmed A. Jerraya (TIMA laboratory)

PI-11: On Combining Iteration Space Tiling with Data Space Tiling for Scratch-Pad Memory Systems
Chunhui Zhang, Fadi Kurdahi (UCI)

PI-12: REMIC – Design of a Reactive Embedded Microprocessor Core
Zoran Salcic, Dong Hui, Partha Roop, Morteza Biglari-Abhari (Auckland University)

PI-13: Online Hardware/Software Partitioning in Networked Embedded Systems
Thilo Streichert, Christian Haubelt, Juergen Teich (University of Erlangen-Nuremberg)

PI-14: Comparing High-level Modeling Approaches for Embedded System Design
Lisane Brisolara (UFRGS), Leandro Becker (UFSC), Luigi Carro, Flávio Wagner, Carlos E. Pereira, Ricardo Reis (UFRGS)

PI-15: Deriving a New Efficient Algorithm for Min-Period Retiming
Hai Zhou (Northwestern University)

PI-16: K-Disjointness Paradigm with Application to Symmetry Detection for Incompletely Specified Functions
Kuo-Hua Wang, Jia-Hung Chen (Fu Jen Catholic University)

PI-17: Logic Optimization Using Rule-Based Randomized Search
Petra Farm, Elena Dubrova (Royal Institute of Technology), Andreas Kuehlmann (Cadence Berkeley Labs)

PI-18: Fast Synthesis of Exact Minimal Reversible Circuits using Group Theory
Guowu Yang, Xiaoyu Song, William N.N. Hung, Marek A. Perkowski (Portland State University)

PI-19: Design and Design Automation of Rectification Logic for Engineering Change
Cheng-Hung Lin, Yung-Chang Huang, Shih-Chieh Chang (Tsing Hua University, Hsin-Chu), Wen-Ben Jone (University of Cincinnati)

PI-20: Power Minimization for Dynamic PLAs
Tzyy-Kuen Tien (Southern Taiwan Universithy of Technology), Chih-Sheh Tsai (TSMC), Shih-Chieh Chang (Tsing Hua University, Hsin-Chu), Chingwei Yeh (Chung Cheng University)

PI-21: Integrated Algorithmic Logical and Physical Design of Integer Multiplier
Shuo Zhou, Bo Yao, Jian-Hua Liu, C. K. Cheng (UCSD)

PI-22: Arrival Time Aware Scheduling to Minimize Clock Cycle Length
R. Ruiz-Sautua, M. C. Molina, J. M. Mendías, R. Hermida (Universidad Complutense de Madrid,)

PI-23: Efficient Synthesis of Speed-Independent Combinational Logic Circuits
W. B. Toms, D. A. Edwards (University of Manchester)

PI-24: A Practical Cut-Based Physical Retiming Algorithm for Field Programmable Gate Arrays
Peter Suaris, Dongsheng Wang, Nan-Chi Chou (Mentor Graphics Corporation)

PI-25: BDD-based Two Variable Sharing Extraction
Dennis Wu, Jianwen Zhu (University of Toronto)

Wednesday, January 19, 14:00-15:40

Wednesday, January 19, Time 14:00-15:40

Session 2A: Routing and Interconnects

Organizers: Tong Jing, Martin D. F. Wong, Cheng-Kok Koh, Takeshi Yoshimura

Moderators: Martin D. F. Wong, Tong Jing

Room: Zhong Hua 1 (FL.3)

2A-1
14:00-14:25

A Min-area Solution to Performance and RLC Crosstalk Driven Global Routing Problem
Tong Jing, Ling Zhang, Jinghong Liang, Jingyu Xu, Xianlong Hong (Tsinghua University, Beijing), Jinjun Xiong, Lei He (UCLA)

2A-2 **14:25-14:50**
Thermal-Driven Multilevel Routing for 3-D ICs
Jason Cong, Yan Zhang (UCLA)

2A-3 **14:50-15:15**
Wave-Pipelined On-Chip Global Interconnect
Lizheng Zhang, Yuhen Hu (University of Wisconsin, Madison), Charlie ChungPing Chen (Taiwan University)

2A-4 **15:15-15:40**
Evaluation of On-Chip Transmission Line Interconnect Using Wire Length Distribution
Junpei Inoue, Hiroyuki Ito, Shinichiro Gomi, Takanori Kyogoku, Takumi Uezono, Kenichi Okada, Kazuya Masu (Tokyo Institute of Technology)

Wednesday, January 19, Time 14:00-15:40
Session 2B: System Level Modeling and Embedded Software
Organizers: David Chen, Soonhoi Ha, S. K. Nandy
Moderators: Tim Tuan, S. K. Nandy
Room: Zhong Hua 2 (FL.3)

2B-1 **14:00-14:25**
A Formalism for Functionality Preserving System Level Transformations
Samar Abdi, Daniel Gajski (UCI)

2B-2 **14:25-14:50**
Embedded Software Generation from System Level Specification for Multi-tasking Embedded Systems
Kiseun Kwon, YoungMin Yi, DoHyung Kim, SoonHoi Ha (Seoul National University)

2B-3 **14:50-15:15**
Scheduler Implementation in MP SoC Design
Youngchul Cho (Seoul National University and TIMA Laboratory), Sungjoo Yoo (Samsung Electronics), Kiyoung Choi (Seoul National University), Nacer-Eddine Zergainoh, Ahmed Amine Jerraya (TIMA Laboratory)

2B-4s **15:15-15:28**
Optimizing Embedded Applications Using Programmer-Inserted Hints
Guilin Chen, Mahmut Kandemir (The Pennsylvania State University)

2B-5s **15:28-15:40**
Static Analysis and Automatic Code Synthesis of flexible FSM Model
Dohyung Kim, Soonhoi Ha (Seoul National University)

Wednesday, January 19, Time 14:00-15:40
Session 2C: Test and DFT (2)
Organizers: Xiaowei Li, Terumine Hayashi
Moderators: Kwang-Ting (Tim) Cheng, Shiyi Xu
Room: Han Room 1 (FL.3)

2C-1 **14:00-14:25**
Constraint Extraction for Pseudo- Functional Scan-based Delay Testing
Yung-Chieh Lin, Feng Lu, Kai Yang, Kwang-Ting Cheng (UCSB)

2C-2 **14:25-14:50**
Bridging Fault Detection in Double Fixed-Polarity Reed-Muller (DFPRM) PLA
Hafizur Rahaman (Bengal Eng. & Sci. University, Shibpur), Debesh K. Das (Jadavpur University)

2C-3 **14:50-15:15**
Propagation Delay Fault: A New Fault Model to Test Delay Faults
Xijiang Lin, Janusz Rajski (Mentor Graphics Corp.)

2C-4s **15:15-15:28**
Oscillation Ring Based Interconnect Test Scheme for SOC
Katherine Shu-Min Li, Chung Len Lee, Chauchin Su, Jwu E Chen (Chiao Tung University)

2C-5s **15:28-15:40**
Bridging Fault Testability of BDD Circuits
Junhao Shi, Görschwin Fey, Rolf Drechsler (University of Bremen)

Wednesday, January 19, Time 14:00-15:52

Session 2D: TCAD

Organizers: Zhiping Yu, Kenji Nishi

Moderators: Kenji Nishi, Changhong Dai

Room: Han Room 2 (FL.3)

2D-1
14:00-14:25
Yield Driven Gate Sizing for Coupling-Noise Reduction under Uncertainty
Debjit Sinha, Hai Zhou (Northwestern University)

2D-2
14:25-14:50
Maze Routing with OPC Consideration
Yun-Ru Wu, Ming-Chao Tsai，Ting-Chi Wang (Tsing Hua University, Hsin-Chu)

2D-3s
14:50-15:03
Towards Automatic Parameter Extraction for Surface-Potential-Based MOSFET Models with the Genetic Algorithm
Masahiro Murakawa (AIST), Mitiko Miura-Mattausch (Hiroshima University), Tetsuya Higuchi (AIST)

2D-4s
15:03-15:15
Substrate Resistance Extraction with Direct Boundary Element Method
Xiren Wang, Wenjian Yu, Zeyi Wang (Tsinghua University, Beijing)

2D-5s
15:15-15:28
An Efficient Combinationality Check Technique for the Synthesis of Cyclic Combinational Circuits
Vineet Agarwal, Navneeth Kankani, Ravishankar Rao, Sarvesh Bhardwaj, Janet Wang (University of Arizona)

2D-6s
15:28-15:40
Library Cell Layout with Alt-PSM Compliance and Composability
Ke Cao, Puneet Dhawan, Jiang Hu (Texas A&M University)

2D-7s
15:40-15:52
Forward Discrete Probability Propagation Method for Device Performance Characterization under Process Variations
Rasit Onur Topaloglu，Alex Orailoglu (UCSD)

Wednesday, January 19, Time 14:00-15:40

Session 2E: Simulation and Modeling techniques for RF/Analog Circuits

Organizers: Huazhong Yang, Sheldon X.-D. Tan

Moderators: Jaijeet Roychowdhury, Yici Cai

Room: Tang Room (FL.2)

2E-1
14:00-14:25
Wideband Modeling of RF/Analog Circuits via Hierarchical Multi-Point Model Order Reduction
Zhenyu Qi，Sheldon X.-D. Tan (UCR)，Hou Yu, Lei He (UCLA)

2E-2
14:25-14:50
Efficient Symbolic Sensitivity Analysis of Analog Circuits using Element-Coefficient Diagrams
Huiying Yang，Mukesh Ranjan (University of Cincinnati)，Wim Verhaegen (Katholieke University Leuven), Mengmeng Ding，Ranga Vemuri (University of Cincinnati)，Geoges Gielen (Katholieke University Leuven)

2E-3s
14:50-15:03
A New Approach for Ring Oscillator Simulation Using the Harmonic Balance Method
Xiaochun Duan, Kartikeya Mayaram (Oregon State University)

2E-4s
15:03-15:15
Efficient Transient Simulation for Transistor-Level Analysis
Zhengyong Zhu (UCSD), Khosro Rouz, Manjit Borah (Fastrack Design, Inc.), C. K. Cheng (UCSD), Ernest S. Kuh (UCB)

2E-5s
15:15-15:28
Block SAPOR: Block Second-Order Arnoldi Method for Passive Order Reduction of Multi-Input Multi-Output RCS Interconnect Circuits
Bang Liu, Xuan Zeng, Feng Yang Su, Jun Tao (Fudan University), Zhaojun Bai (UCD), Charles Chiang (Synopsys, Inc.), Dian Zhou (University of Texas at Dallas)

2E-6s
15:28-15:40

Block-Based Statistical Timing Analysis with Extended Canonical Timing Model
Lizheng Zhang, Yuhen Hu (University of Wisconsin, Madison,), Charlie Chung-Ping Chen (Taiwan University)

Wednesday, January 19, Time 14:00-15:40
Poster Session II (25 Boards)

PII-1: Supporting Sequential Assumptions in Hybrid Verification
Ed Cerny, Ashvin Dsouza, Kevin Harer, Pei-Hsin Ho, Tony Ma (Synopsys)

PII-2: Automatic Functional Test Program Generation for Microprocessor Verification
Tun Li, Dan Zhu, Lei Liang, Yang Guo, SiKun Li (National University of Defense Technology)

PII-3: Forward Symbolic Model Checking for Real Time Systems
Georgios Logothetis (University of Karlsruhe)

PII-4: Validating the Result of a Quantified Boolean Formula(QBF) Solver: Theory and Practice
Yinlei Yu, Sharad Malik (Princeton University)

PII-5: Priority Directed Test Generation for Functional Verification using Neural Networks
Hao Shen, Yuzhuo Fu (Shanghai Jiaotong University)

PII-6: Comparison of Schemes for Encoding Unobservability in Translation to SAT
Miroslav N. Velev (Carnegie Mellon University)

PII-7: Implication of Assertion Graphs in GSTE
Guowu Yang (Portland State University), Jin Yang, William N. N. Hung (Intel Corp.), Xiaoyu Song (Portland State University)

PII-8: XTW, a Parallel and Distributed Logic Simulator
Qing Xu, Carl Tropper (McGill University)

PII-9: Comprehensive Frequency Dependent Interconnect Extraction and Evaluation Methodology
Rong Jiang (University of Wisconsin, Madison), Charlie Chung-Ping Chen (Taiwan University)

PII-10: On-Chip Thermal Gradient Analysis and Temperature Flattening for Soc Design
Takashi Sato (Renesas Technology), Junji Ichimiya (Richo), Nobuto Ono (Jedat Innovation), Kotaro Hachiya (NEC Electronics), Masanori Hashimoto (Osaka University)

PII-11: Return Path Selection for Loop RL Extraction
Akira Tsuchiya (Kyoto University), Masanori Hashimoto (Osaka University), Hidetoshi Onodera (Kyoto University)

PII-12: Delay Extraction Based Closed-Form Spice Compatible Passive Macromodels for Distributed Transmission Line Interconnects
Natalie Nakhla, Ram Achar, Michel Nakhla (Carleton University), Anestis Dounavis (University of Western Ontario)

PII-13: Vector Extraction for Average Total Power Estimation
Yongjun Xu, Jinghua Chen (Institute of Computing Technology, Chinese Academy of Sciences), Zuying Luo (Tsinghua University, Beijing), Xiaowei Li (Institute of Computing Technology, Chinese Academy of Sciences)

PII-14: Relaxed Hierarchical Power/Ground Grid Analysis
Yici Cai, Zhu Pan (Tsinghua University, Beijing), Sheldon X.-D. Tan (UCR), Zuying Luo, Xianlong Hong (Tsinghua University, Beijing), Wenting Hou, Lifeng Wu (Cadence Design Systems)

PII-15: Sleep Transistor Sizing Using Timing Criticality and Temporal Currents
Anand Ramalingam, Bin Zhang (The University of Texas, Austin), Anirudh Devgan (Austin Research Laboratory, IBM Research), David Z. Pan (The University of Texas, Austin)

PII-16: Timing Analysis Considering Temporal Supply Voltage Fluctuation
Masanori Hashimoto (Osaka University), Junji Yamaguchi, Takashi Sato, Hidetoshi Onodera (Kyoto University)

PII-17: Fast, and Accurate MOS Table Model for Circuit Simulation Using an Unstructured Grid and Preserving Monotonicity
G. Peter Fang, David C. Yeh, David Zweidinger, Lawrence A. Arledge, Vinod Gupta (Texas Instruments, Inc.)

PII-18: Congestion Prediction in Floorplanning
Chiu-wing Sham, Evangeline F. Y. Young (The Chinese University of Hong Kong)

PII-19: CMP Aware Shuttle Mask Floorplanning
Gang Xu (University of Texas at Austin), Ruiqi Tian (Freescale Semiconductor), David Z. Pan (University of Texas at Austin), Martin D. F. Wong (UIUC)

PII-20: An Improved P-admissible Floorplan Representation Based on Corner Block List
Renshen Wang, Sheqin Dong, Xianlong Hong (Tsinghua University, Beijing)

PII-21: Fast Floorplanning by Look-Ahead Enabled Recursive Bipartitioning
Jason Cong, Michail Romesis, Joseph R. Shinnerl (UCLA)

PII-22: LFF Algorithm for Heterogeneous FPGA Floorplanning
Jun Yuan, Sheqin Dong, Xianlong Hong (Tsinghua University, Beijing), Yu-Liang Wu (Chinese University of Hong Kong)

PII-23: Placement for Configurable Dataflow Architecture
Mongkol Ekpanyapong, Michael Healy, Sung Kyu Lim (Georgia Institute of Technology)

PII-24: Wire Congestion And Thermal Aware 3D Global Placement
Karthik Balakrishnan, Vidit Nanda, Siddharth Easwar, Sung Kyu Lim (Georgia Institute of Technology)

PII-25: Placement with Symmetry Constraints for Analog Layout Design Using TCG-S
Jai-Ming Lin (RealTek Semiconductor Corp.), Guang-Ming Wu (Nan-Hua University), Yao-Wen Chang (Taiwan University), Jen-Hui Chuang (Chiao Tung University)

Wednesday, January 19, 16:10-17:50

Wednesday, January 19, Time 16:10-17:50
Session 3A: Logic Synthesis
Organizers: Jinian Bian, Jianwen Zhu
Moderators: Jianwen Zhu, Sikun Li
Room: Zhong Hua 1 (FL.3)

3A-1
16:10-16:35
FSM Re-Engineering and Its Application in Low Power State Encoding
Lin Yuan, Gang Qu (University of Maryland), Tiziano Villa (University of Udine), Alberto Sangiovanni-Vincentelli (UCB)

3A-2
16:35-17:00
Post-Layout Logic Duplication for Synthesis of Domino Circuits with Complex Gates
Aiqun Cao, Ruibing Lu (Synopsys), Cheng-Kok Koh (Purdue University)

3A-3
17:00-17:25
Detecting Support-Reducing Bound Sets using Two-Cofactor Symmetries
Jin S. Zhang, Malgorzata Chrzanowska-Jeske (Portland State University), Alan Mishchenko (UCB), Jerry R. Burch (Synopsys)

3A-4s
17:25-17:37
Synthesis of Quantum Logic Circuits
Vivek V. Shende (University of Michigan), Stephen S. Bullock (National Institute of Standards and Technology), Igor L. Markov (University of Michigan)

3A-5s
17:37-17:50
STACCATO: Disjoint Support Decompositions from BDDs through Symbolic Kernels
Stephen Michael Plaza , Valeria Bertacco (University of Michigan)

Wednesday, January 19, Time 16:10-17:50

Session 3B: System Level Architecture Design

Organizers: David Chen, Soonhoi Ha, S. K. Nandy

Moderators: Sreedhar Natarrajan, Soo-Ik Chae

Room: Zhong Hua 2 (FL.3)

3B-1
16:10-16:35
A Framework for Automated and Optimized ASIP Implementation Supporting Multiple Hardware Description Languages
Oliver Schliebusch, A. Chattopadhyay, D. Kammler, R. Leupers, H. Meyr (Aachen University of Technology), Tim Kogel (CoWare Inc.)

3B-2
16:35-17:00
A Processor Core Synthesis System in IP-based SoC Design
Naoki Tomono, Shuitsu Kohara, Jumpei Uchida, Yuichiro Miyaoka (Waseda University), Nozomu Togawa (University of Kitakyushu), Masao Yanagisawa, Tatsuo Ohtsuki (Waseda University)

3B-3
17:00-17:25
Speed and Voltage Selection for GALS Systems based on Voltage/Frequency Islands
Koushik Niyogi, Diana Marculescu (Carnegie Mellon University)

3B-4s
17:25-17:37
A System-Level Approach to Hardware Reconfigurable Systems
Christian Haubelt, Stephan Otto, Cornelia Grabbe, Jürgen Teich (University of Erlangen-Nuremberg)

3B-5s
17:37-17:50
High-level Synthesis for DSP Applications using Heterogeneous Functional Units
Zili Shao, Qingfeng Zhuge, Chun Xue (University of Texas at Dallas), Bin Xiao (Hong Kong Polytechnic University), Edwin H.-M. Sha (University of Texas at Dallas)

Wednesday, January 19, Time 16:10-17:50

Session 3C: Test and Verification

Organizers: Xiaowei Li, Jin Yang

Moderators: Yinghua Min, Alan J. Hu

Room: Han Room 1 (FL.3)

3C-1
16:10-16:35
Evaluation of Statistical Delay Quality Model
Yasuo Sato, Shuji Hamada, Toshiyuki Maeda, Atsuo Takatori (Semiconductor Technology Academic Research Center), Seiji Kajihara (Kyushu Institute of Technology)

3C-2
16:35-17:00
Fault Tolerant Nanoelectronic Processor Architectures
Wenjing Rao, Alex Orailoglu (UCSD), Ramesh Karri (Polytechnic University)

3C-3
17:00-17:25
An Efficient Control-Oriented Coverage Metric
Shireesh Verma, Kiran Ramineni, Ian G. Harris (UCI)

3C-4s
17:25-17:37
An Observability Measure to Enhance Statement Coverage Metric for Proper Evaluation of Verification Completeness
Tai-Ying Jiang, Chien-Nan Jimmy Liu, Jing-Yang Jou (Chiao Tung University)

3C-5s
17:37-17:50
Tightly Integrate Dynamic Verification With Formal Verification: A GSTE Based Approach
Jin Yang, Avi Puder (Intel Corp.)

Wednesday, January 19, Time 16:10-17:50

Session 3D-3E: (Special Session)

Room: Han Room 3 (FL.3)

3D-3E-1
16:10-17:50

(Panel I): Who Is Responsible for the Design for Manufacturability Issues in the Era of Nano-Technologies?

Organizers: C. K. Cheng (UCSD) and Steve Lin (Tsing Hua University, Hsin-Chu)

Thursday, January 20, 9:00-10:00

Thursday, January 20, Time 9:00-10:00

Keynote Address II

Room: Imperial Hall 1-2 (FL.2)

Moderator: Jason Cong

K-2
9:00-10:00

Silicon Compilation: The Answer to Reducing IC Development Costs

Rajeev Madhavan (Chairman and CEO of Magma Design Automation)

Thursday, January 20, 10:30-12:10

Thursday, January 20, Time 10:30-12:10

Session 4A: Placement Techniques

Organizers: Tong Jing, Martin D. F. Wong, Cheng- Kok Koh, Takeshi Yoshimura

Moderators: Xianlong Hong, Ting-Chi Wang

Room: Zhong Hua 1 (FL.3)

4A-1
10:30-10:55

On Structure and Suboptimality in Placement

Satoshi Ono, Patrick H. Madden (Binghamton/U. Kitakyushu)

4A-2
10:55-11:20

Optimal Placement by Branch-and-Price

Pradeep Ramachandaran, Ameya R. Agnihotri, Satoshi Ono, Purush Damodaran, Patrick H. Madden (Binghamton/U. Kitakyushu)

4A-3
11:20-11:45

Detailed Placement for Improved Depth of Focus and CD Control

Puneet Gupta, Andrew B. Kahng (Blaze DFM, Inc.), Chul-Hong Park (UCSD)

4A-4
11:45-12:10

Floorplan Management: Incremental Placement for Gate Sizing and Buffer Insertion

Chen Li, Cheng-Kok Koh (Purdue University), Patrick H. Madden (Binghamton University)

Thursday, January 20, Time 10:30-12:10

Session 4B: Security Processor Design

Organizers: Yihe Sun, Hoi-Jun Yoo, Takao Onoye

Moderators: Lorena Anghel, Steve Lin

Room: Zhong Hua 2 (FL.3)

4B-1
10:30-10:55

Low-Power Techniques for Network Security Processors

Yi-Ping You, Chun-Yen Tseng, Yu-Hui Huang, Po-Chiun Huang, TingTing Hwang, Sheng-Yu Hsu (Tsing Hua University, Hsin-Chu)

4B-2
10:55-11:20

A Configurable AES Processor for Enhanced Security

Chih-Pin Su, Chia-Lung Horng, Chih-Tsun Huang, Cheng-Wen Wu (Tsing Hua University, Hsin-Chu)

4B-3s
11:20-11:32

Power Estimation Starategies For A Low-Power Security Processor

Yen-Fong Lee, Shi-Yu Huang (Tsing Hua University, Hsin-Chu), Sheng-Yu Hsu, I-Ling Chen (Industrial Technological Research Institute), Cheng-Tao Shieh, Jian-Cheng Lin, Shih-Chieh Chang (Tsing Hua University, Hsin-Chu)

4B-4s
11:32-11:45

Design and Test of a Scalable Security Processor

Chih-Pin Su, Chen-Hsing Wang, Kuo-Liang Cheng, Chih-Tsun Huang, Cheng-Wen Wu (Tsing Hua University, Hsin-Chu)

4B-5s
11:45-11:57

System-level Design Space Exploration for Security Processor Prototyping in Analytical Approaches
Yung-Chia Lin, Chung-Wen Huang, Jenq-Kuen Lee (Tsing Hua Universuty, Hsin-Chu)

Thursday, January 20, Time 10:30-12:10
Session 4C: (Special Session) Embedded Tutorial II
Organizers: Lei He, X. Sharon Hu
Moderators: Lei He
Room: Han Room 1 (FL.3)

4C-1
10:30-12:10

Leakage Power: Trends, Analysis and Avoidance
David Blaauw, University of Michigan
Anirudh Devgan, IBM Research
Farid Najm, University of Toronto

Thursday, January 20, Time 10:30-12:10
Session 4D: (Special Session) CAD for Microarchitecture Designs
Organizers: Hannah Honghua Yang
Moderators: Hannah Honghua Yang
Room: Han Room 2 (FL.3)

4D-1
10:30-11:20

(Invited Talk) Challenges to Covering the High-level to Silicon Gap
Bill Grundmann (Intel Corp.)

4D-2
11:20-11:45

(Invited Paper) Opportunities and Challenges for Better Than Worst-Case Design
Todd Austin, Valeria Bertacco, David Blaauw, and Trevor Mudge (University of Michigan)

4D-3
11:45-12:10

(Invited Paper) Microarchitecture Evaluation With Floorplanning And Interconnect Pipelining
Ashok Jagannathan (UCLA), Hannah Yang, Kris Konigsfeld, Dan Milliron, Mosur Mohan (Intel Corp.), Michail Romesis, Glenn Reinman, and Jason Cong (UCLA)

Thursday, January 20, Time 10:30-12:10
Session 4E: Design Optimization for High- Performance Digital Circuits
Organizers: Huazhong Yang, Sheldon X.-D. Tan
Moderators: Eli Chiprout, Zheng Shi
Room: Tang Room (FL.2)

4E-1
10:30-10:55

Fast and Effective Gate-Sizing with Multiple-Vt Assignment using Generalized Lagrangian Relaxation
Hsinwei Chou (University of Wisconsin, Madison), Yuhao Wang (Incentia Design Systems, Inc.), Charlie Chung-Ping Chen (Taiwan University)

4E-2
10:55-11:20

Effective analytical delay model for transistor sizing
Zhaojun Wo, Israel Koren (University of Massachusetts, Amherst)

4E-3
11:20-11:45

Achieving Continuous V_t Performance in a Dual V_t Process
Kanak Agarwal, Dennis Sylvester, David Blaauw (University of Michigan), Anirudh Devgan (IBM Research)

4E-4
11:45-12:10

Runtime Leakage Minimization through Probability-Aware Dual-Vt or Dual-Tox Assignment
Dongwoo Lee, David Blaauw, Dennis Sylvester (University of Michigan)

Thursday, January 20, Time 10:30-12:10
Special Session: University Design Contest
Organizers: Xiaoyang Zeng, Makoto Ikeda, Lin Yang
Moderators: Xiaoyang Zeng, Makoto Ikeda, Lin Yang
Room: Ming Room 1 (FL.2)

DC-1
10:30-10:45

TERPS: The Embedded Reliable Processing System
Hongxia Wang, Samuel Rodriguez, Cagdas Dirik, Amol Gole, Vincent Chan, Bruce Jacob (University of Maryland)

DC-2
10:45-11:00

Amdrel: A Novel Low-Energy FPGA Architecture and Supporting Cad Tool Design Flow

D. Soudris (Democritus University of Thrace), S. Nikolaidis, S. Siskos (Aristotle University of Thessaloniki), K. Tatas, K. Siozios, G. Koutroumpezis (Democritus University of Thrace), N. Vasiliadis, V. Kalenteridis, H. Pournara, I. Pappas (Aristotle University of Thessaloniki), A. Thanailakis (Democritus University of Thrace)

DC-3
11:00-11:15

Standard *CMOS* Technology On-chip Inductors with *pn* Junctions Substrate Isolation

Hongyan Jian, Zhangwen Tang, Jie He, Jinglan He, Min Hao (Fudan University)

DC-4
11:15-11:30

A Bandwidth Efficient Subsampling-based Block Matching Architecture for Motion Estimation

Hao-Yun Chin, Chao-Chung Cheng, Yu-Kun Lin, and Tian-Sheuan Chang (Chiao Tung University)

DC-5
11:30-11:45

Design and Measurement of 6.4 Gbps 8:1 Multiplexer in 0.18um CMOS Process

Akinori Shinmyo, Masanori Hashimoto, Hidetoshi Onodera (Kyoto University)

DC-6
11:45-12:00

A Design of High Speed Double Precision Floating Point Adder Using Macro Modules

Chi Huang, Xinyu Wu, Jinmei Lai, Chengshou Sun, Gang Li (Fudan University)

DC-7

A Low-Power Video Segmentation LSI with Boundary-Active-Only Architecture

Takashi Morimoto, Osamu Kiriyama, Hidekazu Adachi, Zhaomin Zhu, Tetsushi Koide, and Hans Jürgen Mattausch (Hiroshima University)

DC-8

The Design and Implementation of a DVB Receiving Chip with PCI Interface

Xu Ningyi, Li Shaohua, Yu Wei, He Guanghui, Zhang Hao, Luo Fei, Zhou Zucheng (Tsinghua University, Beijing)

DC-9

Design and Implementation of an SDH High-Speed Switch

Dehui Zhang, Quanliang Zhao, Jungang Han (Xi'an Institute of Post and Telecommunications)

DC-10

Design of Vehicle Position Tracking System Using Short Message Services and its Implementation on FPGA

Arias Tanti Hapsari, Eniman Y Syamsyuddin (Bandung Institute of Technology), Imron Pramana (PT Elektrindodaya Pakarnusa)

DC-11

Design of A 2.4-GHz integrated Frequency Synthesizer

Fei Wang, Jianyu Zhang, Xuan Wang, Jinmei Lai, Chengshou Sun (Fudan University)

DC-12

An Improved Test Access Mechanism Structure and Optimization technique in System-on-Chip

Feng Jianhua, Long Jieyi, Xu Wenhua, Ye Hongfei (Peking University)

Thursday, January 20, Time 12:30-13:30

Ph. D. Forum

Room: Ming Room 1 (FL.2)

Thursday, January 20, Time 13:30-17:00

The 2nd International Workshop on Compact Modeling (IWCM'05) in Conjunction with ASP-DAC 2005

Room: Ming Room 1 (FL.2)

Thursday, January 20, 14:00-15:40

Thursday, January 20, Time 14:00-15:40
Session 5A: Floorplanning and Partitioning
Organizers: Tong Jing, Martin D. F. Wong, Cheng- Kok Koh, Takeshi Yoshimura
Moderators: Yao-Wen Chang, Yoji Kajitani
Room: Zhong Hua 1 (FL.3)

5A-1
14:00-14:25
Floorplan Design for 3-D VLSI Design
Lei Cheng, Liang Deng, Martin D. F. Wong (UIUC)

5A-2
14:25-14:50
Optimal Redistribution of White Space for Wire Length Minimization
Xiaoping Tang (IBM TJ Watson Research Lab), Ruiqi Tian (Freescale Semiconductor), Martin D. F. Wong (UIUC)

5A-3
14:50-15:15
Crowdedness-Balanced Multilevel Partitioning for Uniform Resource Utilization
Yongseok Cheon (Synopsys), Martin D. F. Wong (UIUC)

5A-4s
15:15-15:28
Partitioning and Placement for Buildable QCA Circuits
Ramprasad Ravichandran, Mike Niemier, Sung Kyu Lim (Georgia Institute of Technology)

5A-5s
15:28-15:40
PMP: Performance-Driven Multilevel Partitioning by Aggregating the Preferred Signal Directions of I/O Conduits
Chanseok Hwang, Massoud Pedram (University of Southern California)

Thursday, January 20, Time 14:00-15:40
Session 5B: (Special Session) Embedded Tutorial III
Organizers: Lei He, X. Sharon Hu
Moderators: Howard Chen, Lei He
Room: Zhong Hua 2 (FL.3)

5B-1
14:00-15:40
Designing Reliable Circuit in the Presence of Soft Errors
Vijaykrishnan Narayanan, Yuan Xie, and Mary Jane Irwin (Pennsylvania State University)

Thursday, January 20, Time 14:00-15:40
Session 5C: Advances in SAT Technology and Application
Organizers: Jin Yang, Yunshan Zhu, Alan J. Hu
Moderators: Masahiro Fujita, Jeremy Levitt
Room: Han Room 1 (FL.3)

5C-1
14:00-14:25
MUP: A Minimal Unsatisfiability Prover
Jinbo Huang (UCLA)

5C-2
14:25-14:50
Integration of Supercubing and Learning in a SAT Solver
Domagoj Babic, Alan J. Hu (University of British Columbia)

5C-3
14:50-15:15
Dynamic Symmetry-Breaking for Improved Boolean Optimization
Fadi A. Aloul, Arathi Ramani, Igor L. Markov, Karem A. Sakallah (University of Michigan)

5C-4s
15:15-15:28
A Fast Counterexample Minimization Approach with Refutation Analysis and Incremental SAT
Shengyu Shen, Ying Qin, SiKun Li (National University of Defense Technology)

5C-5s
15:28-15:40
Sequential Equivalence Checking Using Cuts
Wei Huang, Pushan Tang, Min Ding (Fudan University)

Thursday, January 20, Time 14:00-15:40

Session 5D: Analysis and Simulation Techniques

Organizers: Xuan Zeng, Albert Wang, Koichiro Mashiko

Moderators: Richard Shi, Koichiro Mashiko

Room: Han Room 2 (FL.3)

5D-1
14:00-14:25
Fast PLL Simulation Using Nonlinear VCO Macromodels for Accurate Prediction of Jitter and Cycle-Slipping due to Loop Non-idealities and Supply Noise
Xiaolue Lai, Yayun Wan, Jaijeet Roychowdhury (University of Minnesota)

5D-2
14:25-14:50
Hierarchical Analysis of Process Variation for Mixed-Signal Systems
Fang Liu, Sule Ozev (Duke University)

5D-3
14:50-15:15
A Novel wavelet-based Method for Noise Analysis of Nonlinear Circuits
Xuan Zeng, Bang Liu, Jun Tao (Fudan University), Charles Chiang (Synopsys), Dian Zhou (Fudan University)

5D-4
15:15-15:40
An Error-Driven Adaptive Grid Refinement Algorithm for Automatic Generation of Analog Circuit Performance Macromodels
Mengmeng Ding, Glenn Wolfe, Ranga Vemuri (University of Cincinnati)

Thursday, January 20, Time 14:00-15:40

Session 5E: Interconnect Modeling and Analysis and System Level Design Methodology

Organizers: Huazhong Yang, David Chen

Moderators: Charlie Chung-Ping Chen, Yichi Cai

Room: Tang Room (FL.2)

5E-1
14:00-14:25
Partial Reluctance Based Circuit Simulation Is Efficient and Stable
Yu Du, Wayne Dai (UCSC)

5E-2
14:25-14:50
SAGA: Synthesis Technique for Guaranteed Throughput NoC Architectures
Krishnan Srinivasan, Karam S. Chatha (Arizona State University)

5E-3s
14:50-15:03
Automated Throughput-driven Synthesis of Bus-based Communication Architectures
Sudeep Pasricha, Nikil Dutt (UCI), Mohamed Ben-Romdhane (Conexant Systems Inc)

5E-4s
15:03-15:15
Simulation Acceleration of Transaction-Level Models for SoC with RTL sub-blocks
Jae-Gon Lee (Korea Advanced Institute of Science and Technology), Wooseung Yang, Young-Su Kwon (Dynalith Systems Co., Ltd.), Young-Il Kim, Chong-Min Kyung (Korea Advanced Institute of Science and Technology)

5E-5s
15:15-15:27
Statistical Modeling of Cross-Coupling Effects in VLSI Interconnects.
Mridul Agarwal (Indian Institute of Technology), Kanak Agarwal, Dennis Sylvester, David Blaauw (University of Michigan, Ann Arbor)

5E-6s
15:27-15:40
Compact and Stable Modeling of Partial Inductance and Reluctance Matrices
Hong Li, Venkataramanan Balakrishnan, Cheng-Kok Koh (Purdue Universtiy), Guoan Zhong (Magma Design Automation)

Thursday, January 20, Time 14:00-15:40

Poster Session III (25 Boards)

PIII-1: An LP-Based Methodology for Improved Timing-Driven Placement
Qingzhou Wang, John Lillis, Shubankar Sanyal (University of Illinois at Chicago)

PIII-2: Placement Stability Metrics
Chuck J. Alpert, Gi-joon Nam, Paul Villarribua, Mehmet C. Yildiz (IBM)

PIII-3: Redundant-Via Enhanced Maze Routing for Yield Improvement
Gang Xu (University of Texas at Austin), Li-Da Huang (Texas Instruments), David Z. Pan (University of Texas at Austin), Martin D. F. Wong (UIUC)

PIII-4: Interconnect Estimation without Packing via ACG Floorplans
Jia Wang, Hai Zhou (Northwestern University)

PIII-5: Timing Driven Track Routing Considering Coupling Capacitance
Di Wu, Jiang Hu (Texas A&M University), Min Zhao (Freescale Semiconductor), Rabi Mahapatra (Texas A&M University)

PIII-6: Multilevel Full-Chip Gridless Routing Considering Optical Proximity Correction
Tai-Chen Chen, Yao-Wen Chang (Taiwan University)

PIII-7: Improving the Scalability of SAMBA Bus Architecture
Ruibing Lu, Aiqun Cao (Synopsys), Cheng-Kok Koh (Purdue University)

PIII-8: Process-Variation Robust and Low-Power Zero-Skew Buffered Clock-Tree Synthesis Using Projected Scan-Line Sampling
Jeng-Liang Tsai (University of Wisconsin, Madison), Charlie Chung-Ping Chen (Taiwan University)

PIII-9: Register-Transfer Level Functional Scan for Hierarchical Designs
Ho Fai Ko, Qiang Xu, Nicola Nicolici (McMaster University)

PIII-10: Using Fault Model Relaxation to Diagnose Real Scan Chain Defects
Yu Huang, Wu-Tung Cheng (Mentor Graphics Corp.), Greg Crowell (LSI Logic Corp.)

PIII-11: A Retention-Aware Test Power Model for Embedded SRAM
Baosheng Wang, Josh Yang (University of British Columbia), Yuejian Wu (Nortel Networks Limited), André Ivanov (University of British Columbia)

PIII-12: On-Chip Accumulated Jitter Measurement for Phase-Locked Loops
Chih-Feng Li, Shao-Sheng Yang, Tsin-Yuan Chang (Tsing Hua University, Hsin-Chu)

PIII-13: SoC Test Scheduling Using the B*-Tree Based Floorplanning Technique
Jen-Yi Wuu, Tung-Chieh Chen, Yao-Wen Chang (Taiwan University)

PIII-14: Fault Tolerant Quantum Cellular Array (QCA) Design using Triple Modular Redundancy with Shifted Operands
Tongquan Wei (Polytechnic University at Brooklyn), Kaijie Wu (UIC), Ramesh Karri (Polytechnic University at Brooklyn), Alex Orailoglu (UCSD)

PIII-15: Efficiently Generating Test Vectors with State Pruning
Ying Chen (University of Minnesota), Dennis Abts (Cray Inc.), David J. Lilja (University of Minnesota)

PIII-16: Cluster-based Detection of SEU-caused Errors in LUTs of SRAM-based FPGAs
E. Syam Sundar Reddy, Vikram Chandrasekhar, M. Sashikanth, V. Kamakoti (Indian Institute of Technology Madras), N. Vijaykrishnan (Pennsylvania State University)

PIII-17: Comprehensive Analysis and Optimization of CMOS LNA Noise Performance
Dong Feng, Bingxue Shi (Tsinghua University, Beijing)

PIII-18: An Analog Front-end IP for 13.56MHz RFID Interrogators
Jung-Hyun Cho, Suk-Byung Chai, Chung-Gi Song, Kyung-Won Min, Shiho Kim (Wonkwang University)

PIII-19: A Two-stage Genetic Algorithm Method for Optimization the ΣΔ Modulators
A. Zahabi, O. Shoaei, Y. Koolivand, P. Jabehdar-maralani (University of Tehran)

PIII-20: A Novel Differential VCO Circuit Design for USB Hub
Gong Qian, Yuan Guo-shun (Institute of Microelectronics, the Chinese Academy of Sciences)

PIII-21: Static Power Minimization in Current-Mode Circuits
M. S. Bhat, H. S. Jamadagni (Indian Institute of Science)

PIII-22: A Novel Transmitter for 1000Base-T Physical Transceiver
Yang Li, Zengyu Zheng, Junyan Ren, Junbiao Ding, Cheng Tao, Lian Li (Fudan University)

PIII-23: A novel Data Processing Circuit in High-Speed Serial Communication
Yongjian Tang, Lenian He, Xiaolang Yan (Zhejiang University)

PIII-24: A Monolithic CMOS L Band DAB Receiver
Ziqiang Wang, Baoyong Chi, Min Lin, Shuguang Han, Lu Liu, Jinke Yao, Zhihua Wang (Tsinghua University, Beijing)

PIII-25: A Bipolar IF Amplifier/RSSI for ASK Receiver
Yonggang Tao, Yongsheng Xu, Wei Jin, Hui Yu, Zongsheng Lai (East China Normal Unversity)

Thursday, January 20, 16:10-17:50

Thursday, January 20, Time 16:10-17:50
Session 6A: High-Level Synthesis
Organizers: Jinian Bian, Jianwen Zhu
Moderators: Fan Mo, Jinian Bian
Room: Zhong Hua 1 (FL.3)

6A-1
16:10-16:35
Scalable Interprocedural Register Allocation for High Level Synthesis
Rami Beidas, Jianwen Zhu (University of Toronto)

6A-2
16:35-17:00
Simultaneous Floorplanning and Resource Binding: A Probabilistic Approach
Azadeh Davoodi, Ankur Srivastava (University of Maryland College-Park)

6A-3
17:00-17:25
Reducing Hardware Complexity of Linear DSP Systems by Iteratively Eliminating Two-Term Common Subexpressions
Anup Hosangadi (UCSB), Farzan Fallah (Fujitsu Laboratories of America), Ryan Kastner (UCSB)

6A-4s
17:25-17:38
A Fast Algorithm for Finding Common Multiple-Vertex Dominators in Circuit Graphs
Rene Krenz, Elena Dubrova (Royal Institute of Technology)

Thursday, January 20, Time 16:10-17:50
Session 6B: Low Power
Organizers: Yihe Sun, Hoi-Jun Yoo, Takao Onoye
Moderators: Hai Zhou, Rob Roy
Room: Zhong Hua 2 (FL.3)

6B-1
16:10-16:35
Low-Power Domino Circuits using NMOS Pull-up on Off-critical Paths
Abdulkadir U. Diril, Yuvraj S. Dhillon, Abhijit Chatterjee (Georgia Institute of Technology), Adit D. Singh (Auburn University)

6B-2
16:35-17:00
Low-leakage Robust SRAM cell design for Sub-100nm Technologies
Shengqi Yang, Wayne Wolf (Princeton University), Wenping Wang (Peking University), N. Vijaykrishnan, Yuan Xie (Penn State University)

6B-3s
17:00-17:13
Studying Interactions between Prefetching and Cache Line Turnoff
Ismail Kadayif (Canakkale Onsekiz Mart University), Mahmut Kandemir, Guilin Chen (Pennsylvania State University)

6B-4s
17:13-17:25
The Development of High Performance FFT IP Cores through Hybrid Low Power Algorithmic Methodology
Wei Han, A. T. Erdogan, T. Arslan, and M. Hasan (University of Edinburgh)

6B-5s
17:25-17:38
Battery-Aware Instruction Generation for Embedded Processors
Newton Cheung, Sri Parameswaran (University of New South Wales), Joerg HEnkel (University of Karlsruhe)

6B-6s
17:38-17:50
A Variation-Aware Low-Power Coding Methodology for Tightly Coupled Buses
Masanori Muroyama, Kosuke Tarumi, Koji Makiyama, Hiroto Yasuura (Kyushu University)

Thursday, January 20, Time 16:10-17:50
Session 6C: Formal Verification: Theory and Practice
Organizers: Jin Yang, Yunshan Zhu, Alan J. Hu
Moderators: Karem A. Sakallah, Yuan Lu
Room: Han Room 1 (FL.3)

6C-1
16:10-16:35
Automatic Assume Guarantee Analysis for Assertion-Based Formal Verification
Dong Wang (Synopsys), Jeremy Levitt (Mentor Graphics Corp.)

6C-2
16:35-17:00
TED+: A Data Structure for Microprocessor Verification
Pejman Lotfi-Kamran, Mohammad Hosseinabady, Hamid Shojaei (University of Tehran), Mehran Massoumi (California State University), Zainalabedin Navabi (University of Tehran)

6C-3
17:00-17:25
Improved Boolean Function Hashing based on Multiple-Vertex Dominators
Rene Krenz, Elena Dubrova (Royal Institute of Technology)

6C-4s
17:25-17:38
Lower Bounds for Dynamic BDD Reordering
Rüdiger Ebendt, Rolf Drechsler (University of Bremen)

6C-5s
17:38-17:50
Partitioned Model Checking from Software Specifications
Xiushan Feng, Alan J. Hu (University of British Columbia), Jin Yang (Intel Corp.)

Thursday, January 20, Time 16:10-17:50
Session 6D-6E: (Special Session)
Room: Han Room 3 (FL.3)

6D-6E-1
16:10-17:50
(Panel II): Are We Ready for System- Level Synthesis?
Organizers: Jason Cong (UCLA), Tony Ma (Synopsys)

Friday, January 21, 9:00-10:00

Friday, January 21, Time 9:00-10:00
Keynote Address III
Room: Imperial Hall 1-2 (FL.2)
Moderator: Masaharu Imai

K-3
9:00-10:00
Design at the End of the Silicon Roadmap
Jan M. Rabaey (UCB)

Friday, January 21, 10:30-12:10

Friday, January 21, Time 10:30-12:10
Session 7A: Robust and Low-Power Clock Design
Organizers: Tong Jing, Martin D. F. Wong, Cheng-Kok Koh, Takeshi Yoshimura
Moderators: C. K. Cheng, Weiping Shi
Room: Zhong Hua 1 (FL.3)

7A-1
10:30-10:55
Register Placement for Low Power Clock Network
Yongqiang Lu (Tsinghua University, Beijing), C. N. Sze (Texas A&M University), Xianlong Hong, Qiang Zhou, Yici Cai, Liang Huang (Tsinghua University, Beijing), Jiang Hu (Texas A&M University)

7A-2
10:55-11:20
Skew Scheduling and Clock Routing for Improved Tolerance to Process Variations
Ganesh Venkataraman, C. N. Sze, Jiang Hu (Texas A&M University)

7A-3
11:20-11:45
Stability Analysis of Active Clock Deskewing Systems Using a Control Theoretic Approach
Vinil Varghess, Tom Chen, Peter Young (Colorado State University)

7A-4
11:45-12:10
Process Variation Robust Clock Tree Routing
Wai-Ching Douglas Lam, Cheng-Kok Koh (Purdue University)

Friday, January 21, Time 10:30-12:10
Session 7B: DSP
Organizers: Yihe Sun, Hoi-Jun Yoo, Takao Onoye
Moderators: Makoto IKEDA, Xiaoyang Zeng
Room: Zhong Hua 2 (FL.3)

7B-1
10:30-10:55
IP-Block-based Design Environment for High-Throughput VLSI Dedicated Digital Signal Processing Systems
Nacer-Eddine Zergainoh, Katalin Popovici, Ahmed Jerraya (TIMA Laboratory), Pascal Urard (STMicroelectronics)

7B-2
10:55-11:20
A Resource-shared VLIW Processor Architecture for Area-efficient On-chip Multiprocessing
Kazutoshi Kobayashi, Masao Aramoto, Yoichi Yuyama, Akihiko Higuchi, and Hidetoshi Onodera (Kyoto University)

7B-3s
11:20-11:32
An Efficient Deblocking Filter Architecture with 2-Dimensional Parallel Memory for H.264/AVC
Lingfeng Li, Satoshi Goto, Takeshi Ikenaga (Waseda University)

7B-4s
11:32-11:45
A New Register File Access Architecture for Software Pipelining in VLIW Processors
Yanjun Zhang, Hu He, Yihe Sun (Tsinghua University, Beijing)

7B-5s
11:45-11:57
A Fast VLSI Architecture for Full-Search Variable Block SizeMotion Estimation in MPEG-4 AVC/H.264
Minho Kim, Ingu Hwang, Soo-Ik Chae (Seoul National University)

7B-6s
11:57-12:10
Automatic Synthesis and Scheduling of Multirate DSP Algorithms
Ying Yi, Mark Milward, Sami Khawan, Ioannis Nousias, Tughrul Arslan (University of Edinburgh)

Friday, January 21, Time 10:30-12:10
Session 7C: Low Power and Special Purpose FPGAs
Organizers: Yu-Liang Wu, Yao-Wen Chang, Lei He
Moderators: Lei He, Yu-Liang Wu
Room: Han Room 1 (FL.3)

7C-1
10:30-10:55
A High Performance Synthesisable Unsymmetrical Reconfigurable Fabric For Heterogeneous Finite State Machines
Zhenyu Liu, Tughrul Arslan, Sami Khawam, Iain. Lindsay (University of Edinburgh)

7C-2
10:55-11:20
Routing Track Duplication with Fine-Grained Power-Gating for FPGA Interconnect Power Reduction
Yan Lin, Fei Li, Lei He (UCLA)

7C-3
11:20-11:45
Exploiting Temporal Idleness To Reduce Leakage Power in Programmable Architectures
Rajarshee P. Bharadwaj, Rajan Konar, Poras T. Balsara, Dinesh Bhatia (University of Texas at Dallas)

7C-4s
11:45-11:58
Methodology for High Level Estimation of FPGA Power Consumption
Vijay Degalahal (Pennsylvania State University), Tim Tuan (Xilinx Research Labs)

7C-5s
11:58-12:10
Leakage Control in FPGA Routing Fabric
Suresh Srinivasan, A. Gayasen, N.Vijaykrishnan (Pennsylvania State University), T. Tuan (Xilinx Research Labs)

Friday, January 21, Time 10:30-12:10
Session 7D: RF Circuit Design and Design Methodology
Organizers: Xuan Zeng, Albert Wang, Koichiro Mashiko
Moderators: Koichiro Mashiko, Wing Hung Ki
Room: Han Room 2 (FL.3)

7D-1
10:30-10:55
A 1GHz CMOS Fourth-Order Continuous-Time Bandpass Sigma Delta Modulator for RF receiver front end A/D conversion
K. Praveen Jayakar Thomas, Ram Singh Rana, Yong Lian (National University of Singapore)

7D-2s
10:55-11:08
An Elitist Distributed Particle Swarm Algorithm for RF IC Optimization
Min Chu and David J. Allstot (University of Washington)

7D-3s
11:08-11:20
Phase-Locked Loop Synthesis Using Hierarchical Divide-and-Conquer Multi- Optimization
Min Chu and David J. Allstot (University of Washington)

7D-4s
11:20-11:33
A 10Gbps Transmitter with Multi-Tap FIR Pre-Emphasis in 0.18µm CMOS Technology
Miao Li, Tad Kwasniewski (Carleton University), Shoujun Wang, Yuming Tao (ALTERA CO)

7D-5s
11:33-11:45
A Dynamic Reconfigurable RF Circuit Architecture
Kenichi Okada, Yoshiaki Yoshihara, Hirotaka Sugawara, Kazuya Masu (Tokyo Institute of Technology)

7D-6s
11:45-11:58
Prediction of LC-VCOs' Tuning Curves with Period Calculation Technique
Zhangwen Tang, Jie He, Hongyan Jian, Haiqing Zhang, Jie Zhang, Hao Min (Fudan University)

Friday, January 21, Time 10:30-12:10
Session 7E: Design Techniques in Embedded and Real-time System
Organizers: Jihua Chen, X. Sharon Hu, Chong-Min Kyung
Moderators: Soon-Hoi Ha, Chenglian Peng
Room: Tang Room (FL.2)

7E-1
10:30-10:55
Hardware/Software Partitioning for Platform-Based Design Methods
Zhihui Xiong, Sikun Li, Jihua Chen (National University of Defense Technology)

7E-2
10:55-11:20
Abstracting Functionality for Modular Performance Analysis of Hard Real- Time Systems
Ernesto Wandeler, Lothar Thiele (Swiss Federal Institute of Technology (ETH) Zurich)

7E-3
11:20-11:45
Optimizing Intra-Task Voltage Scheduling Using Data Flow Analysis
Dongkun Shin, Jihong Kim (Seoul National University)

7E-4s
11:45-11:58

FD-HGAC: A Hybrid Heuristic/Genetic Algorithm Hardware/Software Co-synthesis Framework with Fault Detection
John Conner, Yuan Xie, Mahmut Kandemir (The Pennsylvania State University), Robert Dick (Northwestern University), Greg Link (The Pennsylvania State University)

7E-5s
11:58-12:10

Compiler-Directed Selective Data Protection Against Soft Errors
G. Chen, M. Kandemir, M. J. Irwin (The Pennsylvania State University), G. Memik (Northwestern University)

Friday, January 21, 14:00-15:40

Friday, January 21, Time 14:00-15:40
Session 8A: Crosstalk Noise Avoidance and Power/Ground Network Optimization
Organizers: Tong Jing, Martin D. F. Wong, Cheng- Kok Koh, Takeshi Yoshimura
Moderators: David Z. Pan, Dennis Sylvester
Room: Zhong Hua 1 (FL.3)

8A-1
14:00-14:25

A Perturbation-aware Noise Convergence Methodology for High Frequency Microprocessors
Prashant Saxena, Kumar Lalgudi, Hans Greub (Intel Corp.), Janet Meiling Wang-roveda (University of Arizona)

8A-2
14:25-14:50

Successive Pad Assignment Algorithm to Optimize Number and Location of Power Supply Pad Using Incremental Matrix Inversion
Takashi Sato (Kyoto University), Masanori Hashimoto (Osaka University), Hidetoshi Onodera (Kyoto University)

8A-3
14:50-15:15

A Unified Transformational Approach for Reductions in Fault Vulnerability, Power, and Crosstalk Noise & Delay on Processor Buses
Raid Ayoub, Alex Orailoglu (UCSD)

8A-4s
15:15-15:28

VLSI On-Chip Power/Ground Network Optimization Considering Decap Leakage Currents
Jingjing Fu, Zuying Luo, Xianlong Hong, Yici Cai (Tsinghua University, Beijing), Sheldon X.-D. Tan (UCR), Zhu Pan (Tsinghua University, Beijing)

8A-5s
15:28-15:40

Probabilistic Congestion Model Considering Shielding for Crosstalk Reduction
Jinjun Xiong, Lei He (UCLA)

Friday, January 21, Time 14:00-15:40
Session 8B: Others in Leading Edge Designs
Organizers: Yihe Sun, Hoi-Jun Yoo, Takao Onoye
Moderators: Sheldon X.-D. Tan, Hai Zhou
Room: Zhong Hua 2 (FL.3)

8B-1
14:00-14:25

Customized On-Chip Memories for Embedded Chip Multiprocessors
O. Ozturk, M. Kandemir, G. Chen, M. J. Irwin (The Pennsylvania State University), M. Karakoy (Imperial College)

8B-2
14:25-14:50

Performance Driven Reliable Link Design for Networks on Chips
Rutuparna Ramesh Tamhankar (Sun Microsystems Inc), Srinivasan Murali, Giovanni De Micheli (Stanford University)

8B-3s
14:50-15:03

Dynamic Power Management using On Demand Paging for Networked Embedded Systems
Yuvraj Agarwal, Curt Schurgers, Rajesh Gupta (UCSD)

8B-4s
15:03-15:15

An FPGA Implementation of Low-Density Parity-Check Code Decoder with Multi-Rate Capability
Lei Yang, Manyuan Shen, Hui Liu, C.-J. Richard Shi (University of Washington)

8B-5s
15:15-15:27

Single-Track Asynchronous Pipeline Controller Design
Xiao Yong, Zhou Runde (Tsinghua University, Beijing)

8B-6s
15:27-15:40

Using Data Replication to Reduce Communication Energy on Chip Multiprocessors
M. Kandemir, G. Chen, F. Li (Penn State University), I. Demirkiran (Syracuse University)

Friday, January 21, Time 14:00-15:40
Session 8C: Synthesis for FPGAs
Organizers: Yu-Liang Wu, Yao-Wen Chang, Lei He
Moderators: Kia Bazargan, Evangeline F. Y. Young
Room: Han Room 1 (FL.3)

8C-1
14:00-14:25

Three-dimensional Place and Route for FPGAs
Cristinel Ababei, Hushrav Mogal, Kia Bazargan (University of Minnesota)

8C-2
14:25-14:50

Modern FPGA Constrained Placement
Wai-Kei Mak (Tsing Hua University, Hsin-Chu)

8C-3
14:50-15:15

Clustering Techniques for Coarse- grained, Antifuse FPGAs
Chang Woo Kang, Massoud Pedram (University of Southern California)

8C-4s
15:15-15:28

A Novel CLB Architecture and Circuit Packing Algorithm for Logic-Area Reduction in SRAM-based FPGAs
Vivek Garg, Vikram Chandrasekhar, M. Sashikanth, V. Kamakoti (Indian Institute of Technology, Madras.)

8C-5s
15:28-15:40

Resource Sharing in Pipelined CDFG Synthesis
Somsubhra Mondal, Seda Ogrenci Memik (Northwestern University)

Friday, January 21, Time 14:00-15:40
Session 8D: Analog Circuit Design
Organizers: Xuan Zeng, Albert Wang, Koichiro Mashiko
Moderators: Chris Verhoeven, Junyan Ren
Room: Han Room 2 (FL.3)

8D-1
14:00-14:25

A 2.4-GHz Linear-tuning CMOS LC Voltage-controlled Oscillator
Hong Zhang, GuiCan Chen, Ning Li (Xi'an Jiaotong University)

8D-2
14:25-14:50

Adiabatic CMOS Gate and Adiabatic Circuit Design for Low-Power Applications
Guoqiang Hang (Zhejiang University)

8D-3
14:50-15:15

An 11-bit 160-MS/s 1.35-V 10-mW D/A Converter Using Automated Device Sizing System
Osamu Matsumoto, Hisashi Harada, Yasuo Morimoto, Toshio Kumamoto, Takahiro Miki, Masao Hotta (Renesas Technology Corp.)

8D-4s
15:15-15:28

A Class D Audio Power Amplifier with High-Efficiency and Low-Distortion
Chen Hai, Wu Xiaobo (Zhejiang University)

8D-5s
15:28-15:40

Substrate Noise Modeling in Early Floorplanning of MS-SOCs
Grzegorz Blakiewicz, Marcin Jeske, Malgorzata Chrzanowska-Jeske, Jin S. Zhang (Portland State University)

Friday, January 21, Time 14:00-15:40

Session 8E: Low Power Design for Embedded and Real-time Systems

Organizers: Jihua Chen, X. Sharon Hu, Chong-Min Kyung

Moderators: Joerg Henkel, Jihua Chen

Room: Tang Room (FL.2)

8E-1
14:00-14:25
Instruction Scheduling of VLIW Architectures for Balanced Power Consumption
Shu Xiao, Edmund M-K. Lai (Nanyang Technological University)

8E-2
14:25-14:50
Power Minimization Techniques on Distributed Real-Time Systems by Global and Local Slack Management
Shaoxiong Hua, Gang Qu (University of Maryland)

8E-3
14:50-15:15
A Generalized Technique for Energy-efficient Operating Voltage Set-up in Dynamic Voltage Scaled Processors
Jaewon Seo (KAIST), Nikil Dutt (UCI)

8E-4s
15:15-15:28
A Dynamic Voltage Scaling Algorithm for Energy Reduction in Hard Real-time Systems
Van R. Culver (University of Colorado), Sunil P. Khatri (Texas A&M University)

8E-5s
15:28-15:40
An Efficient Dynamic Task Scheduling Algorithm for Battery Powered DVS System
Jianli Zhuo, Chaitali Chakrabarti (Arizona State University)

Friday, January 21, Time 14:00-15:40

Poster Session IV (19 Boards)

PIV-1: Evaluation of Dual V_{DD} Fabrics for Low Power FPGAs
Rajarshi Mukherjee, Seda Ogrenci Memik (Northwestern University)

PIV-2: Design of an Application-Specific PLD Architecture
Jae-Jin Lee, Gi-Yong Song (Chungbuk National University)

PIV-3: Event-Oriented Computing with Reconfigurable Platform
Mitsuru Tomono, Masaki Nakanishi, Shigeru Yamashita, Katsumasa Watanabe (Nara Institute of Science and Technology)

PIV-4: Reconfigurable Adaptive FEC System with Interleaving
Kazunori Shimizu (Waseda University), Nozomu Togawa (The University of Kitakyushu), Takeshi Ikenaga, Satoshi Goto (Waseda University)

PIV-5: An Amba Ahb-Based Reconfigurable Soc Architecture Using Multiplicity Of Dedicated Flyby Dma Blocks
Adeoye Olugbon, Sami Khawam, Tughrul Arslan, Ioannis Nousias, Iain Lindsay (The University Of Edinburgh)

PIV-6: Using GALS Architecture to Reduce the Impact of Long Wire Delay on FPGA Performance
Xin Jia, Ranga Vemuri (University of Cincinnati)

PIV-7: A Novel Configurable Motion Estimation Architecture for High-Efficiency Mpeg-4/H.264 Encoding
Tiejun Li, Sikun Li, Chengdong Shen (National University of Defense Technology)

PIV-8: A Fast Digit-Serial SystolicMultiplier for Finite Field GF(2^m)
Chang Hoon Kim (Daegu University), Soonhak Kwon (Sungkyunkwan University), Chun Pyo Hong (Daegu University)

PIV-9: Adaptive Fuzzy Control Scheduling of Window-Constrained Real-Time Systems
Zhu Xiangbin, Tu Shiliang (Fudan University)

PIV-10: A High Performance QAM Receiver for Digital Cable TV with Integrated A/D and FEC Decoder
Bo Shen, Junhua Tian, Zheng Li, Jianing Su, Qianling Zhang (Fudan University)

PIV-11: Partitioned Bus Coding for Energy Reduction
Lin Xie, Peiliang Qiu (Zhejiang University), Qinru Qiu (State University of New York)

PIV-12: An Improved Bit-plane and Pass Dual Parallel Architecture for Coefficient Bit Modeling in JPEG2000
Yanju Han, Chao Xu, Yizhen Zhang (Peking University)

PIV-13: A Generalized Quadrature Bandpass Sampling in Radio Receivers
Yi-Ran Sun, Svante Signell (Royal Institute of Technology)

PIV-14: Reducing Leakage Power in Instruction Cache Using WDC for Embedded Processors
Xin Lu, Yuzhuo Fu (Shanghai Jiao Tong University)

PIV-15: System-level Architectural Exploration Using Allocation-on-Demand Technique
Qiang Wu, Jinian Bian, Hongxi Xue (Tsinghua University, Beijing)

PIV-16: A Fractional Delay-Locked Loop for on Chip Clock Generation Applications
P. Torkzadeh (Sharif University of Technology), A. Tajalli (Iran Microelectronics Research Center), M. Atarodi (Mix Core Design)

PIV-17: A Novel O(n) Parallel Banker's Algorithm for System-on-a-Chip
Jaehwan John Lee, Vincent John Mooney III (Georgia Institute of Technology)

PIV-18: Hardware/Software Co-Design Using Hierarchical Platform-Based Design Method
Zhihui Xiong, Sikun Li, Jihua Chen (National University of Defense Technology)

PIV-19: Architecture And Performance Comparison of a Statistic-Based Lottery Arbiter for Shared Bus on Chip
Yan Zhang (Harbin Institute of Technology)

Friday, January 21, 16:10-17:50

Friday, January 21, Time 16:10-17:50
Session 9A: Synthesis for Low Power
Organizers: Jinian Bian, Jianwen Zhu
Moderators: Shih-Chieh Chang, Farzan Falla
Room: Zhong Hua 1 (FL.3)

9A-1
16:10-16:35
Optimal Module and Voltage Assignment for Low-Power
Deming Chen, Jason Cong (UCLA), Junjuan Xu (Peking University)

9A-2
16:35-17:00
Bitwidth-Aware Scheduling and Binding in High-Level Synthesis
Jason Cong, Yiping Fan, Guoling Han, Yizhou Lin (UCLA), Junjuan Xu (Peking University), Zhiru Zhang (UCLA), Xu Cheng (Peking University)

9A-3
17:00-17:25
Functionality Directed Clustering for Low Power MTCMOS Design
Tsuang-Wei Chang, Ting-Ting Hwang, Sheng-Yu Hsu (Tsing Hua University, Hsin-Chu)

9A-4s
17:25-17:38
Wake-up Protocols for Controlling Current Surges in MTCMOS-based Technology
Azadeh Davoodi, Ankur Srivastava (University of Maryland)

9A-5s
17:38-17:50
On Multiple-voltage High-Level Synthesis Using Algorithmic Transformations
Hsueh-Chih Yang, Lan-Rong Dung (Chiao Tung University)

Friday, January 21, Time 16:10-17:50

Session 9B: New Circuit and methodology

Organizers: Yihe Sun, Hoi-Jun Yoo, Takao Onoye

Moderators: Jinmei Lai, Zheng Shi

Room: Zhong Hua 2 (FL.3)

9B-1
16:10-16:35
An Advanced Bit-line Clamping Scheme in Magnetic RAM for Wide Sensing Margin
Jong-Chul Lim, Hye-Seung Yu, Jae-Suk Choi, Soo-Won Kim (Korea University)

9B-2
16:35-17:00
Constructing Zero-deficiency Parallel Prefix Adder of Minimum Depth
Haikun Zhu, C. K. Cheng, Ronald Graham (UCSD)

9B-3s
17:00-17:13
An Accurate 1.08-GHz CMOS LC Voltage-Controlled Oscillator
Zhangwen Tang, Jie He, Hongyan Jian, Hao Min (Fudan University)

9B-4s
17:13-17:25
Area-IO DRAM/Logic Integration with System-in-a-Package(SiP)
Anru Wang, Wayne Dai (UCSC)

9B-5s
17:25-17:38
Design of an Efficient Memory Subsystem for Network Processor
Shuguang Gong, Huawei Li, Yufeng Xu, Tong Liu, Xiaowei Li (Graduate School of the Chinese Academy of Sciences)

9B-6s
17:38-17:50
Design of Clocked Circuits using UML
Zhenxin Sun, Weng-Fai Wong, Yongxin Zhu (National University of Singapore), Santhosh Kumar Pilakkat (Institute for Infocomm Research, Singapore)

Friday, January 21, Time 16:10-17:50

Session 9C: FPGA Circuits and Architectures

Organizers: Yu-Liang Wu, Yao-Wen Chang, Lei He

Moderators: Wai-Kei Mak, Feng Zhou

Room: Han Room 1 (FL.3)

9C-1
16:10-16:35
A Function Generator-based Reconfigurable System
Vivek Garg, Vikram Chandrasekhar, M. Sashikanth, V. Kamakoti (Indian Institute of Technology)

9C-2
16:35-17:00
Crossbar Based Design Schemes for Switch Boxes and Programmable Interconnection Networks
Hongbing Fan (Wilfrid Laurier University), Yu-Liang Wu (The Chinese University of Hong Kong)

9C-3s
17:00-17:13
A Domain Specific Reconfigurable Viterbi Fabric for System-On-Chip Applications
Cheng Zhan, Tughrul Arslan, Sami Khawam, Iain Lindsay (University of Edinburgh)

9C-4s
17:13-17:25
Design of a High Performance FFT Processor Based on FPGA
Chu Chao, Zhang Qin, Xie Yingke, Han Chengde (Institute of Computing Technology, Chinese Academy of Sciences)

9C-5s
17:25-17:38
Increasing FPGA Resilience Against Soft Errors Using Task Duplication
G. Chen, F. Li, M. Kandemir (The Pennsylvania State University), I. Demirkiran (Syracuse University)

9C-6s
17:38-17:50
Automatic Extraction of Function Bodies from Software Binaries
Gaurav Mittal, David Zaretsky, Gokhan Memik, Prith Banerjee (Northwestern University)

Friday, January 21, Time 16:10-17:50

Session 9D-9E: (Special Session) EDA Market in China

Room: Han Room 3 (FL.3)

9D-9E-1 **(Panel III): EDA Market in China**
16:10-17:50 **Organizer**: David Chen, IDT Corp.

Keynote Addresses

Keynote Address I

Wednesday, January 19, 9:00-10:00

The Development of Integrated Circuit Industry in China

By Zhenghua Jiang (Professor, Vice Chairman of The National People's Congress, PRC)

Abstract

The first semiconductor device of China was invented in Shanghai by Fudan University. The China made chips had been equipped national missiles in 1960s. However, The progress of technology was interrupted in the period of "cultural revolution". Since 1980s, the semiconductor industry has recovered and developed extremely fast due to many reasons. The progress of industrialization has been accelerated in late 1990s to early 2000s. The annual growth rate of general output of IC industry of China has reached more than 30% in last six years. We expect that the growth rate will be kept at same or higher level in next decade. Shanghai is the leading region and representative of IC industry of China. The output of IC industry in Shanghai took 51% of that of China in recent years. An IC industry chain system with design, production, encapsulation, test and other functions has been established. Among many enterprises, Huahong NEC, Zhongxin, Hongli and others own 6 four to six-inch chip production lines and 11 eight-inch IC production lines. Huahong Design, Shengsheng Shanghai, Jiaodahanxin, Fudan Micro-Electronics and some other enterprises are strong in IC design. Intel and many other world famous enterprises have set their foot in Shanghai too.

The production of chips in China has increased from 5.88 billion pieces in 2000 to 12.41 billion in 2003, which valued 18.62 billion Yuan and 35.14 billion Yuan respectively. The average annual growth rates both reached 30%. The import of chips has increased from 24.5 billion to 43.6 billion pieces valued 13.3 billion and 35.8 billion U.S dollars in the same period of time. Correspondingly, the export of IC chips has increased from 6.384 to 11.94 billion

pieces and 2.772 to 5.97 billion U.S dollars. We expect that the demand of the market for integrated circuits will keep about the same or even higher growth rate in the years to come.

At present, there are 463 enterprises in China working in the field of IC design. Chinese engineers have made break through achievements in core technology and product designs. By the end of 2003, 17 production lines of 5~8-inch IC chips have been in operation. Shanghai, Jiangsu, Tianjin, Beijing, Guangdong are the main production bases for the encapsulation industry with productivity capacity of 17 billion pieces per year. The production equipment, technology, R&D and management in this field have reached international level.

In year 2003, the demand of market for IC in China reached 48.7 billion pieces valued 237.3 billion Yuan. Comparing to that in year 2002, the annual growth rates are 35.3% and 28.9% respectively. The quota of IC market in China increased from 1.84% in 2002 to 2.04% in 2003. According to sample survey, the demand for products of 0.35μm line-width and above accounts for 46.3% of the IC market in terms of number and 19.6% of the value. The proportions of numbers and values of chips are 46.0% and 39.9% for 0.35-0.18μm, 7.8% and 40.5% for 0.18μm IC products. The demand for different consumption IC was 13.16 billion pieces valued 46.86 billion Yuan, which accounts for 27.0% and 25.6% of the total demands in year 2003 correspondingly. The same terms are 11.01 billion pieces, 46.06 billion Yuan, 22.6%, 19.4% for communication IC products and 15.36 billion pieces, 38.11 billion Yuan, 31.5%, 16.1% for computing IC products and 18.9% of quantity, 38.9% of value for other IC products.

The R&D in the filed of IC products has made significant progress in last few years. The second generation of identification IC chip was put into application. A large number of high-level CPU, DSP and digital multi-media chips made in China have found their way in the market. The quality of many products has reached the world advanced level.

The IC market has strong potential development power in China. The digitalization of consumption products, the popularization of different kinds of

IC cards, the development of E-business, mobile net PC computers, the upgrade of mobile communication and the demands from other industries are all pushing IC industry growing in high rate in China.

The main reasons responsible for the tremendous fast-growth of IC industry in China could be summarized as follows:

1. The beneficial policy of China Government created excellent investment environment for enterprises.

2. The strong support from other sectors such as finance, market management etc is there.

3. The large amount of qualified personnel in China helps the enterprises getting strong technical support with relatively low cost.

4. The sincere cooperation among Chinese and foreign companies reached win-win achievements.

5. The fast growth of China economy and living standard of Chinese people provides unlimited demand on the development of IC industry.

Keynote Address II

Thursday, January 20, 9:00-10:00

Silicon Compilation: The Answer to Reducing IC Development Costs

By Rajeev Madhavan (Chairman and CEO of Magma Design Automation)

Abstract

Developing today's increasingly large and complex digital integrated circuit (IC) and system-on-chip (SoC) devices is becoming cost-prohibitive in terms of engineering resources and development time. Packing the advanced functionality of a microprocessor, a graphics processor, or a network controller into a silicon die just 18 millimeters on a side is a complex undertaking that can require a 50-person engineering team and up to 4 million lines of HDL code. In these complex designs managing and minimizing power is becoming a huge challenge. Meanwhile, the cost of the mask set needed to drive the semiconductor production equipment stands at more than $1 million. Errors found after

the mask set is created increase costs by an additional $1 million or more.

The current chip development process is fraught with pitfalls that can delay schedules and run up huge unexpected costs. Traditional EDA vendors claim to offer a plethora of tools to address the problems. The time required to run these point tools and the poor quality of results they deliver further increase the cost of chip design.

Yesterday's design methodologies are simply not up to the task of producing designs efficiently, on time, and error free. It's clear that at 65-nanometer and below, a revolutionary design methodology that integrates advanced techniques must emerge.

The only feasible methodology to today's design, cost and time-to-market challenges is silicon compilation. This concept was introduced many years ago, but was never fully realized due to a lack of integration and inadequate algorithms. Today, all the necessary technology to enable silicon compilation is available.

What is silicon compilation

At the beginning of a chip design, a model is created at a high level of abstraction known as the register transfer level (RTL). Once this representation has been verified, a variety of tools are employed to transform it into a form known as GDSII. This refers to the file format used to produce the photo-masks, which are, in turn, used to create the IC.

The term "silicon compilation" refers to a tool or tool suite with the ability to take the RTL describing a design, and to automatically generate the corresponding GDSII files. This means that the silicon compiler has to assume control of all of the prototyping and physical implementation portions of the design process, including synthesis, floorplanning, and place-and-route, along with the corresponding power, timing, and signal integrity (SI) analysis engines.

Problems with traditional design environments

Conventional design flows are either a cluster of separate tools or use a common database. Neither of these approaches can adequately address power, signal integrity or other complex challenges. Fixing one problem in isolation can result in new problems being introduced in different domains, and the resulting iterations make this type of design environment unsuitable as a base for silicon compilation. The hierarchical solutions of today are a patch work of pieces trying to integrate the block level solutions.

A higher level of automation to significantly improve productivity is essential. This is not possible in traditional flows where the responsibility for much of the flow and its automation is not an inherent part of the system.

Modern design environments facilitate silicon compilation

The core requirement for true silicon compilation is a modern design environment based on a common data model, in which all of the implementation and analysis engines have concurrent access to all of the data pertaining to the design. One extremely significant advantage of the common data model is that the knowledge associated with any decision making is preserved throughout the flow. This means that any decisions made early in the flow based on incomplete data can be modified downstream as required.

The next big step will be to take such a modern design environment and augment it with the capability to perform true "push-button" silicon compilation that accepts verified design as input and generates GDSII as output. It is anticipated that this would reduce the implementation portion of the design cycle from a typical 26 weeks to only 2 weeks! In reality, there are no fully operational silicon compilation solutions available at this time, but some industry observers are predicting that true silicon compilation may become available within an 18 to 24 month timeframe! Soon, such a tool will be realized and will dramatically reduce both the costs and the time-to-market associated with new IC designs.

Keynote Address III

Friday, January 21, 9:00-10:00

Design at the End of the Silicon Roadmap

By Jan M. Rabaey (Professor UC Berkeley and GSRC director)

Abstract

Scaling of silicon integrated technology into the deep sub-100 nm space

brings with it a number of formidable challenges to the designer. Issues such as design complexity, power dissipation, process variability and reliability are challenging the traditional design methodologies. In this presentation, it is conjectured that the only viable long-term solution to these challenges is to drastically revise the way we do design, and a roadmap of potential solutions is presented. Ultimately, these innovative design solutions will help to pave the way to the post-silicon era.

Tutorials

Tutorial 1 (FULL DAY)

Tuesday, January 18, 9:00-17:00

C-based Design: Industrial Experience

Organizer: Srimat Chakradhar, NEC Labs
Speakers: Srimat Chakradhar, NEC
Wakabayashi, NEC
John Correia, CoWare
David Greavers, TensionEDA

Abstract

C-based design reduces overall turn around time, deals well with complexity, supports optimization based on various objective functions (e.g., area, power consumption), and improves HW/SW co-design. It facilitates the creation of behavioral IP-cores that are more re-usable, a critical competitive success factor; re-use of traditional RTL IPs has been poor. This tutorial describes C-based design techniques in use in the industry. In particular, this tutorial showcases C-based design techniques in use in several companies including Philips and NEC. The tutorial covers C-based design fundamentals, motivation for C-based design, industry need and why the timing is right for C-based design. After discussion of C-based design fundamentals, we move on to support

technologies (power, verification) that are necessary for realizing the full potential of C-based design. EDA response to a call for C-based design is also covered.

Tutorial 2 (FULL DAY)

Tuesday, January 18, 9:00-17:00

Power Aware Design for Performance: Practical Techniques and Tools to Achieve Custom Like Performance in A Power-Aware Asics Design Flow

Organizer: Leon Stok, IBM
Speakers: Ruchir Puri, IBM Research,
Leon Stok, IBM,
Dennis Sylvester, University of Michigan,

Abstract

Power is the limiter in reaching performance in modern design. While ultra-low power design in itself is difficult, the problem becomes ever more complex when aggressive performance targets need to be met within a power budget. After illustrating and motivating the power problem for ASICs, this tutorial will describe circuits, techniques, CAD tools and methodologies to reach aggressive performance targets on strict power budgets. We will present practical techniques and tools that complement a standard ASIC flow in order to achieve performance and power improvement. Traditional synthesis based on conservative wireload models lead to significant overdesign, especially from a power perspective. Modern physical synthesis systems, using gain-based delay models and appropriate libraries, can significantly reduce the power. The design of ASICs/SOCs requires automated techniques that can complement a physical design flow for addition of sleep transistors (header/footer devices). The flexibility of ASIC implementations allows for the use of multiple power supplies to match the performance of critical regions to their timing constraints, and minimize the power every where else. The use of multiple supply voltages presents some unique physical and electrical challenges. Level shifters need to

be introduced between the various voltage regions. Power-aware voltage-scaling and multi-threshold techniques are very effective in an ASIC flow. We will explore the trade-off between multiple supply voltages and multiple threshold voltages in the optimization of dynamic and static power in the design. The application of practical techniques and tools discussed in this tutorial can yield significant improvement in ASIC speed and its power dissipation. During the presentation, we will follow an ASIC design flow through various stages and discuss the impact of the proposed techniques with several high-speed as well as low-power ASICs.

Tutorial 3 (HALF DAY)

Tuesday, January 18, 9:00-12:00

Automated Macromodeling Techniques for Design of Complex Analog and Mixed-Signal Integrated Systems

Organizer: Georges Gielen, Katholieke Universiteit Leuven
Belgium Jaijeet Roychowdhury, University of Minnesota

Speakers: Georges Gielen, Katholieke Universiteit Leuven
Jaijeet Roychowdhury, University of Minnesota

Intended audience

This tutorial is targeted towards design and CAD practitioners in the mixed-signal, analog and RF areas who wish to stay abreast of work in a number of growth areas related to macromodelling. It may also be of interest to those in the high-performance digital design and CAD community who wish to understand or deal with analog effects that are becoming commonplace in high-speed digital (especially communication) systems.

Abstract

The use of simplified macromodels for analog circuits, both to accelerate simulation and to enhance early design exploration, has a long history in analog and mixed-signal design. Traditionally, macromodel construction has relied on

design expertise to create suitably simplified circuit models. With the anticipation of complex multi-standard communications systems, semiconductor process feature sizes below 100nm, and single-chip systems integrating mixed-signal, RF, analog and digital functionalities, manual macromodeling approaches are beginning to constitute a significant design and verification bottleneck. In recent years, there has been a surge of activity in automated approaches to macromodeling that aim to address this bottleneck. There is growing consensus that such automated macromodeling approaches will be essential for realistic design space exploration and verification in current and future mixed-signal SoCs/SiPs.

In this tutorial, a detailed overview will be provided of the state-of-the-art methods for macromodeling. We will cover a variety of approaches for generating macromodels and explain the variety of algorithmic techniques, outline the applications of macromodeling in current and future system-level design flows, and comment on tools in this domain for designers. This will be illustrated with several practical macromodeling examples.

Tutorial 4 (HALF DAY)

Tuesday, January 18, 13:30-16:30

Intellectual Property Protection in Semiconductor and VLSI Design

Organizer: Gang Qu, University of Maryland

Speakers: Gang Qu, University of Maryland
Ian Mackintosh, Sonics Inc.

Abstract

In the early 90's the liabilities of VLSI design intellectual property (IP) infringement were forewarned by experts, once design reuse emerged as a leading design practice clearly able to help in addressing the design productivity gap. However, only recently has such infringement gained the attention it has long deserved. In 2003 and 2004, two years in a row, the World Semiconductor Council (WSC) reported ``an increasing number of instances of counterfeiting of integrated circuits and other semiconductors" in its annual meeting

statement. In June 2004, the Virtual Socket Interface (VSI) Alliance also identified IP protection as the one of the critical IP challenges that must be addressed. With the growth of the Asia Pacific semiconductor market and China entering the World Trade Organization, it is both important and timely to report upon current academic research and industrial practice, as well as the new challenges and opportunities in IP protection.

In the first part of this tutorial, we will briefly introduce the organization of VSI Alliance, whom China recently engaged to provide guidance on IP Protection, Quality and Reuse. We will then focus on issues surrounding IP infringement and current protection mechanisms used in industry. Topics include: the severity of IP theft in semiconductor and IC industry; examples of IP infringement; law enforcement for IP protection; licensing agreements and encryption in VLSI design-IP protection; VSI Alliance's physical tagging standard; cases of successful and failed IP protection.

In the second part, we will introduce both the basics and research advances in IP protection through information hiding. Our discussion will concentrate upon the digital watermarking and fingerprinting approaches, where the VSI Alliance is currently considering the opportunity for standards. We will point out current challenges and possible solutions that must pave the way for such techniques to be adopted as industry standards. Our focus will be on maintaining performance in watermarked designs, efficient watermark detection, and protecting "soft IPs" in the form of Verilog/VHDL codes.

Tutorial 5 (HALF DAY)

Tuesday, January 18, 9:00-12:00

Current Practices and Future Directions in High-Level Design Verification

Organizer: Indradeep Ghosh, Fujitsu Laboratories of America, Inc.

Speakers: Indradeep Ghosh, Fujitsu Laboratories of America, Inc.
Mukul Prasad, Fujitsu Laboratories of America, Inc.
Rajarshi Mukherjee, Calypto Design Systems
Masahiro Fujita, The University of Tokyo

Target Audience

This tutorial is targeted towards VLSI design engineers, managers, professors, students and researchers. It will be particularly useful to persons who work at the RTL and higher levels of design abstraction. Preliminary knowledge of the VLSI design process and logic design in assumed. It will also benefit persons who want to know the latest advances in the area of design verification and validation.

Abstract

With the increasing complexity of VLSI design and time-to-market pressures, two major paradigms have emerged to address the difficulties currently being faced by the industry. They are: (1) the use of higher levels of design abstraction and (2) efficient and seamless design reuse. The design and modeling of a chip at higher levels of design abstraction brings with it additional burdens of validation, verification and testing at these levels. This tutorial will discuss current industrial practices and academic research in design verification and validation at these levels - specifically RTL, behavioral, specification and system level. System level modeling using languages like UML, SpecC and SystemC will be presented and the associated verification challenges highlighted. The next part of the tutorial will discuss formal verification techniques for verifying combinational and sequential designs, including model checking and equivalence checking technology. Details of internals of typical industrial combinational equivalence checking tools will be discussed. The various notions of sequential equivalence will be briefly mentioned. The various challenges in sequential equivalence checking including differences in abstraction levels, precision differences, interface differences, differences in data-types, memory verification, and techniques for handling the state-space explosion problem will be discussed. Industrial practices and recent research results in property based model checking will be presented. The tutorial will touch upon mapping, abstraction and refinement techniques that people use to make formal verification techniques practical. Subsequently the tutorial will focus on

semi-formal methods like bounded model checking, symbolic trajectory evaluation, and symbolic simulation. This will be followed by simulation based validation methods. HDL coverage analysis techniques, and current advances in interface protocol checking using transition coverage will be presented. Simulation based assertion checking methods will be discussed. The tutorial will focus on automatic test bench generation based on test bench automation languages like Sugar {\em etc}. An industrial design verification experience will be presented in the simulation based arena to show the application of these techniques from an industrial perspective. The tutorial will conclude by presenting some future research directions and industrial trends in verification and validation of higher level models in the VLSI design process.

Tutorial 6 (HALF DAY)

Tuesday, January 18, 13:30-16:30

Chip-Package Codesign: Power Integrity Issues, Parasitic Extraction, Parameterized Model Order Reduction, and Design Methodology

Organizer: Luca Daniel, Massachusetts Institute of Technology

Speakers: Shauki Elassaad, Rio Design Automation

Zhenhai Zhu, IBM T.J.Watson Research Center

Luca Daniel, Massachusetts Institute of Technology

Abstract

Signal integrity (SI) and power integrity on-chip and on-package are forecasted to be paramount issues for future designs where the number of IOs is increasing and the switching speed is rising. Higher frequencies and tighter noise margins necessitate the merging of the chip IO and the package design which until recently were two detached paradigms. To enable such a flow, chip design has to be tightly coupled with the package design. For instance parameterized reduced order models accounting for all high frequency SI effects in the package can be reliably and automatically extracted by field solvers, and employed by chip designers when designing the chip's IOs. With time-to-market pressures, package design as an after thought coupled with manual and ad-hoc approaches will fail to meet design goals. Chip-package codesign is emerging as a necessary design flow to tackle design complexity and the staggering issues arising from process developments. In this tutorial, we'll shed light on this new paradigm and all the technologies necessary to enable it. Emphasis will be given to package-aware chip IO planning, package escape analysis and routing, timing, and signal and power integrity analysis.

We will then cover in details some of the most fundamental algorithms and tools for parasitic extraction of complicated 3D geometries such as on-chip and on-package interconnects. We will first explain several commonly used approximations and the corresponding governing equations, and introduce some of the existing efficient numerical techniques to solve these governing equations, such as Pre-corrected FFT algorithm and Hierarchical SVD method. We will then present two of the very latest developments in this field. The first one is a wideband surface integral formulation based extraction approach which can extract the impedance of very complicated 3D geometries with over one million unknowns on a desktop PC. The second is a stochastic integral equation method that can efficiently extract the mean and the variance of parasitic parameters in the presence of surface roughness, an emerging problem in today's package and PCB interconnect design and analysis.

We will then further develop examples to illustrate how to automatically generate accurate parameterized reduced order models from the parasitics extracted by the above mentioned 3D field solvers. Specifically we will show how to assemble a dynamical state space system description from a field solver generated description; how to compress such system using Krylov subspace moment matching techniques such as PRIMA and PVL; and how to generate accurate reduced order models that can be promptly instantiated for different values of geometrical parameters such as wire widths and separations. Finally we will illustrate how to generate passive reduced order models from field solvers descriptions with frequency dependent matrices, typically encountered when handling substrate effects or full-wave effects present in high frequency ICs and packages.

Embedded Tutorials

1D-1: Design for Manufacturability

Abstract

DFM (Design for Manufacturability) has recently become a buzzword; it excites passion in semiconductor process, design, EDA and manufacturing circles. What is all this hype about?

This tutorial reviews DFM, the ugly cousin of technology scaling, in a broad context, and includes both hard defects and parametric variations arising from manufacturing issues in its scope. It presents the various sources of the problem and their impact on yield, silicon vs. timing model correlation, mask cost, data size and time-to-market. It then presents design methodology and EDA tool solutions, both current and future, including restrictive design rules, preferred rules, layout fixes, design-manufacturing integration, layout-dependent modeling, variation-aware analysis and design.

This tutorial is intended for engineers and project managers involved in design, EDA, OPC/RET/tapeout and design rule formulation.

4C-1: Leakage Power: Trends, Analysis and Avoidance

Abstract

Leakage power is emerging as a key challenge in IC design. Leakage is increasingly exponentially with each technology generation and is expected to become the dominant part of total power. Device threshold voltage scaling, shrinking device dimensions, and larger circuit sizes are causing this dramatic increase in leakage. As leakage varies exponentially with process parameters, yield of the chip is often directly influenced by leakage. Increasing amount of leakage is also critical for power constraint ICs. Traditionally, leakage has been considered as an important design variable in handheld devices and in standby circuit operation. However, this significant increase of leakage now warrants that it be considered as the key design variable in all IC designs.

This tutorial presents a comprehensive review of leakage power issues in IC design. The tutorial is organized in four major parts. The first part provides an overview of technology and scaling trends which are causing the significant increase in leakage current. The device physics that leads to sub-threshold and gate leakage will be described, along with their dependence on circuit design variables. This part of the tutorial will also cover basic transistor and circuit techniques to minimize leakage, such as the stack effect.

The second part of the tutorial will focus on circuit level leakage estimation and avoidance. Use of multiple threshold voltages has been very successful in controlling the leakage of the circuit. Comprehensive description of multiple-Vt techniques for leakage avoidance will be presented along with associated leakage estimation techniques. Multiple-threshold design (MTCMOS) will be described along with its leakage benefits and performance trade-offs. Multiple oxide technology options and associated impact on gate leakage will also be discussed.

Third part of the tutorial focuses on chip level effects on leakage. Leakage is heavily dependent on local and global process variations and can vary by an order of magnitude over the technology spread. Leakage estimation techniques which consider both inter and intra-die process variations will be covered. This part of the tutorial also focuses on chip- level leakage minimization techniques. Leakage minimization techniques such as Adaptive Body Bias (ABB) and power supply control will be presented.

The last part of the tutorial covers system and circuit architectures for leakage avoidance. In standby mode, the leakage of the circuit can be lowered by putting it a low-leakage state. Caches and memory circuits occupy large percentage of area in model chips. The leakage of caches and memories need to be carefully controlled. This section of the tutorial will cover topics including state assignment for leakage minimization, leakage-driven memory and cache circuits and architectures.

The tutorial is intended for designers and CAD engineers interested in next generation design techniques and methodologies and emerging power challenges. Basic background of VLSI and CAD is useful though not needed.

5B-1: Designing Reliable Circuit in the Presence of Soft Errors

Abstract

As technology scales, with ever shrinking geometries and higher density circuits, the issue of soft errors and reliability in a complex chip design is becoming a challenging design criterion. Soft errors are caused by radiation, which directly or indirectly induces a localized ionization capable of upsetting internal circuit states. While these errors can result in an upset event, the circuit itself is most often not damaged. Addressing soft error issues is important for a broad range of companies either because they incorporate many semiconductor devices that are prone to soft errors in their system or because they design embedded memories, FPGAs and microprocessors. This tutorial is targeted at researchers/industry practitioners who wish to gain a background on the soft error problem, the techniques that exist to counter this problem and future challenges that lie ahead.

Embedded Invited Talks

4D-1 **Challenges to Covering the High-level to Silicon Gap**
10:30-11:20 Bill Grundmann (Intel Corp.)

Abstract

Silicon architects have a difficult task. They have to translate a high-level product desire into a lower-level description for silicon implementation. They are required to balance their own creativity, project schedule, solution cost, and the degree of difficultly of implementation. Now they also have to worry about power dissipation and physical space realities.

Micro-architectural design starts with a high-level premise. For microprocessors, this premise is in the form of an instruction set architectural (ISA) reference, which is usually in book form. The process of interpreting and converting this ISA, for example, into a constructible RTL requires experience, skills, sometimes arrogance and usually needs a lot of luck. Architectural exploration is heavily constrained by experiences and limited by lack of tools and project schedules. Exploration is important if an architect is to understand any of the design sensitivities to each possible micro-architectural choice.

Power dissipation is a silicon limiter. We have already seen the amount of functionality on a design cut due to the amount of total power dissipation. Optimization of most power dissipating operations is severely limited because of the heavily biased point defined by the Micro-architecture. Small changes to the Micro-architecture can result in significant change in power dissipation. Current circuit optimization tools will never compete with an alternative micro-architectural choice in power savings. Since there is such high power sensitivity to simple architectural decisions, there seems to be a significant gap in tools for the architects to address these problems.

Tools for architects to experiment and explore their architectural options are rare to nonexistent. Tools to assess the relative value of their choices do not exist with the exception of performance analysis that architects usually have to write themselves. So, architects resort to an educated guess, not knowing if their choices will be ultimately good or bad until it's really too late to respond.

To enable any tool assisted architectural exploration we have to solve some tough barriers. The foremost barrier is the problem of modification and correctness proof of time spent in a functional operation, most commonly in the form of latency. Most micro-architectural features and advantages are the result of how functional time is spent. For example, a deterministic-latency of *N* needs changing to *M* while maintaining equivalent overall behavior to the ISA reference. Another case might be a deterministic-latency of *K* needs changing to or from a non-deterministic-latency. If we are to help the architects, we have

to address this essential area. Tools to help perform these kinds of changes and tools to prove correctness of the transformation are fundamental to success.

This talk will look at the whole path from high-level to silicon, look at some of the research along that path and challenge everyone on the important need to cover the micro-architectural exploration gap.

4D-2 **Opportunities and Challenges for Better Than Worst-Case Design**
11:20-11:45
Todd Austin, Valeria Bertacco, David Blaauw, and Trevor Mudge (University of Michigan)

Abstract

The progressive trend of fabrication technologies towards the nanometer regime has created a number of new physical design challenges for computer architects. Design complexity, uncertainty in environmental and fabrication conditions, and single-event upsets all conspire to compromise system correctness and reliability. Recently, researchers have begun to advocate a new design strategy called Better Than Worst-Case design that couples a complex core component with a simple reliable checker mechanism. By delegating the responsibility for correctness and reliability of the design to the checker, it becomes possible to build provably correct designs that e_ectively address the challenges of deep submicron design. In this paper, we present the concepts of Better Than Worst-Case design and highlight two exemplary designs: the DIVA checker and Razor logic. We show how this approach to system implementation relaxes design constraints on core components, which reduces the e_ects of physical design challenges and creates opportunities to optimize performance and power characteristics. We demonstrate the advantages of relaxed design constraints for the core components by applying typical-case optimization (TCO) techniques to an adder circuit. Finally, we discuss the challenges and opportunities posed to CAD tools in the context of Better Than Worst-Case design. In particular, we describe the additional support required for analyzing run-time characteristics of designs and the many opportunities which are created to incorporate typical-case optimizations into synthesis and veri_cation.

4D-3 **Microarchitecture Evaluation With Floorplanning And Interconnect Pipelining**
11:45-12:10
Ashok Jagannathan (UCLA), Hannah Yang, Kris Konigsfeld, Dan Milliron, Mosur Mohan (Intel Corp.), Michail Romesis, Glenn Reinman, and Jason Cong (UCLA)

Abstract

As microprocessor technology continues to scale into the nanometer regime, recent studies show that interconnect delay will be a limiting factor for performance, and multiple cycles will be necessary to communicate global signals across the chip. Thus, longer interconnects need to be pipelined, and the impact of the extra latency along wires needs to be considered during early micro-architecture design exploration. In this paper, we address this problem and make the following contributions: (1) a floorplan-driven micro-architecture evaluation methodology considering interconnect pipelining at a given target frequency by selectively optimizing architecture level critical paths. (2) use of micro-architecture performance sensitivity models to weight micro-architectural critical paths during floorplanning and optimize them for higher performance. (3) a methodology to study the impact of frequency scaling on micro-architecture performance with consideration of interconnect pipelining. For a sample micro-architecture design space, we show that considering interconnect pipelining can increase the estimated performance against a no-wire-pipelining approach between 25% to 45%. We also demonstrate the value of the methodology in exploring the target frequency of the processor.

Panels

Panel I

Wednesday, January 19, 16:10-17:50

Who Is Responsible for the Design for Manufacturability Issues in the Era of Nano-Technologies?

Organizers:	C.K. Cheng, UCSD
	Steve Lin, Tsing Hua University, Hsin-Chu
Moderator:	Andrew Kahng, UCSD
Panelists:	Keh-Jeng Chang, Tsing Hua University, Hsin-Chu
	Vijay Pitchumani, Intel
	Toshiyuki Shibuya, Fujitsu
	Roberto Suaya, Mentor Graphics
	Zhiping Yu, Tsinghua University, Beijing
	Fook-Luen Heng, IBM
	Don MacMillen, Synopsys

The notion of design for manufacturability is blurring the separation between the tasks of design and manufacture. In the era of nano-technologies, the description of the design rules has retreated back to an early stage form of many conditional cases and even an art. Thus, it is important to set the metrics for the manufacturability. However, who is going to be held accountable for the final outcomes? Should the designer, the EDA developer, the manufacture engineer, or a new breed of experts take the lead to tackle the problem?

Panel II

Thursday, January 20, 16:10-17:50

Are We Ready for System- Level Synthesis?

Organizers:	Jason Cong, UCLA
	Tony Ma, Synopsys
Moderator:	Jason Cong, UCLA
Panelists:	Ivo Bolsens, Xilinx
	Phil Moorby, Synopsys
	Jan Rabaey, UCB
	John Sanguinetti, Forte Design Systems
	Kazutoshi Wakabayashi, NEC Laboratories
	Yoshi Watanabe, Cadence Berkeley Labs

Electronic system-level (ESL) design automation has been identified by Dataquest as the next productivity boost for the semiconductor industry. We have put together a distinguished panel of experts to discuss if we are ready for system-level synthesis. In particular, the panle will cover the following questions:

1. Why all previous efforts on behavior and system level synthesis failed to make a real impact to the industry?
2. Do we now have a system-level design language for synthesis?
3. What are the merits and limitations of the existing system-level design language (SystemVerilog, SystemC, SpecC, C/C++, Java, etc.)? Do we have a true winner yet (to be accepted like Verilog or VHDL)? If so, which one? If not, how/who will develop one?

4. What kind of quality of results can we expect from the existing system-level synthesis tools? Can they match manual designs?
5. Who will be the first adopt system-level synthesis? When?

Panel III

Friday, January 21, 16:10-17:50

EDA Market in China

Organizers: David Chen, IDT Corp.
Moderator: Nancy Wu
Panelists: Wayne Dai, CEO of VeriSilicon
Jun Tan, President of ARM China
Weiping Liu GM of CEC Huada Electronic Design
Hao Min, GM of Shanghai Huahong IC Design, Prof. of Fudan
Jian-yue Pan, China Country Manager, Synopsys
Nancy Wu, Analyst of EDA Asia Market, Gartner Dataquest

ASP-DAC 2005 at a Glance

Tuesday, January 18

FULL-DAY Tutorials

TUTORIAL 1	**(9:00-17:00)**
C-based Design: Industrial Experience	
TUTORIAL 2	**(9:00-17:00)**
Power Aware Design for Performance: Practical Techniques and Tools to Achieve Custom Like Performance in a Power-Aware ASICs Design Flow	

HALF-DAY Tutorials

TUTORIAL 3	**(9:00-12:00)**
Automated Macromodeling Techniques for Design of Complex Analog and Mixed-Signal Integrated Systems	
TUTORIAL 4	**(13:30-16:30)**
Intellectual Property Protection in Semiconductor and VLSI Design	
TUTORIAL 5	**(9:00-17:00)**
Current Practices and Future Directions in High-Level Design Verification	
TUTORIAL 6	**(13:30-16:30)**
Chip-package codesign: power integrity issues, parasitic extraction, parameterized model order reduction, and design methodology	

	Wednesday, January 19					
8:30	A	B	C	D	E	Joint
9:15	Opening Session					
10:15	**Keynote Address I**					
10:30	**Coffee Break**					
	1A Tree Construction and Buffering	1B System Level Design Methodology for Network-on-Chip	1C Test and DFT (1)	1D Special Session (DFM) Embedded Tutorial I	1E Clock, Power Grid and Thermal Analysis and Optimization	Poster Session I (25 Boards)
12:10	**Lunch Time**					
14:00	2A Routing and Interconnects	2B System Level Modeling and Embedded Software	2C Test and DFT (2)	2D TCAD	2E Simulation and Modeling Techniques for RF/Analog Circuits	Poster Session II (25 Boards)
15:40	**Coffee Break**					
16:10	3A Logic Synthesis	3B System Level Architecture Design	3C Test and Verification	Panel I Who Is Responsible for the Design for Manufacturability Issues in the Era of Nano-Technologies?		
17:50						

	Thursday, January 20					
9:00	A	B	C	D	E	Joint
10:00	**Keynote Address II**					
10:30	**Coffee Break**					
	4A Placement Techniques	4B Security Processor Design	4C Special Session Embedded Tutorial II	4D Special Session CAD for Microarchitecture Designs	4E Design Optimization for High-Performance Digital Circuits	University Design Contest Session
12:10	**Lunch Time**			**Ph.D. Forum Session**		
14:00	5A Floorplanning and Partitioning	5B Special Session Embedded Tutorial III	5C Advances in SAT Technology and Application	5D Analysis and Simulation Techniques	5E Interconnect Modeling and Analysis and System Level Design Methodology	Poster Session III (25 Boards)
15:40	**Coffee Break**					
16:10	6A High-Level Synthesis	6B Low Power	6C Formal Verification: Theory and Practice	Panel II Are We Ready for System-Level Synthesis?		
17:50						

	Friday, January 21					
9:00	A	B	C	D	E	Joint
10:00	**Keynote Address III**					
10:30	**Coffee Break**					
	7A Robust and Low-Power Clock Design	7B DSP	7C Low Power and Special Purpose FPGAs	7D RF Circuit Design and Design Methodology	7E Design Techniques in Embedded and Real-time System	
12:10	**Lunch Time**					
14:00	8A Crosstalk Noise Avoidance and Power/Ground Network Optimization	8B Others in Leading Edge Designs	8C Synthesis for FPGAs	8D Analog Circuit Design	8E Low Power Design for Embedded and Real-time Systems	Poster Session IV (19 Boards)
15:40	**Coffee Break**					
16:10	9A Synthesis for Low Power	9B New Circuit and Methodology	9C FPGA Circuits and Architectures	Panel III EDA Market in China		
17:50						

Registration Form

Deliver this form fax (or mail) this form to:

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Huihua Yu
Dept. of Microelectronic
Fudan University
220 Handan Road
Shanghai 200433, China

Email：register@aspdac2005.com

A. Participant

□ Mr. □ Ms.	First Name:	Last Name:
Affiliation （University/Company）		
Address:		
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B. Registration Fee

Classification	**Before Dec.24, 2004**	**After Dec.24, 2004**	**Amount**
★ **Member**	□ USD 375	□ USD 405	
Non-member	□ USD 455	□ USD 485	
Full-time student	□ USD 195	□ USD 225	
One-day only	□ USD 230	□ USD 250	
Extra banquet	□ USD 40		

C. Tutorial Fee

★ **Member**	□ USD 225	□ USD 255	
Non-member	□ USD 275	□ USD 305	
Full-time student	□ USD 135	□ USD 155	
Total Amount Payment			**USD**

(★ **Member** of IEEE, ACM SIGDA)

★ **Member number:**_____

Registration fee includes:

- Admission to all sessions
- Reception & Banquet (excluding Full-time students and One-day only)
- Three days lunch
- Conference kit (with a conference bag, a program, a CD-ROM and a copy of Proceedings)

Tutorial fee includes:

● Admission to tutorial(s) ● One copy of text ● Lunch

Payment (Please give clear indication of registration for ASP-DAC 2005)

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Weather

January is the winter season in Shanghai. The temperature is around 3 ^{o}C- 15 ^{o}C.