Robust Analytical Gate Delay Modeling for Low Voltage Circuits

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Outline

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2. Elmore View of Sakurai-Newton Model
3. A New/Robust Analytical Gate Delay Model
4. Experimental Results
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1. Introduction & Motivation

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One of the most fundamental EDA problems

Two components of delay modeling
- Gate delay
- Interconnect delay

Different levels of accuracy and abstraction
- Analytical formula: simple and intuitive to guide optimization
- Table look-up based
- Simulation-based, e.g., SPICE

This work is on gate delay modeling
Table-look up

Closed-form formula: Sakurai-Newton (SN) model [1990]
- Widely used due to its simplicity and reasonable accuracy
- However, it does not work well at low voltages [Taur and Ning, 1998]

Contribution of this work
- We provide a new Elmore-perspective of the SN model, which is the centroid of the current
- We propose a new closed-form gate delay model based on the centroid of the power dissipated by the gate
- This new model is robust (across wide ranges) with very high fidelity
Gate delay can be approximated as

$$\Delta t = \frac{\Delta Q}{I_D}$$

where

- $\Delta Q$: change in charge at load capacitor $C_L$
- $I_D$: drain current

The 50% gate delay is

$$t_{\text{delay}} = \frac{C_L \left( \frac{V_{DD}}{2} \right)}{I_D}$$
SN current equation (saturation-mode) \( I_D = \frac{k}{2}(\nu_{GS} - V_T)^\alpha \)

- \( \alpha \) is velocity saturation index, \( \alpha \approx 1 \) for nm regimes

Assume a step input, \( \nu_{GS} = V_{DD} \cdot u(t) \)

SN assumes that the transistor is in saturation region till \( \frac{V_{DD}}{2} \)

\[
\begin{align*}
t_{delay} &= \frac{C_L \frac{V_{DD}}{2}}{I_D} \\ &\approx \frac{C_L \frac{V_{DD}}{2}}{k \frac{V_{DD}}{2}(V_{DD} - V_T)^\alpha} 
\end{align*}
\]

But discharge under step input has two regions

- Saturation: \( V_{DD} \geq \nu_{DS} > V_{DD} - V_T \)
- Linear: \( V_{DD} - V_T \geq \nu_{DS} \geq 0 \)

Thus SN delay formula is obtained through approximation

We show that it is in fact Elmore delay of gate
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Elmore delay

Definition

Elmore delay is defined as the centroid of the impulse response $h(t)$

- The centroid of a function $f(x)$ is defined as $C[f(x)] = \frac{\int_x x f(x) \, dx}{\int_x f(x) \, dx}$

- Since $\int_0^\infty h(t) \, dt = 1$ for monotonic RC circuit

- Note that Elmore delay is Mean of impulse response
  - Real delay is given by Median
  - Mean is an upperbound of Median for RC circuits
Impulse response $\propto$ switching current in RC circuit

- Model inverter as an RC circuit
  - \( R \): nonlinear resistor
- Laplace transform of \( h(t) \) (\( H(s) \))
  \[
  H(s) = \frac{V_{DS}(s)}{V_{GS}(s)} = \frac{V_{DS}(s)}{\frac{1}{s}} = sV_{DS}(s)
  \]
- Translate to time domain
  \[
  h(t) = \frac{dv_{DS}}{dt} = \frac{1}{C_L}I(t) \propto I(t)
  \]
- Centroid of \( I(t) \) instead of \( h(t) \)
Elmore delay is centroid of switching current

**Lemma**

The Elmore delay of a CMOS gate under step input is the centroid of the current dissipated by it during switching.

- Thus Elmore delay is

\[ t_{elmore} = \frac{\int_0^\infty t h(t) dt}{\int_0^\infty h(t) dt} = \frac{\int_0^\infty t I(t) dt}{\int_0^\infty I(t) dt} \]

\[ = \frac{\int_{t_{sat}}^\infty t i_{DSAT} dt + \int_{t_{sat}}^\infty t i_{DLIN} dt}{\int_{t_{sat}}^\infty i_{DSAT} dt + \int_{t_{sat}}^\infty i_{DLIN} dt} \]

- The unknowns in the above equation are
  - \( t_{sat} \): Transition point from saturation to linear
  - \( i_{DSAT} \), \( i_{DLIN} \): Current in the saturation/linear region of operation
**$t_{\text{sat}}$: Transition point from saturation to linear**

- The transistor under step input **switches** from saturation to linear when $v_{DS} = V_{DD} - V_T$

- $t_{\text{sat}}$: time taken to change from saturation to linear

- $t_{\text{sat}}$ is obtained by applying KCL at $C_L$

\[
t_{\text{sat}} = \frac{2C_LV_T}{k(V_{DD} - V_T)^\alpha}
\]
\( i_{D_{\text{SAT}}} \): Constant current in saturation

\[
i_{D_{\text{SAT}}} = \frac{k}{2} (V_{DD} - V_T)^\alpha
\]

\( i_{D_{\text{LIN}}} \): Current in linear region

\[
i_{D_{\text{LIN}}} = k (V_{DD} - V_T)^\alpha \frac{v_{DS}}{V_{DD} - V_T} = \frac{v_{DS}}{R}
\]

\( v_{DS} \): is given by

\[
v_{DS} = (V_{DD} - V_T)e^{-\frac{(t-t_{\text{sat}})}{RCL}} u(t-t_{\text{sat}})
\]
SN delay formula is Elmore delay

• Putting $t_{sat}$ and $i_{DSAT}/i_{DLIN}$ back to the Elmore delay (the centroid of $I(t)$), we have

$$t_{elmore} = \frac{C_L V_{DD}}{k(V_{DD} - V_T)\alpha}$$

• It is exactly the same as the Sakurai-Newton formula

**Theorem**

*The Sakurai-Newton formula is the Elmore delay of the CMOS gate under the following conditions:*

(i) *A step input is applied;*

(ii) *The CMOS gate is modeled as an RC circuit.*
- Data of 65nm inverter with $C_L = 20\, \text{fF}$ and $V_{T0} = 0.22\, \text{V}$

- Under nominal voltages ($V_{DD} \geq 0.9\, \text{V}$), delay varies over small range $[150, 180]\, \text{ps}$
  - Empirically delay $\propto \frac{1}{V_{DD}}$, captured well by SN

- Under low voltages ($V_{DD} < 0.9\, \text{V}$), delay varies over wide range $[200, 800]\, \text{ps}$
  - Need higher order terms to capture this spread which SN lacks
A New/Robust Analytical Gate Delay Model

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SN metric fails to track delay under low voltages where delay
\[ \propto \frac{1}{V_{DD}^2} \]
A natural idea is to use centroid of power instead of current to track this quadratic term since power \( \propto (\text{current})^2 \)
- This results in Elmore-like closed form expression

Centroid-of-power delay \( (t_{cp}) \) is defined as

\[
 t_{cp} = \frac{\int_0^\infty t v_{DS} i_D \, dt}{\int_0^\infty v_{DS} i_D \, dt}
\]

\[
 t_{cp} = \frac{ C_L(3V_{DD}^3 + 3V_{DD}^2 V_T - 3V_{DD}V_T^2 + V_T^3) }{ 6kV_{DD}^2(V_{DD} - V_T)^\alpha }
\]
We empirically found that \( \frac{1}{(V_{DD} - V_T)^2} \) tracks delay better than \( \frac{1}{V_{DD}^2} \) in the denominator.

- Have not found the rigid theory behind yet

**Modified** centroid of power based delay metric

\[
t_{cpm} \propto \frac{C_L(3V_{DD}^3 + 3V_{DD}^2V_T - 3V_{DD}V_T^2 + V_T^3)}{(V_{DD} - V_T)^2(V_{DD} - V_T)^\alpha}
\]

- This modification on \( t_{cp} \) leads to **near perfect correlation** across all voltage ranges
- Possible reasons why it works
  - Gate overdrive is proportional to \( (V_{DD} - V_T) \)
  - When \( V_{DD} \) varies, \( \frac{1}{(V_{DD} - V_T)^2} \) has a faster rate of change compared with \( \frac{1}{V_{DD}^2} \)
Experimental Results

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Data of 65nm inverter with $C_L = 20\, fF$ and $V_{T0} = 0.22V$

- Observe that CPM can track delay across all voltages
  - Higher order terms of CPM help track delay in low voltages
Experimental Results

Comparison across Different Technologies and Gates

<table>
<thead>
<tr>
<th>Gate</th>
<th>45nm</th>
<th>65nm</th>
<th>100nm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SN</td>
<td>CP</td>
<td>CPM</td>
</tr>
<tr>
<td>INV</td>
<td>0.76</td>
<td>0.81</td>
<td>0.99</td>
</tr>
<tr>
<td>NAND2</td>
<td>0.72</td>
<td>0.76</td>
<td>0.99</td>
</tr>
<tr>
<td>NOR2</td>
<td>0.73</td>
<td>0.78</td>
<td>0.99</td>
</tr>
<tr>
<td>XOR2</td>
<td>0.71</td>
<td>0.76</td>
<td>0.99</td>
</tr>
</tbody>
</table>

- Correlation indices for each delay model/gate/technology
- Data obtained by varying $V_{DD}$, $V_{TO}$, $C_L$
- HSPICE delay of a gate is measured for its worst case input combination
- Modified Centroid of Power (CPM) has correlation $\geq 0.98$ consistently
Conclusion

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**Conclusion**

- Provide **theoretic proof** that the classic Sakurai-Newton delay model is indeed Elmore delay.
- We propose a new **closed form** delay model based on the modified centroid of power (modify the Elmore).
- Our proposed metric has very high correlation ($\geq 0.98$) compared to HSPICE simulations.
- We expect this simple, accurate and robust gate delay model be used:
  - in low power, low voltage circuit designs
  - in inner optimization loop of physical design tools where it is necessary to obtain quick and accurate delay estimates.