A Built-in Power Supply Noise Probe for Digital LSIs

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Built-in noise probing technique

- Dynamic PS drop analysis
  - time-varying digital activity distribution
  - AC transfer characteristics of on/off chip LRC network
- Profile PS noise distribution
  - chip level
  - PS-grid resolution
  - vector-length acquisition
SF+Gm detector

➢ Simplest way of noise probing, w/o sampling
➢ Footprint comparable to D-type flip flop (FF) cell

Vbias

Vnoise

SF

Gm

I_{out}
Test circuit design

#Cell Row

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

IoutN1 IoutP1 IoutN2 IoutP2 VDDD GNDD

pSF+Gm nSF+Gm pSF+Gm nSF+Gm

32-bit SR 32-bit LFSR 32-bit SR 32-bit LFSR 32-bit SR 32-bit LFSR

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Vcal

N1 P1 N2 P2
Measured dynamic drop waveforms

$V_{dd}$ (mV) vs. $V_{gnd}$ (mV)

Fck = 40 MHz

$V_{drop}$