IEEE Standard 1500 Based Interconnect Diagnosis for Delay and Crosstalk Faults

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Outline

- Introduction
- Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis
- Interconnect Diagnosis Algorithm
- Optimization Techniques for Interconnect Diagnosis
- Experimental Results
- Conclusion
Why Interconnect Testing and Diagnosis are Difficult?

**Complexity issue**
- Too many rings
- Consider a bus-connected system
  - m cores, n bus lines
  - Assuming each core passed by a ring at most once (a lower bound)

# rings of length l from n buses (connecting i cores): \( C_i^n \)

# all rings: \( \sum_{i=2}^{\min(m,n)} C_i^m C_i^n \) \( \rightarrow \) Exponential!
Introduction (Cont’d)

- Interconnect dominates performance
  - Interconnect Diagnosis
- SoC Design Methodology
  - IEEE Std.1500 Based Interconnect Diagnosis
- Other Applications: PCB, MCM, SiP
- Interconnect Test
  - Goal
    - Interconnect Detection Problem => Pass/Fail
    - Interconnect Diagnosis Problem => Fault Location
  - Target Fault Models
    - Delay Fault
    - Crosstalk Glitch Fault
    - Traditional Stuck-at Fault, Open Fault
  - Oscillation Ring (OR) Based Test Scheme
Contribution of this Work

- Apply a heuristic algorithm to generate test rings quickly ($R_t$)
  - Previous Work on Oscillation Ring (OR) Based Interconnect Test Scheme for SOC
    - ASPDAC 2005
- Provide a fast diagnosability check algorithm
  - Similar to fast fault simulation
- Provide a heuristic algorithm to generate extra diagnosis rings
  - Similar to IORD test pattern generation
- Present two optimization testing process
  - Concurrent OR
  - Adaptive OR
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Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
  - Test Architecture
  - Enhanced IEEE Std.1500-Compliant Wrapper Cell Design
  - Effectiveness
    - Delay Fault: longest & shortest ring in HP circuit ($f_{\text{min}}$ vs. $f_{\text{max}}$)
    - Crosstalk Glitch Fault: SoC simulation results

- Oscillation Ring Test Scheme for
  - Interconnect Detection Problem (IORT)
  - Interconnect Diagnosis Problem (IORD)
Test Architecture for Delay and Crosstalk Detection and Delay Measurement
Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
  - Test Architecture
  - Enhanced IEEE Std.1500-Compliant Wrapper Cell Design
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    - Delay Fault: longest & shortest ring in HP circuit ($f_{\text{min}}$ vs. $f_{\text{max}}$)
    - Crosstalk Glitch Fault:

Oscillation Ring Test Scheme for
- Interconnect Detection Problem (ORT)
- Interconnect Diagnosis Problem (ORD)
IEEE Std.1500 Wrapper Cell Design

(a) Input

(b) Output

Modified with force Inversion
Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
  - Test Architecture
  - Enhanced IEEE Std.1500-Compliant Wrapper Cell Design
- Effectiveness
  - Delay Fault:
    - longest & shortest ring in HP circuit ($f_{\text{min}}$ vs. $f_{\text{max}}$)
    - Delay Measurement
  - Crosstalk Glitch Fault:
Longest Test Ring in HP circuit
Simulated Waveforms of Longest and Shortest Test Rings of HP Circuit

Longest Ring of 38 ns

\[ f_{\text{min}} = 21.316 \text{ MHz} \]

Shortest Ring of 2.8 ns

\[ f_{\text{max}} = 357.143 \text{ MHz} \]
Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
  - Test Architecture
  - Enhanced IEEE Std.1500-Compliant Wrapper Cell Design
- Effectiveness
  - Delay Fault:
    - longest & shortest ring in HP circuit ($f_{\text{min}}$ vs. $f_{\text{max}}$)
    - Delay Measurement
  - Crosstalk Glitch Fault:
Delay Measurement

\[ f_i = f \times \frac{n_i}{n} \]

Let \( f_i \) be 4 MHz to 400 MHz 
\((f_{\text{min}} = 4\text{MHz}, \ f_{\text{max}} = 400\text{MHz})\)

\[ \varepsilon = \frac{1}{f_{\text{min}} \times T_0} \leq \zeta \]

\( \xi \) be at least is 0.001

\( \Rightarrow n_{\text{min}} \geq 1000 \)
\( \Rightarrow T_0 \geq 250\mu s \)
\( \Rightarrow T_0 = 250\mu s \) (OscTest Spec.)
Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
  - Test Architecture
  - Enhanced IEEE Std.1500-Compliant Wrapper Cell Design
- Effectiveness
  - Delay Fault:
    - longest & shortest ring in HP circuit ($f_{\text{min}}$ vs. $f_{\text{max}}$)
    - Delay Measurement
  - Crosstalk Glitch Fault:
    - longest ring in HP circuit with 5 wrapper cells
Crosstalk Glitch Fault Detection –
longest ring in HP with 5 wrapper cells

oscillation circuit

Oscillation Signal

Counter output

Glitches on victim net
Crosstalk Glitch Detection (cont’d)

Detector output

Xtalk-induced Glitch

Oscillation Signal

After 5 wrapper cells

Counter output
Modified Input Wrapper Cell for Crosstalk Glitch Faults

Pulse detector – an inverter with special W/L

normal wrappe

To Core

OscTest

sel

SI

IN

SO
Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
  - Test Architecture
  - Effectiveness
    - Delay Fault: longest & shortest ring in HP circuit ($f_{\text{min}}$ vs. $f_{\text{max}}$)
    - Crosstalk Glitch Fault:

- Oscillation Ring Test Scheme for
  - Interconnect Detection Problem (IORT)
  - Interconnect Diagnosis Problem (IORD)
Oscillation Ring Test Scheme

- Single-Fault Assumption
- Interconnect Detection Problem (IORT)
  - Pass or Fail $\Rightarrow$ Edge-Covering Problem
  - Goal: Fault Detection on Test Rings
  - Interconnect Detection Model
- Interconnect Diagnosis Problem (IORD)
  - Fault Diagnosis $\Rightarrow$ Fault Location Problem
  - Goal: Optimal Resolution to Net Segment
  - Interconnect Diagnosis Model
An Example SOC Circuit for Interconnect Test

Hypernet

(a) Hypergraph of SoC Circuit with multiple-terminal nets

(b) Interconnect Test Modeling
**Oscillation Ring Test Scheme**

- **Single-Fault Assumption**
- **Interconnect Detection Problem (IORT)**
  - Pass or Fail $\Rightarrow$ Edge-Covering Problem
  - Goal: Faults on Test Rings
  - Interconnect Detection Model
- **Interconnect Diagnosis Problem (IORD)**
  - Fault Diagnosis $\Rightarrow$ Fault Location Problem
  - Goal: Optimal Resolution to Net Segment
  - Interconnect Diagnosis Model
Interconnect Detection Model

2-pin nets \( N_{11} = n_{11} + n_{12}, \ N_{12} = n_{11} + n_{13} \)
Oscillation Ring Test Scheme

- Single-Fault Assumption
- Interconnect Detection Problem (ORT)
  - Pass or Fail $\Rightarrow$ Edge-Covering Problem
  - Goal: Faults on Test Rings
  - Interconnect Detection Model
- Interconnect Diagnosis Problem (ORD)
  - Fault Diagnosis $\Rightarrow$ Fault Location Problem
  - Goal: Optimal Resolution to Net Segment
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Interconnect Diagnosis Model

(a) Hypernet
(b) Interconnect Diagnosis Model

For Diagnosis: Every Edge Influences Different Rings => Optimal Diagnosis Resolution is Edge
Outline

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- Interconnect Diagnosis Algorithm
- Optimization Techniques for Interconnect Diagnosis
- Experimental Results
- Concluding Remarks
Interconnect Diagnosis Algorithm

- Diagosalibility Conditions
- Heuristic Diagosalibility Check
- Number of Tests
- Interconnect Diagnosis Algorithm
  - IORT (Interconnect Oscillation Ring Test)
  - IORD (Interconnect Oscillation Ring Diagnosis)
An Interconnect Diagnosis Graph Example to Show Diagnosability Conditions

\[ r_1 = r_2 = r_3 = r_4 = \{ e_i, e_j, e_k \} \]

\[ r_5 = \{ e_j, e_k \} \]

\[ R_i = \{ r_1, r_2, r_3, r_4 \} \]

\[ R_j = R_k = \{ r_1, r_2, r_3, r_4, r_5 \} \]

\[ E_j = E_k = r_1 \cap r_2 \cap r_3 \cap r_4 \cap r_5 = \{ e_j, e_k \} \Rightarrow E_i \neq E_j = E_k \]
An Interconnect Diagnosis Graph Example
An Illustrative SoC Circuit for Interconnect Diagnosis

(a) Hypergraph

(b) Interconnect Diagnosis Model

=> Optimal Resolution is Edge
An Illustrative Diagnosability Example

\[ r_1 = \{e_1, e_2, e_3, e_6\} \]
\[ r_2 = \{e_1, e_3, e_5\} \]
\[ r_3 = \{e_1, e_4, e_6\} \]

For Test Rings thru \(e_1\)
\[ \Rightarrow R_1 = \{r_1, r_2, r_3\} \]
\[ \Rightarrow |R_1| = 3 \]
\[ \Rightarrow \text{Syndrome} = [1,1,1] \]
Matrices for the Heuristic Diagnosability Checking

<table>
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<tr>
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<th>$e_1$</th>
<th>$e_3$</th>
<th>$e_6$</th>
<th>$e_2$</th>
<th>$e_4$</th>
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(a)

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</table>

(b)

Complexity for check: $O(n^2m)$
Flow Chart of Diagnosability Checking

Sort all edges $e_i$ according to $|R_i|$.

Pick an edge $e_i$.

If $|E_i| = 1$, then:

- Yes: Compare $e_i$ to all $e_j$ with $|R_j| = |R_i|$.

Otherwise:

- No: Compare $e_i$ to all $e_j$ with $|R_j| = |R_i|$.

If there exists an $e_j$ such that $E_j = E_i$:

- Yes: Edge $e_i$ is diagnosable, remove $e_i$ from all rings in $R_j$ with $|R_j| = |R_i|$.

Otherwise:

- No: All edges processed or not enough resolution.

Yes: All edges processed or not enough resolution.

No: All edges processed or not enough resolution.
Interconnect Diagnosis Algorithm

- Diagonosability Conditions
- Heuristic Diagonosability Check
- Number of Tests
- Interconnect Diagnosis Algorithm
  - IORT (Interconnect Oscillation Ring Test)
  - IORD (Interconnect Oscillation Ring Diagnosis)
Number of Tests

- IORT ($|R_t|$)
  - Lower Bound: 1
  - Upper Bound: $n$

- IORD ($|R_d|$)
  - Previous Example: $n/2$ distinct rings
  - N-bus Example: $n-1$ rings
  - Random Case: $|R_d| = |R_t| + \text{additional Diagnosis Rings}$
    predetermined rings
Theorem for Upper Bound of Predetermined Diganosis

Assume:

- $m$ equivalence classes, whose sizes are $s_1$, $s_2$, ..., $s_m$, respectively.
- The upper bound on the number of additional diagnosis rings “$|R_d| - |R_t|$” as theoretical results:

$$\sum_{i=1}^{m} (S_i - 1) = \sum_{i=1}^{m} S_i - m = \# \text{NoDiag} - \# \text{EquClass}$$
An Illustrated Example of Predetermined Diganosis Ring Generation

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<th>$e_2$</th>
<th>$e_4$</th>
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<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td>$r_4$</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
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</tr>
</tbody>
</table>

Add $r_4$ to distinguish between $e_3$ and $e_6$ in Group of $|R_i|=2$

=> Syndrome of $e_3$ and $e_6$ is different!
Interconnect Diagnosis Algorithm

- Interconnect Diagnosability Analysis
- Heuristic Diagnosability Check
- Number of Tests
- Interconnect Diagnosis Algorithm
  - IORT (Interconnect Oscillation Ring Test)
  - IORD (Interconnect Oscillation Ring Diagnosis)
Diagnosis Ring Generation Procedure

1. Test Ring Generation ($R_t$)
2. Diagnosability Check
   - Generate a Diagnosis Ring ($R_a$)
3. Diagnosability Check
   - Enough diagnosis resolution?
     - Yes
     - No
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Optimization Techniques for Interconnect Diagnosis

- Concurrent Diagnosis: under Worst Case Scenario
  - Scan Path Constraint
  - Shared Edge Constraint
- Adaptive Diagnosis ($R_a$)
  - Use almost same test cost with IORT ($R_t$) only to reduce test time efficiently
Scan Path Constraints

Core Boundary
Concurrent Test

Scan path conflict

Shared edge conflict

(a) Conflict Graph

(b) Graph coloring
Optimization Techniques for Interconnect Diagnosis

- Concurrent Diagnosis
  - Scan Path Constraint
  - Shared Edge Constraint
- Adaptive Diagnosis ($R_a$)
  - Construct adaptive diagnosis tree
  - Diagnosis cost
    - Best Case: Balanced adaptive tree
    - Worst Case: Skewed adaptive tree
Adaptive Diagnosis Tree

Diagnosability Checking Matrix
Upper Bound of Adaptive Diagnosis

- $|R_t|$: the number of test rings for detection (IORT)
- $L_h$: the length of the longest test ring
- Best Case
  - If the tree is balanced, the minimum number of diagnosis patterns required is $\left\lceil \log(n + 1) \right\rceil$
- Worst case for Skewed Adaptive Tree,
  - Apply $|R_t|$ rings to find out that there is a faulty net, and
  - The last ring contains $L_h$ net segments that are all passed by the ring only. It takes up to $L_h-1$ rings to distinguish these $L_h$ possible faults, and thus the maximum number of diagnosis rings is $|R_t| + (L_h-1)$. 
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Experimental Results  
for Interconnect Diagnosis both for  
Predetermined and Adaptive Methods

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Statistics</th>
<th>Predetermined</th>
<th>Analysis</th>
<th>Adaptive</th>
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<tr>
<td>xerox</td>
<td>10</td>
<td>2</td>
<td>16</td>
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<tr>
<td>Compar.</td>
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</tr>
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</table>
# Experimental Results – Concurrent Test Sessions

| Circuit | $|R_d|$ | $|R_c|$ (worst case) | $|R_d|-|R_c|$ |
|---------|-------|---------------------|----------------|
| ac3     | 374   | 373                 | 1 (0.27%)      |
| ami33   | 303   | 290                 | 17 (5.86%)     |
| ami49   | 386   | 352                 | 34 (9.66%)     |
| apte    | 122   | 119                 | 3 (2.52%)      |
| hp      | 164   | 160                 | 4 (2.50%)      |
| xerox   | 342   | 327                 | 15 (4.59%)     |
| Comparison | 1.0432 | 1 | 4.57% |
## Experimental Results – Comparison between Theoretical Bounds and Experimental Results

| Circuit | #NoDiag | #EqClass | (#NoDiag-#EqClass) | Extra Rings (|R_d|–|R_t|) | (#NoDiag-#EqClass) and (|R_d|–|R_t|) |
|---------|---------|----------|---------------------|----------------|----------------------------------|
| ac3     | 323     | 68       | 255                 | 241            | 14 (5.49%)                      |
| ami33   | 126     | 59       | 67                  | 61             | 6 (8.96%)                       |
| ami49   | 337     | 88       | 249                 | 230            | 19 (7.63%)                      |
| apte    | 94      | 40       | 50                  | 49             | 1 (2.00%)                       |
| hp      | 145     | 51       | 94                  | 82             | 12 (12.77%)                     |
| xerox   | 214     | 86       | 128                 | 124            | 4 (3.13%)                       |
| Comparison | 1.0712 | 1 | 6.64%               |                |                                  |
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Conclusion

- Present an Interconnect OR Test scheme for interconnect faults in SOC circuits
  - IORT scheme achieves 100% fault detection coverage for each net
  - IORD scheme achieves the maximum diagnosability for each net segment
- Present fast diagnosability check and diagnosis ring generation
  - with theoretical study and integrated them into the IORD algorithm
  - with difference around 6 or 7% between theoretical and experimental results
Conclusion (Cont’d)

- Two optimization techniques
  - Concurrent OR Test ($R_c$)
    - Under worst case scenario: average within 5% and up to 9.66%
  - Adaptive OR Test ($R_a$)
    - Improves by $1.23 \times$ to $2.38 \times$ compared with \textit{predetermined diagnosis} $R_d$
    - with difference of \textit{predetermined detection} IORT ($R_t$) by 3.21%
Thank you for your Kind Participation!