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Low-Power Design Methodology for Module-wise Dynamic Voltage and Frequency Scaling with Dynamic De-skewing Systems

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130 130th Anniversary

Outline

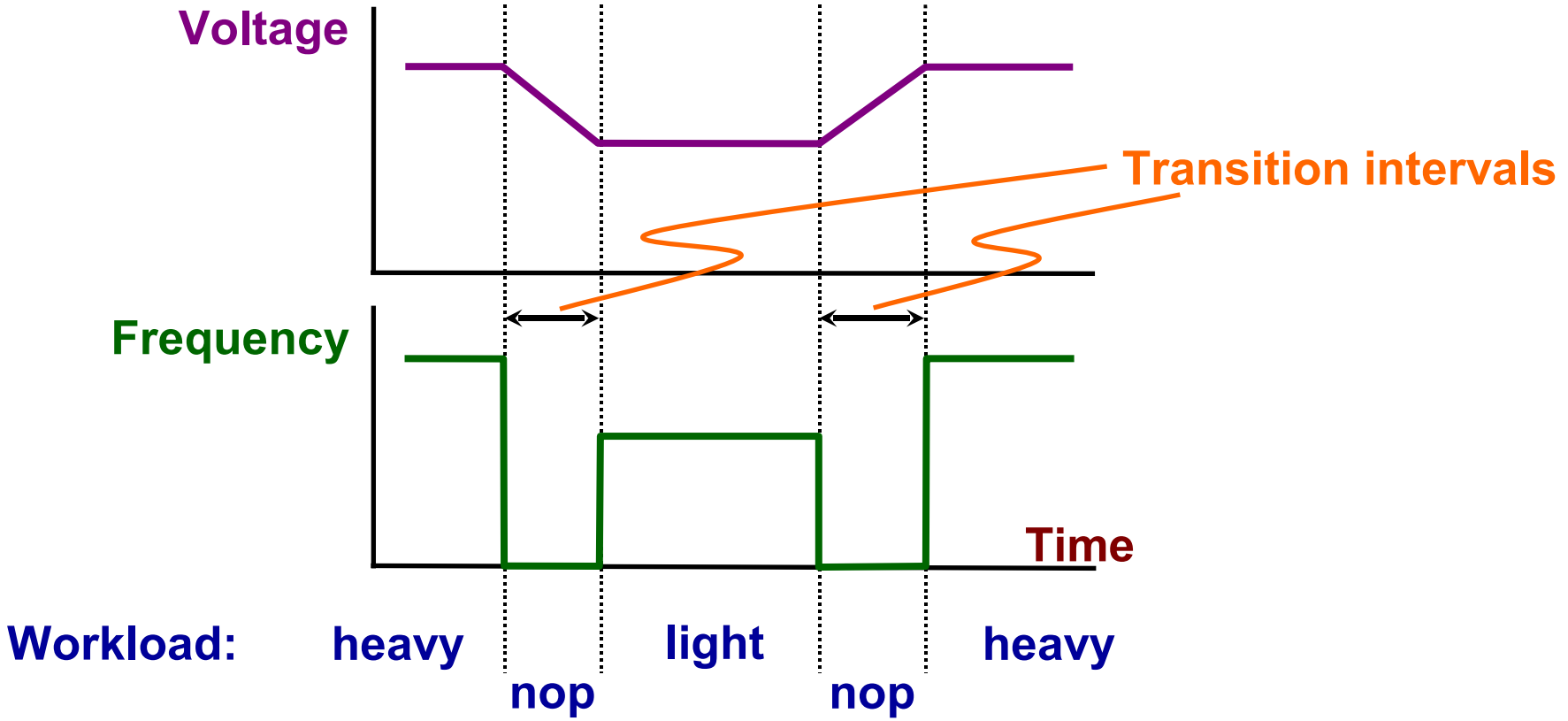
- Introduction
- Problem Definition
- Clock Design Methodology
- Experimental Results
- Conclusion

Introduction

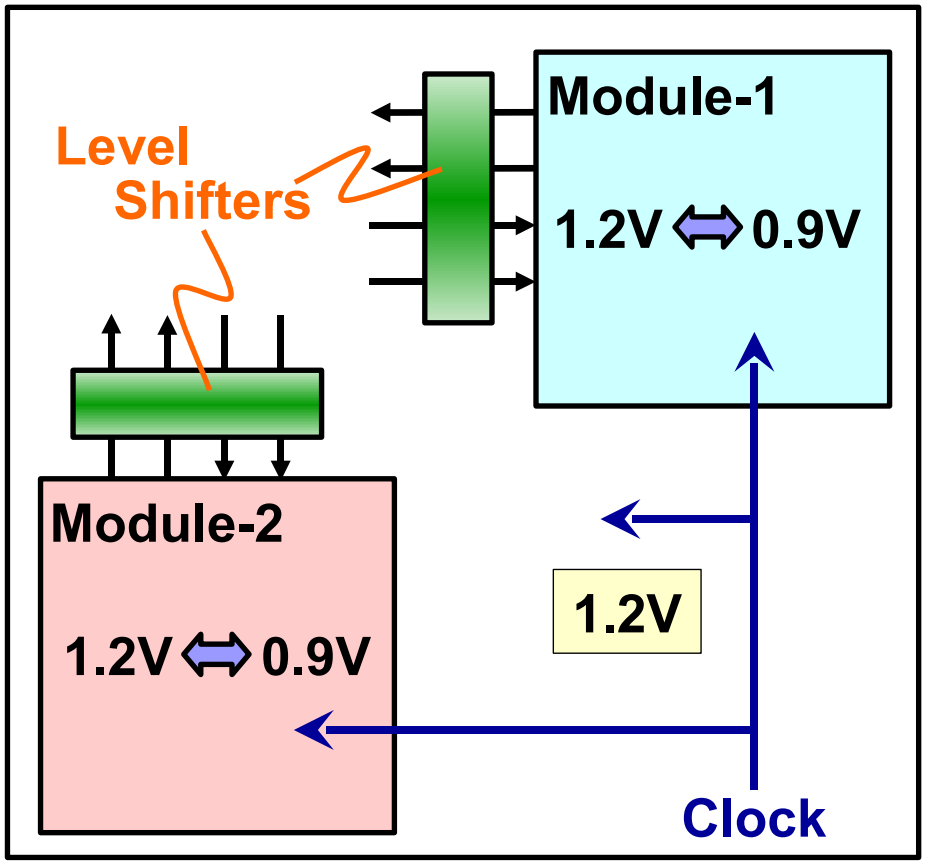
Dynamic Voltage and Frequency Scaling (DVFS):

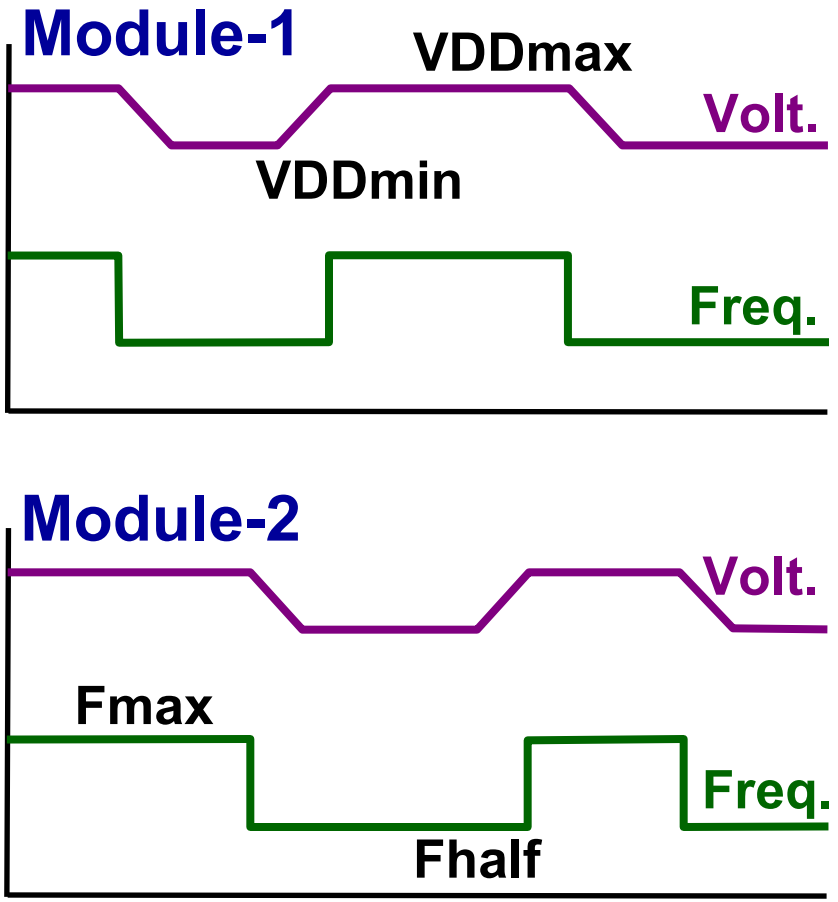
[Chip-wise]

ex. Intel Speedstep(R) technology
Transmeta LongRun™ technology



Module-wise DVFS





- Possibility of lowering supply voltage for Module-wise DVFS is larger than that of Chip-wise DVFS.
- Module can work at lower frequency while supply voltage changes, by using Dynamic De-skewing System.

Problem Definition

- Constructing clock design strategy for minimizing clock skew.
- Clarifying setup and hold timing constraints with clock skew taken into consideration.

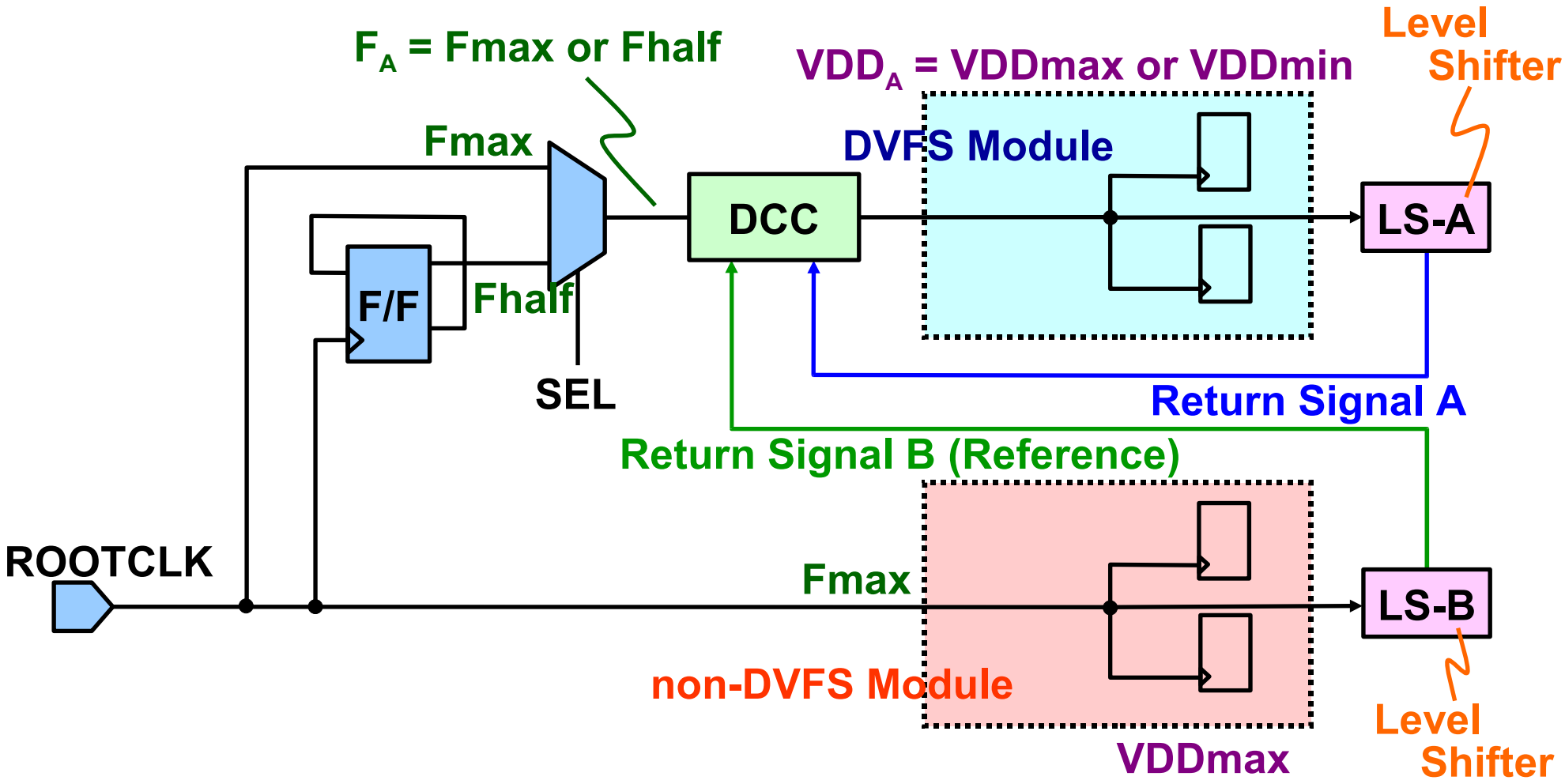
  => Module-wise DVFS
  with dynamic de-skewing system

- Determining supply voltage value for lower clock frequency.

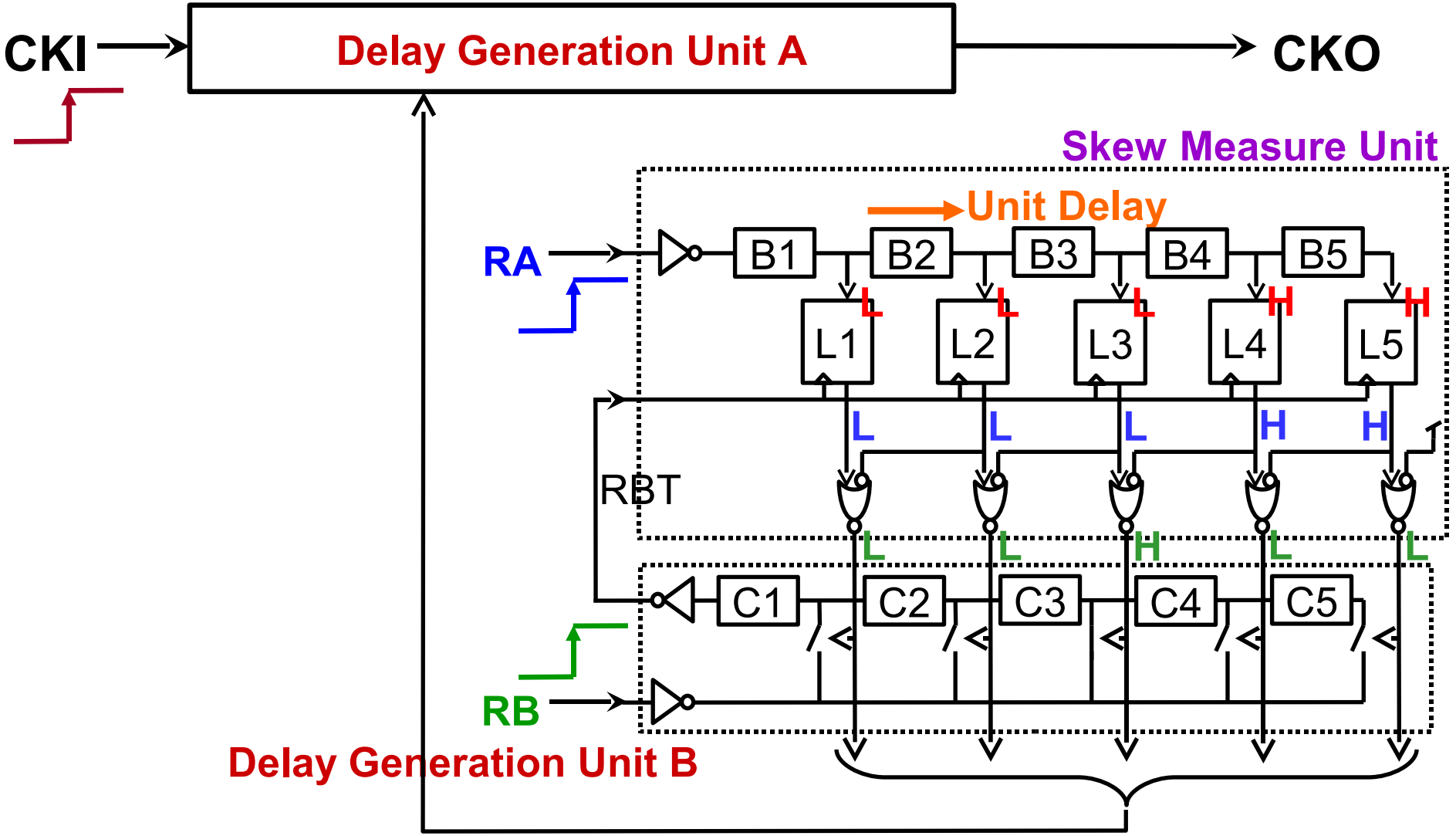
  => Module-wise DVFS, Chip-wise DVFS

Clock Network of Dynamic De-skewing System

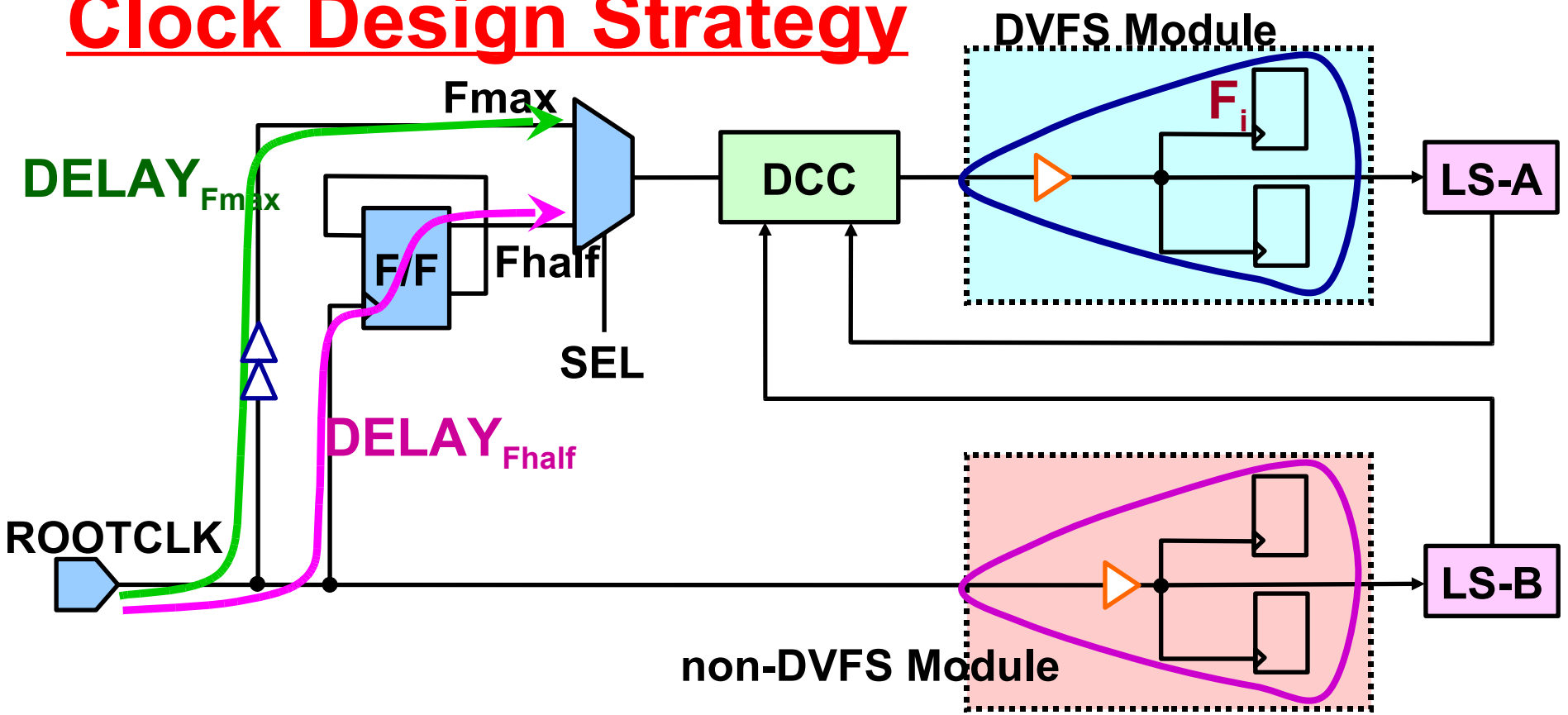
- Clock-delay changes in DVFS module, according to supply voltage.



Delay Control Circuit (DCC)



Clock Design Strategy



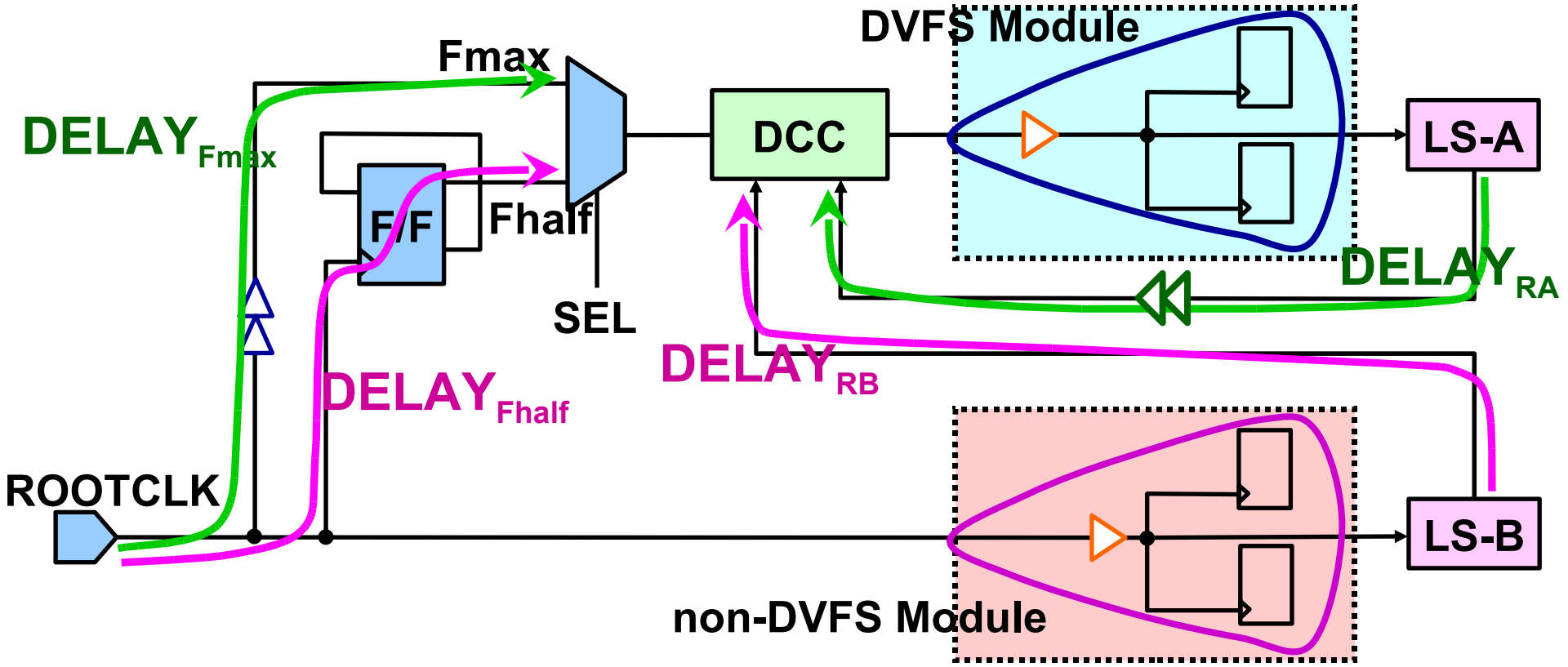
(1)Equalizing $DELAY_{Fmax}$ and $DELAY_{Fhalf}$, by adding delay buffers appropriately.

(2)Generating clock tree structure by adding clock buffers to DVFS and non-DVFS modules.

$$|DELAY_{Fi} - DELAY_{Fj}| < \beta \text{ for } \forall Fi, Fj \in \{F/F \text{ in DVFS or non-DVFS, LSA, LSB}\}$$

under $VDD_A = VDDmax$ β : maximum clock skew

Clock Design Strategy (Cont.)



(3)Equalizing $DELAY_{RA}$ and $DELAY_{RB}$, by adding delay buffers appropriately.

(4)Adding or removing one delay buffer on return signal, to adjust total delay.

Timing Constraints

- Setup and hold timing constraints can be expressed with three parameters for following two cases.

α : delay of minimum delay buffer

β : maximum clock skew among flip-flops

γ : unit delay in Delay Control Circuit (DCC)

(I) $VDD_A = VDDmax$, $F_A = Fmax$

(II) $VDDmin \leq VDD_A < VDDmax$, $F_A = Fhalf$

Scalable Polynomial Delay Model (SPDM)

- Cell delay can be expressed by three parameters.

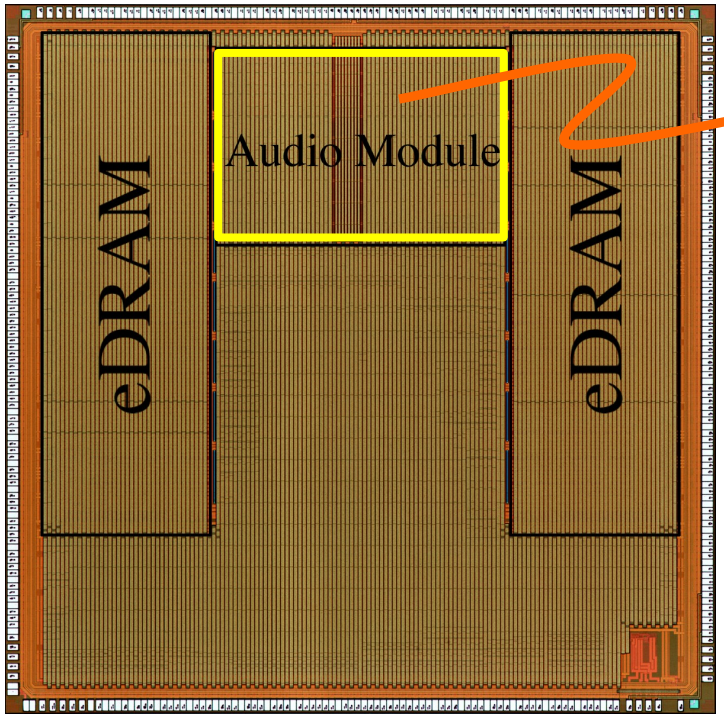
$$Delay = Delay(c,s,v) = \sum_{i,j,k=0}^{l,m,n} a_{ijk} * c^i * s^j * v^k$$

c : output capacitance
s : input slew
v : supply voltage

Path delay can be expressed by polynomial expression, so we can obtain value of *VDDmin* by solving *n*-th degree inequality.

Experimental Results

- H.264/MPEG-4 Audio/Visual Codec LSI [2]

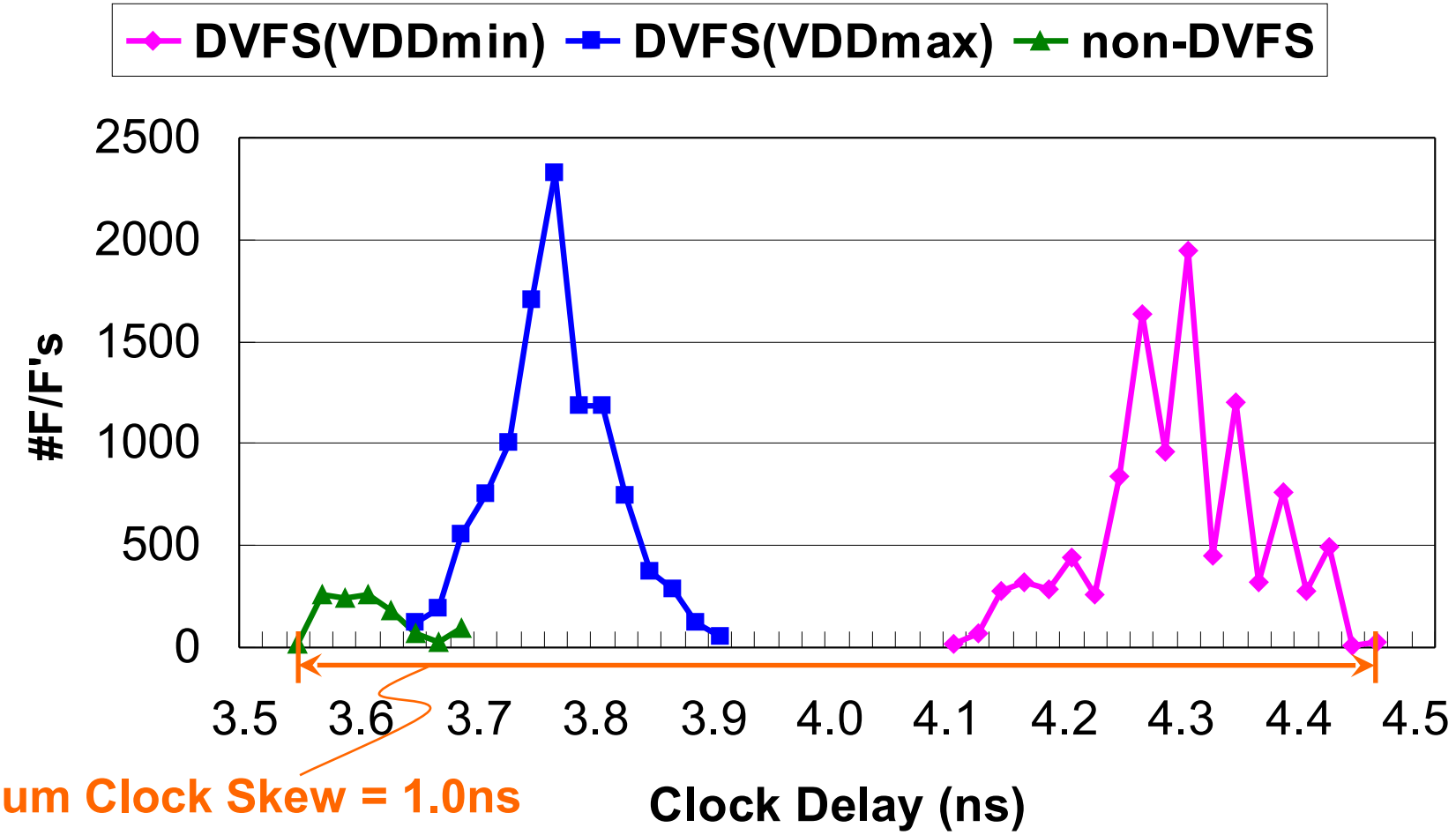


Module-wise DVFS technique was applied to "Audio Module".

90nm CMOS technology
Frequency : 180MHz/90MHz
Voltage:
1.2V/0.9V (DVFS module)
1.2V (non-DFVS module)
2.5V (eDRAM)

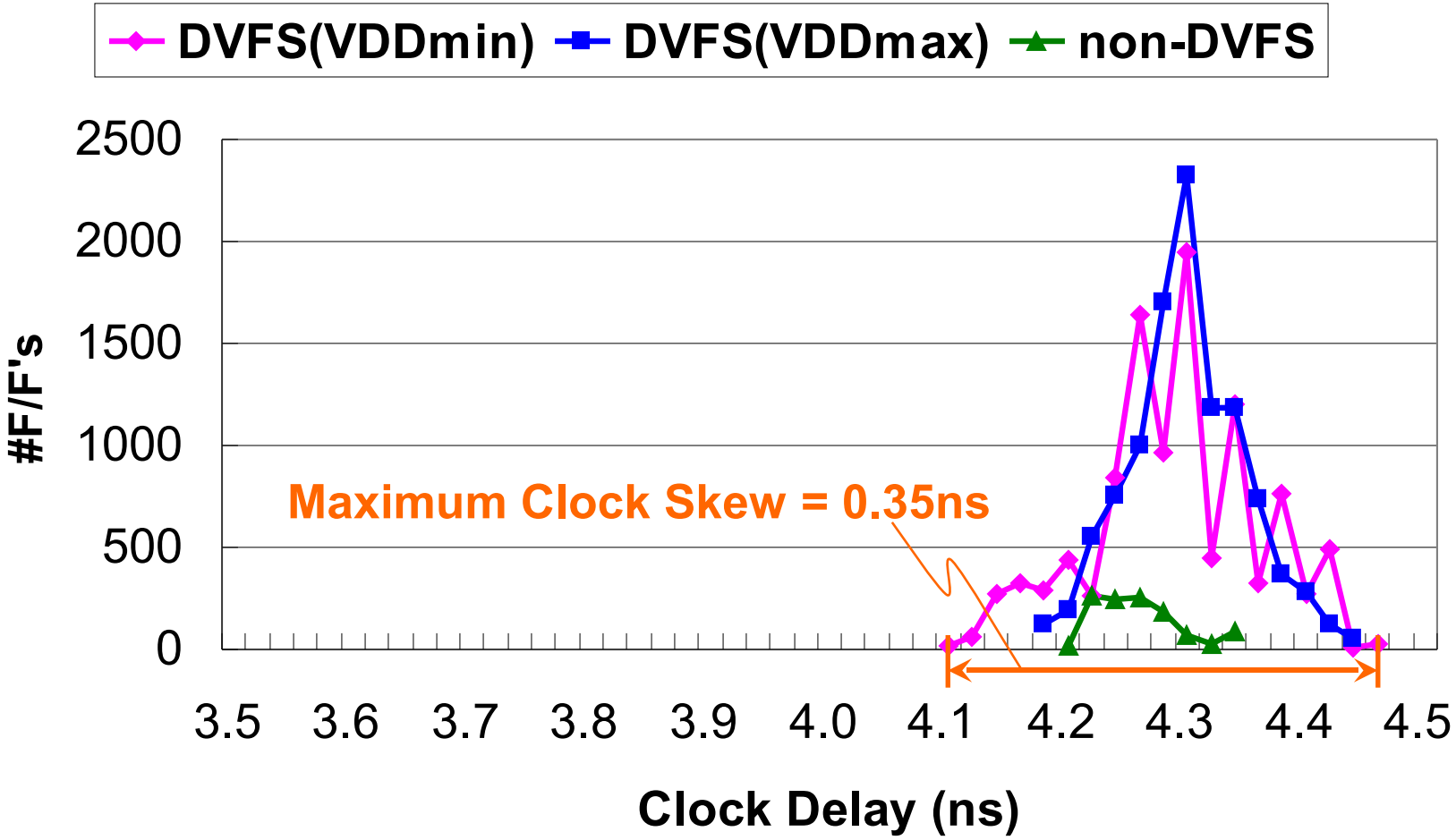
Clock Delay Distribution

- Without clock design methodology



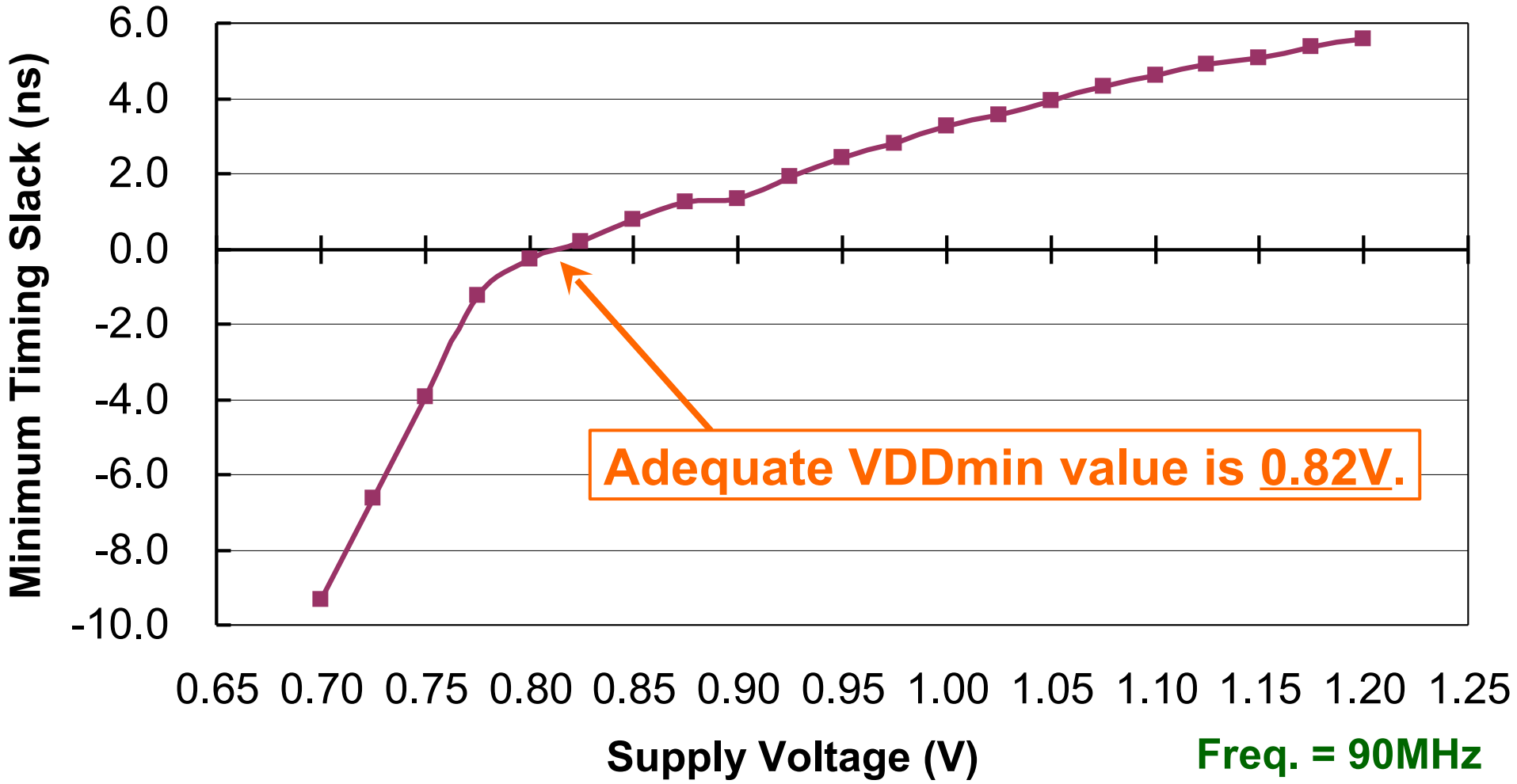
Clock Delay Distribution (Cont.)

- With clock design methodology



Timing Slack in DVFS module

- Timing was analyzed with SPDM library for various supply voltage.



Power Dissipation of Codec LSI

DVFS module (Audio Module)	Chip-wise (1.20V/0.90V)	Module-wise (1.20V/0.90V)	Module-wise (1.20V/0.82V)
decoding	5.3mW (100.0%)	2.5mW (47.1%)	2.1mW (39.6%)
encoding	6.8mW (100.0%)	3.3mW (48.5%)	2.7mW (39.7%)

DVFS module + non-DVFS modules	Chip-wise (1.20V/0.90V)	Module-wise (1.20V/0.90V)	Module-wise (1.20V/0.82V)
decoding	41.3mW (100.0%)	38.5mW (93.2%)	38.1mW (92.3%)
encoding	50.9mW (100.0%)	47.4mW (93.1%)	46.8mW (91.9%)

Conclusion

- Presented design methodology for module-wise DVFS.
- Explained clock design strategy to minimize clock skew between flip-flop in DVFS module and one in non-DFVS module.
- Showed effectiveness for reducing power through experimental results.

- If designers want to reduce power further more, design and circuit will become more complicated.
- To design such complicated LSI's, collaboration among circuit engineers, LSI engineers and methodology engineers has become more indispensable than ever.