Single-Chip Multi-Processor Integrating Quadruple 8-way VLIW Processors with interface timing analysis considering power supply noise

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Outline

- Motivation
- Architecture
- Physical design
  - Design flow considering power supply noise
  - LSI model for power integrity analysis
  - Interface analysis example
- MPEG2 MP@HL decoding on evaluation board
- Summary
Motivation: high performance and low power

Performance

<table>
<thead>
<tr>
<th></th>
<th>Previous work: FR550</th>
<th>This work: FR1000</th>
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<tr>
<td>Parallelism</td>
<td>Data-level</td>
<td>Instruction-level</td>
</tr>
<tr>
<td></td>
<td>SIMD</td>
<td>VLIW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Multi-thread</td>
</tr>
<tr>
<td></td>
<td>SDTV, etc.</td>
<td>HDTV, etc.</td>
</tr>
</tbody>
</table>

Thread-level
## FR1000 chip specifications

<table>
<thead>
<tr>
<th>Core</th>
<th>4 cores with 8-way VLIW architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td>32 KB+32 KB/core (D-cache, I-cache)</td>
</tr>
<tr>
<td></td>
<td>128 KB/core (Local memory)</td>
</tr>
<tr>
<td>DMA controller</td>
<td>16 ch (Internal), 16 ch (External)</td>
</tr>
<tr>
<td>Interface</td>
<td>Main memory 266 MHz 64 bit x 2 ch</td>
</tr>
<tr>
<td></td>
<td>System Bus 178 MHz 64 bit</td>
</tr>
<tr>
<td>Technology</td>
<td>90-nm CMOS, 9-metal layers</td>
</tr>
<tr>
<td>Transistor count</td>
<td>28M (Logic), 55M (Memory)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>533 MHz @1.2 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>3.0 W @1.2 V, 533 MHz</td>
</tr>
<tr>
<td>Package</td>
<td>900-pin FCBGA</td>
</tr>
<tr>
<td>size</td>
<td>11.9 mm x 10.3mm</td>
</tr>
</tbody>
</table>

High speed interface cause power supply noise issue.
Power integrity issue on system board

Technology scaling

- signal I/O frequency
- signal I/O number

Increase of noise

FR1000: 230SSTL I/O buffers, 2ch 266MHz

Timing analysis considering power supply noise of DIE, PKG and PCB is required
Design flow considering power supply noise

Conventional flow

- FR1000 RTL
- Synthesis
- Timing budget
- netlist
- Layout and timing analysis
- FR1000 netlist

Additional flow

- PKG design
- PCB design
- DIE Layout Data
- PKG Layout Data
- PCB Layout Data

Power supply noise analysis model

Timing margin analysis considering power supply noise

Very long analysis time!

Timing margin
LSI power analysis model
Our timing margin analysis flow

### Conventional flow
- **400K elements for FR1000 design**
- Power supply analysis model
- I/O stimulus
- Power supply noise analysis & delay penalty analysis
- Delay penalty
- Timing margin analysis
- Timing margin

**Simulation time**: 400 hours

### Our new flow
- Power supply analysis model
- I/O stimulus
- Transmission line model
- Power supply noise analysis
- Delay penalty analysis
- Power supply voltage waveform
- Timing margin analysis
- Timing margin

**Simulation time**: 12 hours
Transmission line model

Apply the power supply voltage waveforms of DIE, PKG, and PCB.
Delay penalty by power supply noise analysis method

Driver side
- Power supply noise (External power supply)
- Drived signal
- Power supply noise (Ground)

Receiver side
- Received signal (without power supply noise)
- Received signal (with power supply noise)
- Propagation time (without power supply noise)
- Worst case delay penalty

\[ \text{Worst case delay penalty} = \text{delay} - \text{delay} + \text{delay} \]
Analysis result of main memory interface

- Analysis conditions:
  - Process: slow
  - Voltage: VDE=2.3V, VDD=1.1V
  - Temperature: 125°
  - I/O: All active
  - Core logic: stop

- Results:
  - Clock-Address Setup: 28.9%
  - Clock-Address Hold: 26.0%
  - DQS-DQ Setup: 36.5%
  - DQS-DQ Hold: 36.6%
  - Clock-DQS Skew: 35.4%

- The margin without considering any delay penalty.
PCB/Package design guideline

DQ-DQS interface timing analysis result

Timing budget = 1.38 ns

tDS = 0.5 ns

On die variation
PKG/PCB skew
PKG/PCB Xtalk
Delay penalty by noise

Timing margin [ns]

0.5 1.0 1.5

PCB/Package design guideline

- Power
  Plane resource, Decoupling capacitors

- Signal
  Layer usage, Line width/length/spacing
MPEG2 MP@HL decode for HDTV on FR1000
Summary

The low power single-chip multi-processor FR1000

-4 processor cores, internal DMAC, external DMAC
-MPEG2 MP@HL without any dedicated circuits
-3.0W@1.2V, 533MHz

Introducing interface timing analysis considering power supply noise

-DIE(LSI) noise model development
-Timing analysis method at shorter times