Low-Overhead Design of Soft-Error-Tolerant Scan Flip-Flops with Enhanced-Scan Capability

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Motivation

- Critical charge: $Q_c$
- Scaling: $C \downarrow$, $V \downarrow$, $Q_c \downarrow$
- Unlike memories flip flops not protected by parity and ECC
- Cross-coupled inverters
- Feedback increases soft error vulnerability
Motivation

- Reuse of on chip scan design-for-testability (DFT) resources to reduce overhead
- Integration of soft error tolerant flip-flops into the scan path

Scan Flip-flop design of a Microprocessor*

Soft Error in Transmission Gate Flip-Flop

- **Clk = 1**, Master Stage susceptible
- **Clk = 0**, Slave Stage susceptible
- Need a redundant copy for soft error detection / correction
Reuse of On Chip Scan DFT resources

Scan Reuse for Soft Error blocking* (ISR)

- Scan latches sized up to store a copy of data, increases area and power overhead
- Four latches required to store the two copies of the data

Test Mode TC = ‘0’
HOLD = ‘0’
Proposed Design (Contd.)

Normal Mode TC = ‘1’

Implicit Pulsing
Proposed Design (Contd.)

Normal Mode TC = ‘1’

CLK = ‘0’

CLK = ‘1’

C-element
### ESFF-SEC vs. ISR

<table>
<thead>
<tr>
<th></th>
<th>ESFF-SEC</th>
<th>ISR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>1.0</td>
<td>1.26</td>
</tr>
<tr>
<td>Area</td>
<td>1.0</td>
<td>1.61</td>
</tr>
<tr>
<td>Setup Time</td>
<td>1.0</td>
<td>1.70</td>
</tr>
<tr>
<td>C-to-Q Delay</td>
<td>1.0</td>
<td>1.00</td>
</tr>
</tbody>
</table>

- Power and Area - Reduction in the number of latches from four to three
- Setup time - Scan Latch is sized up in ISR, more load on the data driver
During $t_d$ if soft error in $L1$, it propagates to both $QD$ and $SO$. 
Proposed Design for Enhanced Scan and Soft Error Detection (ESFF-SED)
Scan Gadget Scheme (HSSG)*

- **Scan Gadget Scheme (HSSG)** – uses a Scan Gadget along with system latch to scan in and hold test vector
- **Overhead** – extra latch, complicated design of system flip-flop requiring two clocks and extra timing signals required (SCANCLK, SHIFT)

Proposed Design for Enhanced Scan Delay Testing (ESFF)

- Drivers $I_1$ and $I_2$ converted into latch $L3$ using $T_3$ and $T_4$
- Normal Mode, $TC = '1'$, $T_4$ is OFF and $T_3$ is ON
- Test Mode, $TC = '0'$, $T_3$ is OFF and $T_4$ is ON, $L3$ disconnected from $L2$ and $L1$, acts as a hold latch
- No extra timing control signals required
Results

• HSPICE simulation of ISCAS89 benchmarks in BPTM 70nm node

• 16% power and 17% area reduction on average at no delay overhead

• % of sequential elements in the benchmark decrease from 74% in s13207 to 22% in s1196, hence total savings decrease
Conclusion

• Novel Flip-Flop designs are proposed having soft error detection/correction capability along with enhanced scan based delay fault testing

• A simplified version having enhanced scan delay fault testing capability is proposed

• Low area and power overhead due to reuse of existing hardware resources
Thank You!

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## C-element and Keeper

<table>
<thead>
<tr>
<th>O1</th>
<th>O2</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Previous Value</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Previous Value</td>
</tr>
</tbody>
</table>

- Keeper is used to retain the previous value when O1 and O2 are different from each other.