An Approach to
Topology Synthesis of Analog Circuits
Using Hierarchical Blocks and
Symbolic Analysis

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Outline

- Introduction
- Topology generation
  - Hierarchical blocks
  - Synthesis rules
- Topology selection
  - Symbolic analysis
- Synthesis results
- Conclusion
Motivation

- Automatic design of analog circuits
  - Support for designer
  - Reduce time to market
- Exploration of structural design space
  - Find appropriate circuits methodically and systematically
  - Analyze and evaluate performances quickly
Hierarchical View of Circuits

- Sizing tools (e.g. WiCkeD)
- Topology synthesis, e.g.:
  - Rutenbar et al. (OASYS): topology library
  - Dastidar et al.: genetic algorithm
  - Our: rules-based algorithm
Hierarchical Topology Synthesis

- A set of well-defined blocks with specialized signal information of terminals
- Synthesis rules for combination between blocks
- Block-chains/nets can represent the topology of circuits
Block with terminal info

- Type of signal: voltage \( (U) \) or current \( (I) \)
  - Current direction: determined by the bias current
- Type of terminal: input or output
- Impedance: low or high
Examples of blocks

- Differential pair

- Current source

- Current mirror (basic & cascode)
Synthesis rules

- General rules
  - Connection between two blocks
  - One dimension

- Current source rule
  - Adding Current source between two blocks
  - Quasi-one dimension

- Split & combination rules
  - Expanding the connection between blocks
  - Two dimensions
General rules

- Signal type rule
  - current to current, voltage to voltage

- Current rule
  - Matched bias current direction
  - Low input impedance of block B

- Voltage rule
  - High input impedance of block B
Current Source Rule

- Block A with current source can be treated as a block with either current or voltage output.

- E.g. folded cascode
Split & Combination Rules

- **Split rule (voltage)**

- **Combination rule (current)**

- Typical application area: differential pair
Topography Generation – Work Flow

specification

terminal info

max size of block-chains

hierarchical block-chain/net generation

rules

transformation to topology

diff-pair
resistor
cascode stage
current mirror
cascode current mirror

transform

symbolic analysis

sizing

X. Wang ASPDAC 2006
Topology Selection – Symbolic Analysis

- Goal of topology selection
  - Reduce high number of synthesized circuits
  - Short run time

- Symbolic analysis
  - Fast performance estimation
  - Performance $\Leftrightarrow$ parameter dependencies
  - Simple design equations $\Rightarrow$ Initial sizing
Symbolic Analysis – Work Flow

**topology generation**

**linear symbolic analysis**

- linear transistor model
- set-up
- simplify solute
- transfer function

**performance evaluation**

- Performance = \( f(W_1, ..., W_n, L_1, ..., L_n, I_{Bias1}, ..., I_{Biasn}) \)
- with \( \forall i \ W_i \in [W_{min}, W_{max}] \), \( L_i \in [L_{min}, L_{max}] \), \( I_{Biasi} \in [I_{Bias min}, I_{Bias max}] \)

**sizing**

- compare to spec.
Performance Estimation

- Linear performances
- Structural constraints
- Parameter dependencies given by symbolic expressions

Parameter Space

Gain

Performance Space

f_1(W_1, L_j, I_{Bias_k}), f_2(…)

X. Wang  ASPDAC 2006

L_1 \rightarrow L_2=L_1

W_1 \rightarrow W_2
Results – Unbuffered Op Amp (I)

- Op amp without a buffered output stage
- Terminal information:
  - Differential voltage input with high impedance
  - Voltage output with high impedance
Results – Unbuffered Op Amp (II)

ΔU input
U output
#block ≤ 4

gain ≥ 80dB,
f_c ≥ 1MHz,
R_{out} ≥ 400kΩ

blocknet generation
448

transformation

Run time: ca. 2h

selection - symbolic analysis

\[ W, L = [1 \cdot 10^{-7} \ldots 2 \cdot 10^{-5}] \]
\[ I_{Bias} = [0.01 \cdot 10^{-6} \ldots 0.2 \cdot 10^{-6}] \]
Results – Unbuffered Op Amp (III)

- 1 of 50 results: block-net

- Schematic

- Estimated performances
  - gain = 81.3 dB
  - $f_c = 1.01$MHz,
  - $R_{out} = 5\Omega$
Conclusion

- A new concept of circuit synthesis
  - Exhaustive exploration of structural space with respect to
    - Predefined hierarchical blocks
    - Structural restrictions by rules
    - Limited size of block chain
  - Symbolic analysis
    - Fast performance evaluation
  - First results for standard linear circuits
Future work

- Circuit classes
  - Mixer, output stage
  - ...
- Automatic Sizing
Thank you!