2nd Call for Papers
ASP-DAC 2006

Asia and South Pacific Design Automation Conference 2006

http://www.aspdac.com/aspdac2006/

January 24 – 27, 2006

Pacifico Yokohama, Yokohama, JAPAN

Aims of the Conference:

ASP-DAC 2006 is the eleventh in a series of annual international conferences on VLSI design automation. Asia and South Pacific region is one of the most active regions of design and fabrication of silicon chips in the world. The conference aims are providing the Asian and South Pacific CAD/DA and Design community with opportunities of interchanging ideas and collaboratively discussing the directions of the technologies related to all of Electronic Design Automation (EDA). The goal of the conference is to provide a forum for presentation, discussion, and observation of the state-of-the-art of EDA technologies and design methodologies of electronic systems. The format of the meeting intends to cultivate and promote an instructive and productive interchange among EDA researchers/developers, and system/circuit/device designers. A wide variety of those scientists, engineers, and students who are interested in theoretical issues on EDA are also welcome.

Area of Interest:

Original papers on, but not limited to, the following areas are invited.

[1] System Level Design Methodology:
System VLSI and SOC design methods, System specification, Specification languages, Design languages, Design reuse and IPs, Platform-based design, Network on chip design

[2] Embedded and Real-Time Systems:
Hardware-software co-design, Co-simulation, Co-verification, Real-time OS and middleware, Design language for embedded systems, Compilation techniques, ASIP synthesis

[3] Behavioral/Logic Synthesis and Optimization:
Behavioral/RTL synthesis, Technology independent optimization, Technology mapping, Interaction between logic design and layout, Sequential and asynchronous logic synthesis

[4] Validation and Verification for Behavioral/Logic Design:
Logic simulation, Symbolic simulation, Formal verification, Equivalence checking, Transaction-level/RTL and gate level modeling and validation

[5] Physical Design (Routing):
Routing, Repeater issues, Interconnect optimization, Interconnect planning, Module generation, Layout verification

[6] Physical Design (Placement):
Placement, Floorplanning, Partitioning, Hierarchical design,

[7] Timing, Power, Signal/Power Integrity Analysis and Optimization:
Timing analysis, Power analysis, Signal/power integrity, Clock and global signal design

[8] Interconnect, Device and Circuit Modeling and Simulation:
Interconnect modeling, Interconnect extraction, Package modeling, Circuit simulation, Device modeling/simulation, Library design, Design fabrics, Design for manufacturability, Yield optimization, Reliability analysis, Emerging technologies

[9] Test and Design for Testability:
Test design, Fault modeling, ATPG, BIST and DFT, Memory, core and system test

[10] Analog, RF and Mixed Signal Design and CAD:
Analog/RF synthesis, Analog layout, Verification, Simulation techniques, Noise analysis, Analog circuit testing, Mixed signal design

[11] Leading Edge Design Methodology for SOCs and SIPs:
Microprocessors, DSP, IP-core design, Design for multimedia, Design for wireless communication, A/D mixed circuits, Memories, Sensors, MEMS chips, FPGA design, Novel reconfigurable systems, Rapid prototyping

Submission of Papers:

Deadline for submission:	**July 20 (Wed), 2005**
Notification of acceptance:	**September 30 (Fri), 2005**
Deadline for final version:	**November 18 (Fri), 2005**

Specification of the paper submission format will be available at our WEB site:
`http://www.aspdac.com/aspdac2006/`

Panels, Special Sessions and Tutorials:

Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (e-mail: `aspdac2006@aspdac.com`) no later than **June 10(Fri.), 2005**.

Prospective Sponsors:

ACM SIGDA, IEEE Circuits and Systems Society, IEICE ESS (Institute of Electronics, Information and Communication Engineers, Engineering Sciences Society), IPSJ SIG-SLDM (Information Processing Society of Japan, SIG System LSI Design Methodology)

ASP-DAC2006 Chairs:

General Chair: Fumiyasu Hirose (Cadence)
Technical Program Chair: Hidetoshi Onodera (Kyoto Univ.)
Technical Program Vice Chair: Yusuke Matsunaga (Kyushu Univ.)

Conference Secretariat:

Please contact Conference Secretariat (`e-mail:aspdac2006@aspdac.com`), if you have questions or comments.