Highlights

Keynote Addresses

Wednesday, January 25, 9:00-10:00, Small Auditorium, 5F

“Automotive Electronics: Steady Growth for Years to Come!”
Alberto Sangiovanni-Vincentelli - The Edgar L. and Harold H. Buttnn Chair of Electrical Engineering and Computer Science, Univ. of California, Berkeley, and Chief Technology Advisor, Member of the Board and Co-founder, Cadence Design Systems, United States

Thursday, January 26, 9:00-10:00, Small Auditorium, 5F

“Challenging Device Innovation”
Satoru Ito - President & CEO, RENESAS Technology Corp., Japan

Friday, January 27, 9:00-10:00, Small Auditorium, 5F

“Effective Platform-based Development for Large-scale Systems Design”
Yukichi Niwa - Senior Advisory Director, Group Executive of Platform Technology Development Headquarters, CANON INC., Japan

Special Sessions

1D: Wednesday, January 25, 10:15-12:20, Room 416+417

“Presentation + Poster Discussion: University Design Contest”

2D: Wednesday, January 25, 13:30-15:35, Room 416+417

“Invited Talks: Electrothermal Design of Nanoscale Integrated Circuits”

2D-1: Electrothermal Analysis and Optimization Techniques for Nanoscale Integrated Circuits
Yong Zhan, Brent Goplen, Sachini S. Sapatekar (Univ. of Minnesota, United States)

2D-2: Electrothermal Engineering in the Nanometer Era: From Devices and Interconnects to Circuits and Systems
Kaustav Banerjee, Sheng-Chih Lin, Navin Srivastava (Univ. of California, Santa Barbara, United States)

2D-3: Area Optimization for Leakage Reduction and Thermal Stability in Nanometer Scale Technologies
Ja Chun Ku, Yehea Ismail (Northwestern Univ., United States)

2D-4: Compact Thermal Models for Estimation of Temperature-dependent Power/Performance in FinFET Technology

3D: Wednesday, January 25, 16:00-18:05, Room 416+417

“Invited Talks: Flash Memory in Embedded Systems”

3D-1: Current Trends in Flash Memory Technology
Sang Lyul Min, Eyee Hyun Nam (Seoul National Univ., Republic of Korea)

3D-2: Configurability of Performance and Overheads in Flash Management
Tei-Wei Kuo, Jon-Wei Hsieh (National Taiwan Univ., Taiwan), Li-Pin Chang (National Chiao-Tung Univ., Taiwan), Yuan-Hao Chang (National Taiwan Univ., Taiwan)

4D: Thursday, January 26, 10:15-12:20, Room 416+417

“Invited Talks: Open Access Overview”

4D-1: An Introduction to OpenAccess - An Open Source Data Model and API for IC Design
Michaela Guiney, Eric Leavitt (Cadence, United States)

4D-2: Open Access Overview "Industrial Experience"
Yosio Inoue (Renesas, Japan)

4D-3: EDA Vendor Adoption
Hillel Ofek (Sagantec, United States)

4D-4: Utility of the OpenAccess Database in Academic Research
David Papa, Igor Markov (Univ. of Michigan, United States), Phillip Chong (Cadence Design Systems, United States)

7D: Friday, January 27, 10:15-12:20, Room 416+417

“Invited Talks + Panel Discussion: H.264/AVC Design Challenges and Solutions”

7D-1: Introduction to H.264 Advanced Video Coding
Jian-Wen Chen, Chao-Yang Kao, Youn-Long Lin (National Tsing Hua Univ., Taiwan)

7D-2: Algorithm and DSP Implementation of H.264/AVC Video Codec
Tung-Chien Chen, Chung-Jr Lian, Liang-Gee Chen (Univ. of California, Santa Barbara, United States)

7D-3: Hardware Architecture Design of an H.264/AVC Video Codec
Sung Dae Kim, Jeong Hoo Lee, Chung Jin Hyun, Myung Hoon Sunwoo (Ajou Univ., Republic of Korea)

7D-4: ASP Approach for Implementation of H.264/AVC

7D-5: Panel Discussion
Designers’ Forum

5D: Thursday, January 26, 13:30-15:30, Small Auditorium, 5F
“Invited Talks: Low Power Design”

5D-1: Low-Power Design Methodology for Module-wise Dynamic Voltage and Frequency Scheduling with Dynamic De-skewing Systems
- Takeshi Kitahara, Hiroyuki Hara, Shinichiro Shiratake (Toshiba, Japan), Yoshiki Tsukiboshi (Toshiba Microelectronics, Japan), Tomoyuki Yoda, Tetsuaki Utsumi, Fumihiro Minami (Toshiba, Japan)

- Satoshi Imai, Atsuki Inoue, Motoaki Matsumura, Kenichi Kawasaki, Atsuhiro Suga (Fujitsu Lab., Japan)

5D-3: A System-level Power-estimation Methodology based on IP-level Modeling, Power-level Adjustment, and Power Accumulation
- Masaumi Onouchi, Tetsuya Yamada (Hitachi Ltd., Japan), Kinmiro Morikawa, Isamu Mochizuki, Hidetoshi Sekine (Renesas, Japan)

5D-4: PowerVIP: SoC Power Estimation Framework at Transaction Level
- Ikkwon Lee, Hyunsuk Kim, Peng Yang, Sungjoo Yoo (Samsung Electronics, Republic of Korea), Eui-Young Chung (Yonsei Univ., Republic of Korea), Kyu-Myung Choi, Jeong-Taek Kong, Soo-Kwan Eo (Samsung Electronics, Republic of Korea)

6D: Thursday, January 26, 18:30-19:00, Small Auditorium, 5F
“Panel Discussion: Functional Verification -now and future-“
Organizer: Haruyuki Tago (TOSIBA)
Moderator: Yoshiaaki Hagihara (Sony)
Panelists: Raul Camposano (Synopsys), Sudeep Pasricha (PDF Solutions, Inc. and CMU), Joe Sawichi (Mentor), Nikil Dutt (UCSD and Blaze DFM), Andrzej Strojwas (PDF Solutions, Inc. and CMU)

Two Full-Day and Four Half-Day Tutorials

FULL-DAY Tutorials:
Tuesday, January 24, 2006, 9:30-17:00

1 DFM Tools and Methodologies for 65nm and Below
Organizer: Andrew B. Kahng -UCSD and Blaze DFM, Inc., United States
Speakers: Andrew B. Kahng -UCSD and Blaze DFM, Inc., United States, Louis K. Schetther -Cadence Design Systems, Inc., United States, Michael Orshansky -Univ. of Texas, Austin, United States, Andrzej Strojwas -PDF Solutions, Inc. and CMU, United States

2 High Performance Interconnect and Packaging
Organizers: Chung-Kuon Cheng -Univ. of California, San Diego, United States, Howard Chen -IBM, United States, Paul M. Harvey -IBM, United States, Manjit Borah -Fairchild, United States, Lei He -Univ. of California, Los Angeles, United States, Sheldon Tan -Univ. of California, Riverside, United States

Speakers: Paul M. Harvey -IBM, United States, Howard Chen -IBM, United States, Chung-Kuan Cheng -Univ. of California, San Diego, United States, Paul M. Harvey -IBM, United States, Manjit Borah -Fairchild, United States, Lei He -Univ. of California, Los Angeles, United States, Sheldon Tan -Univ. of California, Riverside, United States

Tuesday, January 24, 2006, 9:30-12:30

3 Low Power / Low Leakage Technologies for Nanometer Era: System and Architecture Level Approaches
Organizer: Kimiyoshi Usami -Shibaura Inst. of Tech., Japan
Speakers: Naohiko Irie -Hitachi Ltd., Japan, Hiroshi Nakamura -Univ. of Tokyo, Japan

Tuesday, January 24, 2006, 14:00-17:00

4 Low Power / Low Leakage Technologies for Nanometer Era: Circuit and Device Level Approaches
Organizer: Kimiyoshi Usami -Shibaura Inst. of Tech., Japan
Speakers: Kimiyoshi Usami -Shibaura Inst. of Tech., Japan, Tohru Mogami -NEC Corporation, Japan

Tuesday, January 26, 2006, 16:30-18:00

5 Basics and Practice of Current Functional Verification Methods
Organizer: Kiyoharu Hamaguchi -Osaka Univ., Japan
Speakers: Kiyoharu Hamaguchi -Osaka Univ., Japan, Erich Marschner -Cadence Design Systems, Inc., United States

Tuesday, January 26, 2006, 9:30-12:30

6 SoC Communication Architectures: Current Practice, Research and Trends
Organizer: Nikil Dutt -Univ. of California, Irvine, United States
Speakers: Nikil Dutt -Univ. of California, Irvine, United States, Sudeep Pasricha -Univ. of California, Irvine, United States
Welcome to ASP-DAC 2006

On behalf of the Organizing Committee, I would like to welcome you to the Asia and South Pacific Design Automation Conference 2006 (ASP-DAC 2006). ASP-DAC is a sister conference of DAC, DATE and ICCAD, and it is the 11th event of this conference series. ASP-DAC 2006 will be held at Pacific Yokohama, Japan, from January 24 through 27, 2006, jointly with the Electronic Design and Solution Fair 2006.

ASP-DAC is the meeting place where researchers and engineers come together to learn and discuss state of the art technologies of system/SoC design, EDA and design methodologies. In 2006, we put special effort into attracting designers and design industries to produce Designers’ Forum.

We have three keynote speakers from academia, the semiconductor industry and the systems industry. Professor Alberto Sangiovanni-Vincentelli, University of California at Berkeley, will explore future system design perspectives in automotive electronics. Satoru Ito, President & CEO of NEXUS Technology Corp. will discuss challenges of device innovation. Yukichi Niwa, Senior Advisory Director of CANON INC. will present the company’s key concept of architecting platform based design.

The technical program was selected from 424 papers from 27 countries. The 64 members of the Technical Program Committee chaired by Professor Onodera and helped by over 250 reviewers had to make difficult choices to carefully select 135 papers. It is an outstanding program that covers a variety of key topics from system level design to physical design.

Designers’ Forum is a new program that shares design experience and solutions of real product designs of the industries whose topics include the CELL and mobile designs, panels of top 10 design issues and system verification. The University Design Contest is also an important event of ASP-DAC, which focuses on a real chip design in academia. On Tuesday, two full-day and four half-day tutorials are scheduled to provide introductions to hot topics like DFM, low-power, packaging/interconnect, system level design and verification.

I hope you will have a productive and exciting experience at ASP-DAC 2006. We look forward to meeting with you in Yokohama.

Fumiyasu Hirose
General Chair
ASP-DAC 2006
### TPC Subcommittees

(* indicates the subcommittee chair.)

#### [1] System Level Design Methodology

- **Youn-Long Lin**
  National Tsing Hua University  
- **Soonhoi Ha**
  Seoul National University  
- **Ahmed Jerraya**
  TIMA

- **Tsuneo Nakata**
  Fujitsu Lab.  
- **Yoshinori Takeuchi**
  Osaka University

**Youn-Long Lin**
National Tsing Hua University  
**Soonhoi Ha**
Seoul National University  
**Ahmed Jerraya**
TIMA


- **Hiroyuki Tomiyama**
  Nagoya University  
- **Pai Chou**
  University of California, Irvine  
- **Tei-Wei Kuo**
  National Taiwan University

- **Sri Parameswaran**
  University of New South Wales  
- **Sungjoo Yoo**
  Samsung

**Hiroyuki Tomiyama**
Nagoya University  
**Pai Chou**
University of California, Irvine  
**Tei-Wei Kuo**
National Taiwan University

#### [3] Behavioral/Logic Synthesis and Optimization

- **Kiyoungh Choi**
  Seoul National University  
- **Shih-Chieh Chang**
  National Tsing Hua University  
- **Shinji Kimura**
  Waseda University

- **Diana Marculescu**
  Carnegie Mellon University  
- **Shigeru Yamashita**
  AIST Nara

**Kiyoungh Choi**
Seoul National University  
**Shih-Chieh Chang**
National Tsing Hua University  
**Shinji Kimura**
Waseda University

#### [4] Validation and Verification for Behavioral/Logic Design

- **Kiyoharu Hamaguchi**
  Osaka University  
- **Jin-Young Choi**
  Korea University  
- **Shin’ichi Minato**
  Hokkaido University

- **Karem Sakallah**
  University of Michigan  
- **Farn Wang**
  National Taiwan University

**Kiyoharu Hamaguchi**
Osaka University  
**Jin-Young Choi**
Korea University  
**Shin’ichi Minato**
Hokkaido University

#### [5] Physical Design (Routing)

- **Martin D. F. Wong**
  University of Illinois, Urbana Champaign  
- **Tong Jing**
  Tsinghua University  
- **Youichi Shiraishi**
  Gunma University

- **Atsushi Takahashi**
  Tokyo Institute of Technology  
- **Ting-Chi Wang**
  National Tsing Hua University

**Martin D. F. Wong**
University of Illinois, Urbana Champaign  
**Tong Jing**
Tsinghua University  
**Youichi Shiraishi**
Gunma University

#### [6] Physical Design (Placement)

- **Shin’ichi Wakabayashi**
  Hiroshima City University  
- **Yao-Wen Chang**
  National Taiwan University  
- **Jason Cong**
  University of California, Los Angeles

- **Shigetoshi Nakatake**
  University of Kitakyushu  
- **Evangeline F. Y. Young**
  Chinese University of Hong Kong

**Shin’ichi Wakabayashi**
Hiroshima City University  
**Yao-Wen Chang**
National Taiwan University  
**Jason Cong**
University of California, Los Angeles


- **Sachin Sapatnekar**
  University of Minnesota  
- **Shabbir Batterywala**
  Synopsys (India)  
- **Jin-Jia Liu**
  National Taiwan University  
- **Takashi Sato**
  Renesas

- **Weiping Shi**
  Texas A&M University  
- **Youngsoo Shin**
  KAIST  
- **Sheldon Tan**
  University of California, Riverside  
- **Ryuichi Yamaguchi**
  Matsushita

**Sachin Sapatnekar**
University of Minnesota  
**Shabbir Batterywala**
Synopsys (India)  
**Jin-Jia Liu**
National Taiwan University  
**Takashi Sato**
Renesas

#### [8] Interconnect, Device and Circuit Modeling and Simulation

- **Hideki Asai**
  Shizuoka University  
- **Arun Chandrasekhar**
  Intel (India)  
- **Charlie Chung-Ping Chen**
  National Taiwan University  
- **Eli Chiprut**
  Intel

- **Yungseon Eo**
  Hanyang University  
- **Hiroo Masuda**
  STARC  
- **Jae-Kyung Wee**
  Soongsil University

**Hideki Asai**
Shizuoka University  
**Arun Chandrasekhar**
Intel (India)  
**Charlie Chung-Ping Chen**
National Taiwan University  
**Eli Chiprut**
Intel

#### [9] Test and Design for Testability

- **Seiji Kajihara**
  Kyushu Institute of Technology  
- **Masaki Hashizume**
  Tokushima University  
- **Sungho Kang**
  Yonsei University

- **XiaoWei Li**
  China Academy of Sciences  
- **Prab Varma**
  Veritable

**Seiji Kajihara**
Kyushu Institute of Technology  
**Masaki Hashizume**
Tokushima University  
**Sungho Kang**
Yonsei University

#### [10] Analog, RF and Mixed Signal Design and CAD

- **Makoto Nagata**
  Kobe University  
- **Seijiro Moriyama**
  PDF Solutions  
- **Hong-June Park**
  POSTECH

- **Jaieet Roychowdhury**
  University of Minnesota  
- **Chau-Chin Su**
  National Chao-Tung University

**Makoto Nagata**
Kobe University  
**Seijiro Moriyama**
PDF Solutions  
**Hong-June Park**
POSTECH

#### [11] Leading Edge Design Methodology for SOCs and SiPs

- **Hideharu Amano**
  Keio University  
- **Jaijeet Roychowdhury**
  University of Minnesota  
- **In-Cheol Park**
  KAIST

- **Borivoje Nikolic**
  University of California, Berkeley  
- **Yulu Yang**
  Nankai University

**Hideharu Amano**
Keio University  
**Jaijeet Roychowdhury**
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**In-Cheol Park**
KAIST
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Hao San
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Makoto Takamiya
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The Hong Kong University of Science and Technology
Tomohisa Wada
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Kunio Uchiyama
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Shigeru Watari
Matsushita Electric Industrial Co., Ltd.
Takeshi Yamamura
FUJITSU LABORATORIES LTD.

JEITA
Yoshitada Fujinami
NEC Electronics Corporation
Shigemi Saito
Sony Corporation
EDA
Hiromitsu Fujii
Nihon Synopsys Co., Ltd.
Fumiyasu Hirose
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Satoshi Kojima
Mentor Graphics Japan Co., Ltd.

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JEITA Representative
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EDSF Chair
Mitsuru Nadaoka
On Electric Industry Co., Ltd.
IEICE TGCAS Chair
Takao Nishitani
Kochi University of Technology
IEICE TGICD Chair
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IPSJ SIG SLDM Chair
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The University of New South Wales
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Tsinghua University, Beijing
Chong-Min Kyung
Korea Advanced Institute of Science and Technology
Youn-Long Steve Lin
Hsing-Hsuan University, Hsin-Chu
Alexander Stempkovsky
Russian Academy of Sciences
The University LSI Design Contest was conceived as a unique program of ASP-DAC Conference. The purpose of the Contest is to encourage education and research in LSI design, and its realization on chips at universities, and other educational organizations by providing opportunities to present and discuss innovative and state-of-the-art designs at the conference. Application areas and types of circuits include (1) Analog and Mixed-Signal Circuits, (2) Digital Signal processing, (3) Microprocessors, and (4) Custom Application Specific Circuits. Methods or technology used for implementation include (a) Full Custom and Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices, including FPGA/PLDs.

This year, nineteen selected designs from seven countries/areas will be disclosed in Session 1D with a short presentations followed by live discussions in front of posters with light meals. Submitted designs were reviewed by the members of the University Design Contest Committee based on the following criteria: Reliability of design and implementation, Quality of implementation, Performance of the design, Novelty, and Additional special features. In the selection process, emphasis was placed more on reliability, quality, and performance. As a result, the nineteen designs were selected. Also, we have instituted one outstanding design award and two special feature awards.

It is with great pleasure that we acknowledge the contributions to the Design Contest, and it is our earnest belief that it will promote and enhance research and education in LSI design in academic organizations. It is also our hope that many people not only in academia but in industry will attend the contest and enjoy the stimulating discussions.

**Date, Time and Locations:**
- **Oral Presentation**: 10:15-12:20, January 25, 2006, Room 416+417
- **Poster Presentation**: 12:20-13:30, January 25, 2006, Room 418 (Food will be served.)

University LSI Design Contest Committee

**Co-Chair**
- Kazutoshi Kobayashi
  - Kyoto University

**Co-Chair**
- Takahiko Arakawa
  - RENESAS Technology Corp.

**Industries’ Forum**

This brandnew event, Designers’ Forum, is conceived as a unique program for ASP-DAC to encourage mutual exchange both between and within designers in industry, researchers in the area of EDAs, and EDA developers. Here, designs will be presented focusing on design styles, design issues, and ways to tackle design issues. Panel discussions will also be held for the latest design issues.

This year, we will have 2 special sessions in ASP-DAC 2006 as follows. 4 presentations related to low power designs, power models, and power estimation frameworks for the real SoC designs will be given by Toshiba, Fujitsu, Hitachi and Renesas, and Samsung in session 5D, “Low Power Design.” In session 8D, “Cell processor”, 4 presentations will be given focusing on simulations, tests, verifications, power estimation, and design methodology of Cell; and PLL design employed in the Cell processor.

In addition to the special sessions, we will have 2 panel discussions. Session 6D, “Functional Verification -now and future-” will be moderated by Dr. Y. Masubuchi of Toshiba, who has been deeply engaged in the architecture design and verifications of the Cell processor. Three panelists are LSI designers, working for functional verifications in LSI design, and one panelist is from an EDA vendor, developing functional verification tools. Session 9D, “Top 10 design issues seen by LSI designers versus EDA developers”, on the other hand, will be moderated by Dr. Y. Hagihara of Sony. Three panelists are managers of SoC and system designs, will focus on the top 10 design issues seen by LSI designers; and 3 panelists are technology officers from 3 major EDA vendors, and they will focus on top 10 design issues seen by EDA developers. Discussions will be led toward the perspectives of the future SoC design issues, comparing with the two top 10 issues seen by both LSI designers and EDA developers.

This Designers’ Forum is planned by the Industry Laison Members of ASP-DAC2006. It is with great pleasure that we acknowledge the contributions to the Designers’ Forum, and it is our earnest belief that this forum will promote mutual exchange of designers and EDA researchers and developers, toward nano-meter SoC design issues.

**Industry Liaison Chair**
- Haruyuki Tago
  - TOSHIBA CORPORATION

**Designers’ Forum Chair**
- Makoto Ikeda
  - University of Tokyo
Keynote Addresses

Keynote Address I
Wednesday, January 25, 9:00-10:00, Small Auditorium, 5F
“Automotive Electronics: Steady Growth for Years to Come!”
Alberto Sangiovanni-Vincentelli
The Edgar L. and Harold H. Buttners Chair of Electrical Engineering and Computer Science, University of California, Berkeley, and Chief Technology Advisor, Member of the Board and Co-founder, Cadence Design Systems, United States

The world of electronics is witnessing a revolution in the way products are conceived, designed and implemented. The ever growing importance of the web, the advent of microprocessors of great computational power, the explosion of wireless communication, the development of new generations of integrated sensors and actuators are changing the world in which we live and work. The new key words are:

- Disappearing electronics, i.e., electronics has to be invisible to the user, it has to help unobtrusively.
- Pervasive computing, i.e., electronics is everywhere, all common use objects will have an electronic dimension.
- Ambient intelligence, i.e., the environment will react to us with the use of electronic components. They will recognize who we are and what we like.
- Wearable computing, i.e., the new devices will be worn as a watch or a hat. They will become part of our clothes. Some of these devices will be tags that will contain all important information about us.
- Know more, carry less, i.e., the environment will know more about us so that we will not need to carry all the paraphernalia of keys, credit cards, personal I.D.s, access cards, access codes.

We would also like to thank SpringSoft Foundation for providing travel grants for students from Taiwan, the Engineering Sciences Society of the Institute of Electronics, Information and Communication Engineers, and ASP-DAC for providing travel grants for other students and sponsoring the event.

Special thanks to Dr. Fumiyasu Hirose, Professor Young-Long Steve Lin, Professor Hidetoshi Onodera, Dr. Atsushi Takahashi, and Professor Hiroto Yasuura for supporting and contributing to the Ph.D. Forum.

Hidetoshi Onodera
General Chair
ASP-DAC 2007

Invitation to ASP-DAC 2007

On behalf of the Organizing Committee, it is my great pleasure and honor to invite all of you to ASP-DAC 2007, which is the 12th event of this conference series. The conference will be held from January 23 to 26, 2007 at Pacifico Yokohama, Japan. The conference site is the same as this year.

Technical Program Chair of this conference is Professor Yusuke Matsunaga from Kyushu University, Japan. Technical Program Vice Chair is Professor Kiyong Choi from Seoul National University, Korea. Under their strong leadership, internationally organized Program Committee will structure ASP-DAC as a high-quality conference that emphasizes original contributions that open up new vistas in the field with significant theoretical and practical impact.

The conference will include a technical program, keynote talks, tutorials, and special sessions highlighting the latest issues and development in IC design technology and automation. I would like to invite you to actively participate in ASP-DAC by submitting cutting edge research results for publication, by proposing interesting topics for tutorials and special sessions, or simply by dropping by in January to enjoy a lively ASP-DAC event.

Ph.D. Forum at ASP-DAC 2006

This year for the second time ASP-DAC is holding a poster session for Ph.D. students to present their research work. The forum provides a great opportunity for students to get feedback and have discussion with people from academia and industry.

Date and Time: 12:20-13:30, January 26, 2006
Location: Room 418 (Food will be served.)

We would like to thank the following persons that evaluated the submissions,

- Ali Azizi-Kusha, Tehran University, Iran
- Supratik Chakraborty, Indian Institute of Technology Bombay, India
- Naehyuk Chang, Seoul National University, South Korea
- Sheqin Dong, Tsinghua University, China
- Toru Ishihara, Kyushu University, Japan
- Philip Leong, Imperial College, England
- Hiroshi Saito, University of Aizu, Japan
- Toshiyuki Shibuya, Fujitsu, Japan
- Omid Shoaei, University of Tehran, Iran
- Makoto Sugihara, Institute of Systems and Information Technologies, Japan

We would also like to thank SpringSoft Foundation for providing travel grants for students from Taiwan, the Engineering Sciences Society of the Institute of Electronics, Information and Communication Engineers, and ASP-DAC for providing travel grants for other students and sponsoring the event.

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Organizer
Farzam Fallah
Fujitsu Labs. of America
The important thing in the next stage is to optimize the design process by investing in computer resources. For example, it is necessary to thoroughly adapt simulation technology to the development of high quality imaging technology, embedded system (hardware/software) technology, or communication technology. The quantitative evaluation from the early design phase and the workflow based on the accumulated design know-how (IP methodology) will accelerate technology innovation and strengthen the platform even further. Eventually, management can directly obtain absolute advantage of large-scale system design effectiveness.

Keynote Address II
Thursday, January 26, 9:00-10:00,
Small Auditorium, 5F
“Challenging Device Innovation”
Satoru Ito
President & CEO
RENESAS Technology Corp., Japan

The semiconductor industry has continuously transformed our way of life, through a number of underlying technology breakthroughs and innovations over the past years. There are currently two challenges that this industry faces: a limitation of miniaturization technology and a difficulty in maintaining an economy of scale. To cope with these challenges, there is a growing need to work closely with partners and customers who have business related to semiconductors, in addition to semiconductor manufacturers. Especially in the area of semiconductor design, we see a need to create a new EDA methodology that broadens the definition of traditional EDA and re-defines the connection among system designers, SoC designers and development tool designers. As we move closer to the realm driven by the convergence of applications and advancements in miniaturization technology, I’d like to discuss the associated technological challenges as well as economical challenges, and present to you our strategy to overcome these issues.

Keynote Address III
Friday, January 27, 9:00-10:00,
Small Auditorium, 5F
“Effective Platform-based Development for Large-scale Systems Design”
Yukichi Niwa
Senior Advisory Director,
Group Executive of Platform Technology Development Headquarters
CANON INC., Japan

Platform-based development (PBD) aims to continuously add new value in both cases of incremental development and product planning based development. By adding new technology to previously existing technology and by storing the technologies as reusable assets, PBD enables high quality, low cost, and short turnaround time development. Furthermore, PBD allows target-oriented development where we can select and concentrate technology to eliminate unnecessary development.

In order to execute effective PBD, it is important to introduce the firm layer structuring of digital/analog technology so that individual professionals in independent layer can maximize their efficiency without any restraint. The act of layer structuring is nothing but the architectural design of the development methodology. Thus, it’s no exaggeration to say that success in business profitability management directly depends on the presence of the good architect.
1A-5 Generation of Shorter Sequences for High Resolution Error Diagnosis Using Sequential SAT
Sung-Jui Pan, Kwang-Ting Cheng (Univ. of California, Santa Barbara, United States), John Moondanos, Ziyad Hanna (Intel Corp., United States)

Wednesday, January 25, 10:15 - 12:20 Room 413
Session 1B: Interconnect for High-End SoC
Chair(s): Yoshihori Takeuchi – Osaka Univ., Japan
Juin-Dar Huang – National Chiao-Tung Univ., Taiwan

1B-1 Constraint-Driven Bus Matrix Synthesis for MP-SoC
Sudeep Pasricha, Nikil Dutt (Univ. of California, Irvine, United States), Mohamed Ben-Romdhane (Conexant, United States)

1B-2 Improving Routing Efficiency for Network-on-Chip through Contention-Aware Input Selection
Dong Wu, Bashir M. Al-Hashimi, Marcus T. Schmitz (Univ. of Southampton, Great Britain)

1B-3 Physical Design Implementation of Segmented Buses to Reduce Communication Energy
Jin Guo, Antonis Papanikos, Pol Marchal, Francky Cattoor (IMEC, Belgium)

1B-4 Co-Synthesis of a Configurable SoC Platform based on a Network on Chip Architecture
Mário Pereira Vésitas, Horácio Neto (INESC-ID, Portugal)

1B-5 Customized SIMD Unit Synthesis for System on Programmable Chip - A Foundation for HW/SW Partitioning with Vectorization
Muhammad Omer Cheema, Omar Hammami (ENSTA Paris, France)

Wednesday, January 25, 10:15 - 12:20 Room 414+415
Session 1C: Timing Analysis and Optimization
Chair(s): Ryuichi Yamaguchi – Matsushita, Japan
Atsushi Kurokawa – STARC, Japan

1C-1 Robust Analytical Gate Delay Modeling for Low Voltage Circuits
Anand Ramalingam (Univ. of Texas, Austin, United States), Sreekumar V. Kodakara (Univ. of Minnesota at Twin Cities, United States), Aniruddh Devgan (Magna, United States), David Z. Pan (Univ. of Texas, Austin, United States)

1C-2 CGTA: Current Gain-based Timing Analysis for Logic Cells
Shahin Nazarian, Massoud Pedram (Univ. of Southern California, United States), Tao Lin, Emre Tuncer (Magma, United States)

1C-3 Efficient Static Timing Analysis Using a Unified Framework for False Paths and Multi-Cycle Paths
Shuo Zhou, Bo Yao, Hongyu Chen, Yi Zhu, Chung-Kuan Cheng (Univ. of California, San Diego, United States), Mike Hutton (Altera Corp., United States)

1C-4 Crosstalk Analysis using Reconvergence Correlation
Sachin Shrivastava, Rajendra Pratap, Harinranath Parameswaran, Manuj Verma (Cadence Design Systems, India)

1C-5 Process-Induced Skew Reduction in Nominal Zero-Skew Clock Trees
Matthew R. Guthaus, Dennis Sylvester (Univ. of Michigan, United States), Richard B. Brown (Univ. of Utah, United States)

Wednesday, January 25, 10:15 - 12:20 Room 416+417
Session 1D: University Design Contest
Chair(s): Kazutoshi Kobayashi – Kyoto Univ., Japan
Takahiko Arakawa – Renesas, Japan

1D-1 A Low Dynamic Power and Low Leakage Power 90-nm CMOS Square-Root Circuit
Tadayoshi Enomoto, Nobuaki Kobayashi (Chuo Univ., Japan)

1D-2 A High-Throughput Low-Power Fully Parallel 1024-bit 1/2-Rate Low Density Parity Check Code Decoder in 3-Dimensional Integrated Circuits
Lili Zhou, Cherry Wakayama, Nottorn Jangkrajnarong, Bo Hu, Richard Shi (Univ. of Washington, United States)

1D-3 A 16-Bit, Low-Power Microsystem with Monolithic MEMS-LC Clocking
Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale (Univ. of Michigan, United States), Richard B. Brown (Univ. of Utah, United States)

1D-4 Ultra-Low Voltage Power Management Circuit and Computation Methodology for Energy Harvesting Applications
Chi-Ying Tsui, Hui Shao, Wing-Hung Ki, Feng Su (Hong Kong Univ. of Science and Tech., Hong Kong)

1D-5 A 0.5-V Sigma-Delta Modulator Using Analog T-Switch Scheme for the Subthreshold Leakage Suppression
Koichi Ishida, Atit Tamtrakarn, Takayasu Sakurai (Univ. of Tokyo, Japan)

1D-6 An Implementation of a CMOS Down-Conversion Mixer for GSM1900 Receiver
Fangqing Chu, Wei Li, Junyan Ren (Fudan Univ., China)

1D-7 Integrated Direct Output Current Suppression Converter using Symmetrically-Matched Self-Biased Current Sensors
Yat-Hei Lam (Hong Kong Univ. of Science and Tech., Hong Kong), Suet-Chui Koon (National Semiconductor Corp., Hong Kong), Wing-Hung Ki, Chi-Ying Tsui (Hong Kong Univ. of Science and Tech., Hong Kong)

1D-8 Adaptively-Biased Capacitor-Less CMOS Low Dropout Regulator with Direct Current Feedback
Yat-Hei Lam, Wing-Hung Ki, Chi-Ying Tsui (Hong Kong Univ. of Science and Tech., Hong Kong)

1D-9 A Built-in Power Supply Noise Probe for Digital LSIs
Mitsuya Fukazawa, Koichiro Noguchi, Makoto Nagata, Kazuo Taki (Kobe Univ., Japan)

1D-10 A 476-gate-count Dynamic Optically Reconfigurable Gate Array VLSI chip in a standard 0.35um CMOS Technology
Minoru Watanabe, Fuminori Kobayashi (Kyushu Inst. of Tech., Japan)

1D-11 Measurement Results of Within-Die Variations on a 90nm LUT Array for Speed and Yield Enhancement of Reconfigurable Devices
Kazuya Katsuki, Manabu Kotani, Kazutoshi Kobayashi, Hidetoshi Onodera (Kyoto Univ., Japan)

1D-12 High-Throughput Decoder for Low-Density Parity-Check Code
Tatsuyuki Ishikawa, Kazunori Shimizu, Takeshi Ikennaga, Satoshi Goto (Waseda Univ., Japan)

1D-13 Hardware Implementation of Super Minimum All Digital FM Demodulator
Nursani Rahmatullah, Arif Nugroho (Institut Teknologi Bandung, Indonesia)
2D-3 Area Optimization for Leakage Reduction and Thermal Stability in Nanometer Scale Technologies
Ja Chun Ku, Yehea Ismail (Northwestern Univ., United States)

2D-4 Compact Thermal Models for Estimation of Temperature-dependent Power/Performance in FinFET Technology
Aditya Bansal, Mesut Meterelliyoz (Purdue Univ., United States), Siddharth Singh (Osmania University, India), Jung Hwan Choi, Jayathi Murthy, Kaushik Roy (Purdue Univ., United States)

Wednesday, January 25, 16:00 - 18:05
Room 413
Session 3B: Future Technical Directions for Design Automation
Chair(s): Makoto Nagata – Kobe Univ., Japan
Ryuichi Fujimoto – Toshiba, Japan

3B-1 Fast Simulation of Large Networks of Nanotechnological and Biochemical Oscillators for Investigating Self-Organization Phenomena
Xiaolue Lai, Jaijeet Roychowdhury (Univ. of Minnesota, United States)

3B-2 Newton: A Library-Based Analytical Synthesis Tool for RF-MEMS Resonators
Michael S. McCorquodale (Mobius Microsystems, Inc., United States), James L. McCann (Carnegie Mellon Univ., United States), Richard B. Brown (Univ. of Utah, United States)

3B-3 Jitter Decomposition in Ring Oscillators
Qingqi Dou, Jacob Abraham (Univ. of Texas, Austin, United States)

3B-4 A Fast Methodology for First-Time-Correct Design of PLLs Using Nonlinear Phase-Domain VCO Macromodels
Prashant Goyal (Indian Inst. of Tech., Kanpur, India), Xiaolue Lai, Jaijeet Roychowdhury (Univ. of Minnesota, United States)

3B-5 Double Edge Triggered Feedback Flip-Flop in Sub 100nm Technology
Seid Hadi Rasouli, Amir Amirabadi, Azam Seyedi, Ali Afzali-Kusha (Univ. of Tehran, Iran)

Wednesday, January 25, 16:00 - 18:05
Room 414+415
Session 3C: Routing and Interconnect Optimization
Chair(s): Youichi Shiraishi – Gunma Univ., Japan
Tong Jing – Tsinghua Univ., China

3C-1 Post-Routing Redundant Via Insertion for Yield/Reliability Improvement
Kuang-Yao Lee, Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

3C-2 Temperature-Aware Routing in 3D ICs
Tianpei Zhang, Yong Zhan, Sachin S. Sapatnekar (Univ. of Minnesota, United States)

3C-3 Closed Form Solution for Optimal Buffer Sizing Using The Weierstrass Elliptic Function
Sebastian Vogel (Darmstadt Univ. of Tech., Germany), Martin D.F. Wong (Univ. of Illinois, Urbana-Champaign, United States)
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<td>4A-3 Delay Variation Tolerance for Domino Circuits</td>
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<td>4A-4 Efficient Identification of Multi-Cycle False Path</td>
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<td>4B-3 An Automated Design Flow for 3D Microarchitecture Evaluation</td>
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<td>4D-3 EDA Vendor Adoption Hillel Ofek (Sagantec, United States)</td>
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<td>4D-4 Utility of the OpenAccess Database in Academic Research David Papa, Igor Markov (Univ. of Michigan, United States), Phillip Chong (Cadence Design Systems, United States)</td>
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5B-4 PRLGRAN: Parallelism Granularity Selection for Scheduling Task Chains on Dynamically Reconfigurable Architectures
Sudarshan Banerjee, Elaheh Bozorgzadeh, Nikil Dutt (Univ. of California, Irvine, United States)

5B-5 Memory Optimal Single Appearance Schedule with Dynamic Loop Count for Synchronous Dataflow Graphs
Hyunok Oh, Nikil Dutt (Univ. of California, Irvine, United States), Soonhoi Ha (Seoul National Univ., Republic of Korea)

5C-1 Wire Sizing with Scattering Effect for Nanoscale Interconnection
Sean X. Shi, David Z. Pan (Univ. of Texas, Austin, United States)

5C-2 Adaptive Admittance-based Conductor Meshing for Interconnect Analysis
Ya-Chi Yang, Cheng-Kok Koh, Venkataraman Balakrishnan (Purdue Univ., United States)

5C-3 Interconnect RL Extraction at a Single Representative Frequency
Akira Tsuchiya (Kyoto Univ., Japan), Masanori Hashimoto (Osaka Univ., Japan), Hitodoshi Onodera (Kyoto Univ., Japan)

5C-4 An Efficient Algorithm for 3-D Reluctance Extraction Considering High Frequency Effect
Mengsheng Zhang, Wenjian Yu (Tsinghua Univ., China), Yu Du (Synopsys Inc., United States), Zeyi Wang (Tsinghua Univ., China)

5C-5 Macromodelling Oscillators Using Krylov-Subspace Methods
Xiaohua Li, Jaijeet Roychowdhury (Univ. of Minnesota, United States)

5D-1 Low-Power Design Methodology for Module-wise Dynamic Voltage and Frequency Scaling with Dynamic De-skewing Systems
Takeshi Kitahara, Hiroki Hara, Shinichi Shiratake (Toshiba, Japan), Yoshiki Tsukiboshi (Toshiba Microelectronics Co., Japan), Tomoyuki Yoda, Tetsuaki Suzuki, Fumihiro Minami (Toshiba, Japan)

Satoshi Imai, Atsuki Inoue, Motoaki Matsumura, Kenichi Kawasaki, Atsushi Suga (Fujitsu Lab., Japan)

5D-3 A System-level Power-estimation Methodology based on IP-level Modeling, Power-level Adjustment, and Power Accumulation
Masafumi Onouchi, Tetsuya Yamada (Hitachi Ltd., Japan), Kimihito Morikawa, Isamu Mochizuki, Hidetoshi Sekine (Renesas, Japan)

5D-4 PowerVIP: SoC Power Estimation Framework at Transaction Level
Ikhwon Lee, Hyunsuk Kim, Peng Yang, Sunjoo Yoo (Samsung Electronics, Republic of Korea), Eui-Young Chung (Yonsei Univ., Republic of Korea), Kyu-Myung Choi, Jeong-Taek Kong, Soo-Kwan Eo (Samsung Electronics, Republic of Korea)
### Session 6A: Analysis and Optimization of Gate Leakage Current of Power Gating Circuits
Hyung-Ock Kim, Youngsoo Shin (KAIST, Republic of Korea)

### Session 6B: Delay Modeling and Static Timing Analysis for MTCMOS Circuits
Naoki Ohkubo, Kimiyoshi Usami (Shibaura Inst. of Tech., Japan)

### Session 6C: Switching Activity Driven Gate Sizing and Vth Assignment for Low Power Design
Yu-Hui Huang, Po-Yuan Chen, TingTing Hwang (National Tsing Hua Univ., Taiwan)

### Session 6D: Power Driven Placement with Layout Aware Supply Voltage Assignment for Voltage Island Generation in Dual-Vdd Designs
Bin Liu, Yici Cai, Qiang Zhou, Xianlong Hong (Tsinghua Univ., China)

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#### Chair(s):
- **Soonhoi Ha** – Seoul National Univ., Republic of Korea
- **Youn-Long Lin** – National Tsing Hua Univ., Taiwan

### Session 6D: Designers’ Forum Panel: Functional Verification -now and future-

**Organizer:** Haruyuki Tago – TOSHIBA, Japan  
**Moderator:** Yoshio Masubuchi – TOSHIBA, Japan  
**Panelists:** Sanjay Gupta – IBM, United States  
- Michael Stellfox – Cadence, United States  
- Tetsuji Sumioka – Sony, Japan  
- Sunao Torii – NEC, Japan
7C-1 Statistical Corner Conditions of Interconnect Delay (Corner LPE Specifications)
Kenta Yamada, Noriaki Oda (NEC Electronics, Japan)

7C-2 Speed Binning Aware Design Methodology to Improve Profit under Parameter Variations
Animesh Datta (Purdue Univ., United States), Swarup Bhunia (Case Western Reserve Univ., United States), Jung Hwan Choi, Saibal Mukhopadhyay, Kaushik Roy (Purdue Univ., United States)

7C-3 Yield-Area Optimizations of Digital Circuits Using Non-dominated Sorting Genetic Algorithm (YOGA)
Vineet Agarwal, Janet Wang (Univ. of Arizona, United States)

7C-4 A Probabilistic Analysis of Pipelined Global Interconnect Under Process Variations
Navneeth Kankani, Vineet Agarwal, Janet M Wang (Univ. of Arizona, United States)

7C-5 Yield-Preferred Via Insertion Based on Novel Geotopological Technology
Fangyi Luo (Univ. of California, Santa Cruz, United States), Yongbo Jia (Nannon Technologies, Inc., United States), Wayne Wei-Ming Dai (Univ. of California, Santa Cruz, United States)

7D-1 Introduction to H.264 Advanced Video Coding
Jian-Wen Chen, Chao-Yang Kao, Yuon-Long Lin (National Tsing Hua Univ., Taiwan)

7D-2 Algorithm and DSP Implementation of H.264/AVC
Hungh-Chih Lin, Yu-Jen Wang, Kai-Ting Cheng, Shang-Yu Yeh, Wei-Nien Chen, Chia-Yang Tsai, Tian-Sheuan Chang, Hsueh-Ming Hang (National Chiao-Tung Univ., Taiwan)

7D-3 Hardware Architecture Design of an H.264/AVC Video Codec
Tung-Chien Chen, Chung-Jr Lin, Liang-Gee Chen (National Taiwan Univ., Taiwan)

7D-4 ASIP Approach for Implementation of H.264/AVC
Sung Dae Kim, Jeong Hoo Lee, Chung Jin Hyun, Myung Hoon Sunwoo (Ajou Univ., Republic of Korea)

7D-5 Panel Discussion
Youn-Lin Long (National Tsing Hua Univ., Taiwan), Hsueh-Ming Hang (National Chiao-Tung Univ., Taiwan), Liang-Gee Chen (National Taiwan Univ., Taiwan), Myung Hoon Sunwoo (Ajou Univ., Republic of Korea)
8B-3 Maximizing Data Reuse for Minimizing Memory Space Requirements and Execution Cycles
Mahmut Kandemir, Guangyu Chen, Feihui Li (Pennsylvania State Univ., United States)

8B-4 Compiler-Guided Data Compression for Reducing Memory Consumption of Embedded Applications
Ozcan Ozturk, Guangyu Chen, Mahmut Kandemir (Pennsylvania State Univ., United States), Ibrahim Kolcu (Univ. of Manchester, Great Britain)

8B-5 Analysis of Scratch-Pad and Data-Cache Performance Using Statistical Methods
Javed Absar (IMEC, Katholieke Universiteit Leuven, Belgium), Franky Catthoor (IMEC, Belgium)

Session 8C: Inductive Issues in Power Grids and Packages

Chair(s): Takashi Sato – Renesas, Japan
Yehsea Ismail – Northwestern Univ., United States

8C-1 Efficient Early Stage Resonance Estimation Techniques for C4 Package
Jin Shi, Yici Cai (Tsinghua Univ., China), Shelton X-D Tan (Univ. of California, Riverside, United States), Xianlong Hong (Tsinghua Univ., China)

8C-2 Parallel-Distributed Time-Domain Circuit Simulation of Power Distribution Networks with Frequency-Dependent Parameters
Takayuki Watanabe (Univ. of Shizuoka, Japan), Yuichi Tanji (Kagawa Univ., Japan), Hidemasa Kubota, Hideki Asai (Shizuoka Univ., Japan)

8C-3 Power Distribution Techniques for Dual VDD Circuits
 Sarvesh Hemchandra Kulkarni, Dennis Sylvester (Univ. of Michigan, United States)

8C-4 Calculating Frequency-Dependent Inductance of VLSI Interconnect by Complete Multiple Reciprocity Boundary Element Method
Changhao Yan, Wenjian Yu, Zeyi Wang (Tsinghua Univ., China)

8C-5 Controlling Inductive Cross-talk and Power in Off-chip Buses using CODECs
Brock LaMeres (Agilent Technologies Inc., United States), Kanupriya Gulati, Sunil Khatri (Texas A&M Univ., United States)
9A-2 An Automated, Efficient and Static Bit-width Optimization Methodology Towards Maximum Bit-width-to-Error Tradeoff With Affine Arithmetic Model
Yu Pu, Yajun Ha (National Univ. of Singapore, Singapore)

9A-3 Abridged Addressing: A Low Power Memory Addressing Strategy
Preeti Ranjan Panda (Indian Inst. of Tech., Delhi, India)

9A-4 Using Speculative Computation and Parallelizing Techniques to Improve Scheduling of Control based Designs
Roberto Cordone (Univ. degli studi di Crema, Italy), Fabrizio Ferrandi, Gianluca Palermo, Marco Domenico Santambrogio, Donatella Sciuto (Politecnico di Milano, Italy)

9A-5 Worst Case Execution Time Analysis for Synthesized Hardware
Jun-hee Yoo, Xingguang Feng, Kiyoung Choi (Seoul National Univ., Republic of Korea), Eui-Young Chung, Kyu-Myung Choi (Samsung Electronics, Republic of Korea)

9B-4 Reducing Dynamic Compilation Overhead by Overlapping Compilation and Execution
Priya Unnikrishnan (IBM Toronto, Canada), Mahmut Kandemir, Fei-hui Li (Pennsylvania State Univ., United States)

9B-5 Functional Modeling Techniques for Efficient Sw Code Generation of Video Codec Application
Sang-Il Han (TIMA Laboratory, France), Soo-Ik Chae (Seoul National Univ., Republic of Korea), Ahmed Amine Jerjaya (TIMA Laboratory, France)

Friday, January 27, 16:00 - 18:05 Room 413
Session 9B: Modeling, Compilation and Optimization of Embedded Architectures
Chair(s): Hiroyuki Tomiyama – Nagoya Univ., Japan
Lovic Gauthier – FLEETS, Japan

9B-1 Workload Prediction and Dynamic Voltage Scaling for MPEG Decoding
Ying Tan, Parth Malani, Qinru Qiu, Qing Wu (State Univ. of New York, Binghamton, United States)

9B-2 Lazy BTB: Reduce BTB Energy Consumption Using Dynamic Profiling
Yen-Jen Chang (National Chung-Hsing Univ., Taiwan)

9B-3 Cache Size Selection for Performance, Energy and Reliability of Time-Constrained Systems
Yuan Cai (Univ. of Iowa, United States), Marcus T. Schmitz, Alireza Ejafari, Bashir M. Al-Hashimi (Univ. of Southampton, Great Britain), Sudhakar M. Reddy (Univ. of Iowa, United States)

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With the advance of the VLSI technology, interconnect and packaging are becoming dominant factors in deciding system performance and power consumption. The scalability of interconnect and packaging is recognized as a principal challenge in ITRS Roadmap. This tutorial will provide an overview of new and emerging packaging and interconnect technologies and how they will impact silicon performance. A detailed discussion of the critical factors in the packaging and interconnect design that influence chip performance will be included. The tutorial will provide a comprehensive list of simple, often overlooked design methods to get the most out of many today's most promising new packaging technologies.

**Tutorial 3 (HALF DAY)**
Tuesday, January 24, 9:30-12:30 Room 414+415
Low Power / Low Leakage Technologies for Nanometer Era: System and Architecture Level Approaches

Organizer: Kiyoharu Hamaguchi – Osaka Univ., Japan
Speakers: Kiyoharu Hamaguchi – Osaka Univ., Japan
Erich Marschner – Cadence Design Systems, Inc., United States

Energy-efficient design is strongly required in SoCs for portable applications. Even for high-end microprocessors, power dissipation becomes a critical hurdle when increasing the performance. This tutorial discusses technical challenges and approaches for low-power / low-leakage design at system and architecture levels. Topics include: dynamic voltage and frequency scaling (DVFS), queue resizing, pipeline balancing and scaling, cache and memory optimizations, globally asynchronous locally synchronous (GALS) architecture, trade-offs between power and reliability, etc.

**Tutorial 4 (HALF DAY)**
Tuesday, January 24, 14:00-17:00 Room 414+415
Low Power / Low Leakage Technologies for Nanometer Era: Circuit and Device Level Approaches

Organizer: Kimiyoshi Usami – Shibaura Institute of Technology, Japan
Speakers: Kimiyoshi Usami – Shibaura Institute of Technology, Japan
Tohru Mogami – NEC Corporation, Japan

Power dissipation is one of the most critical issues in nanometer devices. In addition to dynamic power, leakage power becomes a major concern. This tutorial discusses technical challenges and approaches for low-power / low-leakage design at circuit and device levels. Topics include: circuit and CAD techniques for power gating (MTCMOS), physical implementation and CAD techniques for multi-voltage design, high-k gate dielectric stacks, Cu/low-k interconnects, 3-D device structures, new materials such as SiGe, etc.

**Tutorial 5 (HALF DAY)**
Tuesday, January 24, 9:30-12:30 Room 416+417
Basics and Practice of Current Functional Verification Methods

Organizer: Kiyoharu Hamaguchi – Osaka Univ., Japan
Speakers: Kiyoharu Hamaguchi – Osaka Univ., Japan
Lei He – Univ. of California, Los Angeles, United States

This tutorial 1) summarizes basic concepts and currently available techniques in modern functional verification, 2) presents, in particular, practice of assertion-based verification, and 3) overviews advanced topics in formal verification methods.

This part overviews currently available techniques in functional verification, which includes functional coverage, assertion, constrained random simulation and bounded/unbounded model checking. Rather than underlying algorithms of the techniques, we mainly dis-
cuss what can be done with the techniques from a point of designers’ view.

Part 2. Practice of Assertion-Based Verification (Marschner).
This part presents various techniques for utilizing assertions and functional coverage monitors to achieve higher quality verification in less time. This includes guidelines for writing assertions and coverage monitors, recommendations for where to apply them, and how to leverage them most effectively in typical verification flows.

Part 3. Advanced Topics in Formal Functional Verification (Hamaguchi).
The last part introduces emerging techniques for functional validation or verification, which will be used in functional verification in near-future. This includes abstraction-refinement techniques for large-scale verification, and also formal verification techniques for high-level languages such as SpecC or UML.

Tutorial 6 (HALF DAY)
Tuesday, January 24, 14:00-17:00 Room 416+417
SoC Communication Architectures: Current Practice, Research and Trends

Organizer: Nikil Dutt – Univ. of California, Irvine, United States
Speakers: Nikil Dutt – Univ. of California, Irvine, United States
Sudeep Pasricha – Univ. of California, Irvine, United States

The increasing complexity of Systems-on-Chip (SoCs) has led to the critical “design productivity gap” problem. Several strategies are being employed to cope with this problem, including an IP-based design flow, as well as platform-based designs for application domains. These approaches have critically increased the amount of on-chip communication. Since on-chip communication architectures have a significant impact on system performance, power dissipation and time-to-market, system designers, as well as the research community have focused on the issue of exploring, evaluating, and designing SoC communication architectures to meet the targeted design goals. This tutorial will focus on the current design practices, research efforts and emerging trends in the area of on-chip communication architectures. In the first part of the tutorial, we will first motivate the need for a communication architecture-centric design flow for SoC designs. We will then present a survey of the communication architectures currently used in industry and discuss commonly used protocols and standards such as OCP-IP, VSIA, AMBA, CoreConnect, STBus and Sonics. This will be followed by a case study of a typical industrial design methodology that incorporates communication architecture design in their flow. In the second part of the tutorial, we will present a survey of research efforts in the area of communication architecture exploration, synthesis and implementation, with the goal of improving system performance, reducing power dissipation, cost and design cycle time. The focus of this part will be on variants of bus based and bus-matrix based communication architectures. In the final part of the tutorial, we will outline emerging trends in the area of on-chip communication architectures design and review research efforts on the topics of network-on-chips and on-chip optical interconnects.
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| 10:15 | **1A (Room 411+412)**:  
Formal Methods for Coverage and Scalable Verification | **1B (Room 413)**:  
Interconnect for High-End SoC | **1C (Room 414+415)**:  
Timing Analysis and Optimization | **1D (Room 416+417)**:  
University Design Contest |
| 12:20 | **Lunch Break / University Design Contest Discussion at ASP-DAC Site (Room 418)** | | **Coffee Break (Room 418)** | |
| 13:30 | **2A (Room 411+412)**:  
Software Techniques for Efficient SoC Design | **2B (Room 413)**:  
Application Examples with Leading Edge Design Methodology | **2C (Room 414+415)**:  
Placement | **2D (Room 416+417)**:  
Special Session: Electrothermal Design of Nanoscale Integrated Circuits |
| 15:35 | **Coffee Break (Room 418)** | | **Coffee Break (Room 418)** | |
| 16:00 | **3A (Room 411+412)**:  
Logic Synthesis | **3B (Room 413)**:  
Future Technical Directions for Design Automation | **3C (Room 414+415)**:  
Routing and Interconnect Optimization | **3D (Room 416+417)**:  
Special Session: Flash Memory in Embedded Systems |
| 18:05 |                  |                                        |                                        |                                        |

**Wednesday, January 25**

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| 10:15 | **4A (Room 411+412)**:  
Resolving Timing Issues: Design and Test | **4B (Room 413)**:  
Leading Edge Design Methodology for SoCs and SiPs | **4C (Room 414+415)**:  
Advanced Circuit Simulation | **4D (Room 416+417)**:  
Special Session: Open Access Overview |
| 12:20 | **Lunch Break / Ph.D. Forum (Room 418)** | | **Coffee Break (Room 418)** | |
| 13:30 | **5A (Room 411+412)**:  
Advances in Simulation Technologies | **5B (Room 413)**:  
Scheduling for Embedded Systems | **5C (Room 414+415)**:  
High Frequency Interconnect Effects in Nanometer Technology | **5D (Small Auditorium, 5F)**:  
13:30-15:30  
Designers’ Forum: Low Power Design |
| 15:35 | **Coffee Break (Room 418)** | | **Coffee Break (Room 418)** | |
| 16:00 | **6A (Room 411+412)**:  
Power Optimization of Large-Scale Circuits | **6B (Room 413)**:  
Advanced Memory and Processor Architectures for MPSoC | **6C (Room 414+415)**:  
New Routing Techniques | **6D (Small Auditorium, 5F)**:  
16:30-18:00  
Designers’ Forum Panel: Functional Verification —now and future— |
| 18:05 |                  |                                        |                                        | **Banquet 18:30–20:30 (Room 501+502)** |

**Thursday, January 26**

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| 10:15 | **7A (Room 411+412)**:  
Minimization of Test Cost and Power | **7B (Room 413)**:  
Substrate Coupling and Analog Synthesis | **7C (Room 414+415)**:  
Statistical and Yield Analysis | **7D (Room 416+417)**:  
Special Session: H.264/AVC Design Challenges and Solutions |
| 12:20 | **Lunch Break** | | **Coffee Break (Room 418)** | |
| 13:30 | **8A (Room 411+412)**:  
Floorplanning | **8B (Room 413)**:  
Memory Optimization for Embedded Systems | **8C (Room 414+415)**:  
Inductive Issues in Power Grids and Packages | **8D (Small Auditorium, 5F)**:  
13:30-15:30  
Designers’ Forum: "Cell" Processor |
| 15:35 | **Coffee Break (Room 418)** | | **Coffee Break (Room 418)** | |
| 16:00 | **9A (Room 411+412)**:  
High-Level Synthesis | **9B (Room 413)**:  
Modeling, Compilation and Optimization of Embedded Architectures | **9C (Room 414+415)**:  
Statistical Design | **9D (Small Auditorium, 5F)**:  
16:30-18:00  
Designers’ Forum Panel: Top 10 Design Issues by LSI Designers versus EDA Developers |
| 18:05 |                  |                                        |                                        |                                        |
**Registration**

Conference pre-registration through Web is strongly advised. Please visit the Online Registration page: (http://www.aspdac.com). If web-based registration is not convenient, pre-registration is possible by filling in and returning the enclosed registration form together with the appropriate fee to the conference secretariat. Registration will be confirmed only upon receipt of the registration fee.

### PAYMENT

All registration fees must be paid in Japanese yen by bank remittance or credit card. Please note that personal checks and bank drafts will not be accepted.

**Bank Remittance**

Please remit the appropriate amount to the following bank account.

Name of Bank: SUMITOMO MITSUI BANKING CORPORATION (The Mitsui Sumitomo Bank) Marunouchi Branch

SWIFT Code: SMBCJPJT

Account Title: ASP-DAC2006 Fumiyasu Hirose

Account No.: 6620287 (Ordinary)

**Credit Card**

The following credit cards will be accepted:

- VISA, MasterCard, American Express

### CANCELLATION AND REFUND

When written notification of cancellation is received by the conference secretariat by December 16, 2005, 5,000 yen will be deducted from the fees paid to cover administrative costs. No refunds will be made for cancellation requests received after this date.

**REGISTRATION HOURS**

- **Tuesday, January 24:** 7:30 – 18:00
- **Wednesday, January 25:** 7:00 – 17:00
- **Thursday January 26:** 7:30 – 17:00
- **Friday January 27:** 7:30 – 17:00

### FEES

<table>
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<tr>
<th>Category</th>
<th>By Dec. 16, ’05</th>
<th>After Dec. 17, ’05 and on site</th>
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<tr>
<td><strong>Conference</strong></td>
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<td><em>Member</em></td>
<td>45,000 yen</td>
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<td>Full-time Student</td>
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<tr>
<td><strong>[Tutorial] (Full-Day or two Half-Days)</strong></td>
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* Member of IEEE, ACM SIGDA, IEICE, IPSJ

The conference fee includes:

- Admission to all sessions (including keynote speeches and designers’ forum) without tutorial
- Banquet (excluding Full-time students)
- One refreshment per break
- Congress kit (with a final program, one copy of conference proceedings, and one CDROM of conference proceedings)

The designers’ forum fee includes:

- Admission to Keynote Speech and Designers’ Forum
- One CDROM of conference proceedings
- One refreshment per break

The tutorial fee includes:

- Admission to full-day or half-day tutorial(s)
- One copy of all tutorial texts
- One lunch coupon
- One refreshment per break

### Advance Registration Deadline: Dec. 16th, 2005

Web-based registration is recommended. Please visit the Online Registration page (http://www.aspdac.com). If web-based registration is not convenient, please complete this form and make a copy, and send it by post mail or fax it to:

**ASP-DAC 2006 SECRETARIAT**

Japan Electronics Show Association

Sumitomo Shibaidaimon Bldg. 2-gokan, 5F
1-12-16, Shibaidaimon, Minato-ku, Tokyo, 105-0012 JAPAN

Tel: +81-3-5402-7601 Fax: +81-3-5402-7605

E-mail: aspdac2006@aspdac.com

**ASP-DAC 2006 Registration Form**

Registra: ( ) Prof. ( ) Dr. ( ) Mr. ( ) Ms. (Please choose one.)

Family name: ___________________________ First name: ___________________________

Other name: ___________________________

Affiliation: ___________________________

Mailstop: ___________________________

Dept./Div.: ___________________________

Mailing address: ___________________________ City: ___________________________

State: ___________________________ Zip: ___________ Country: ___________________________

Phone: ___________________________ Fax: ___________________________

E-mail: ___________________________

Membership: ___________________________

( ) I E I C E ( ) IPSJ ( ) ACM SIGDA ( ) IEEE ( ) Non-member

Member code: ___________________________

**Tutorial:** (Please choose one Full-Day topic or one/two Half-Day topics. If you choose two Half-Day topics, please choose Morning tutorial (Tutorial 3 or 4) and Afternoon tutorial (Tutorial 5 or 6)).

- ( ) Tutorial 1 (Full-Day): DFM Tools and Methodologies for 65nm and Below
- ( ) Tutorial 2 (Full-Day): High Performance Interconnect and Packaging
- ( ) Tutorial 3 (Half-Day): Low Power/Low Leakage Technologies for Nanometer Era: System and Architecture Level Approaches
- ( ) Tutorial 4 (Half-Day): Low Power/Low Leakage Technologies for Nanometer Era: Circuit and Device Level Approaches
- ( ) Tutorial 5 (Half-Day): Basics and Practice of Current Functional Verification Methods
- ( ) Tutorial 6 (Half-Day): SoC Communication Architectures: Current Practice, Research and Trends
Registration Fee & Payment Method

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Grand Total: _________ yen

Invoices and Receipts

Invoice Required? ( ) Yes ( ) No
If you replied “Yes,” and you would like the invoice to be sent to a different address from that of your registration, please input the address below.

Address: ________________________________

Receipt Required? ( ) Yes ( ) No
If you replied “Yes,” and you would like the receipt to be sent to a different address from that of your registration, please input the address below.

Address: ________________________________

Marketing/Sales Management Student Other

Attendee Survey

1) Which category best describes your work?
   ( ) System or LSI Design
   ( ) Research and Development of EDA Tools
   ( ) Design methodology
   ( ) Researcher/Educator in an academic institution
   ( ) Marketing/Sales ( ) Management
   ( ) Student ( ) Other

2) Which area do you primarily work in?
   ( ) System-level Design ( ) Embedded Systems
   ( ) Logic/Behavioral Synthesis ( ) Verification and Test
   ( ) Physical Design ( ) Timing, Power, and Signal Integrity
   ( ) Interconnect, Device, and Circuit Modeling, DFM
   ( ) Analog, RF, Mixed Signal ( ) Emerging Technologies
   ( ) System-level Integration, SIP ( ) Other

3) What is your primary motivation/interest for attending ASP-DAC? (pick all that apply)
   ( ) I am presenting at the conference
   ( ) I want to learn about EDA in general
   ( ) I want to learn more about the basics of EDA
   ( ) I want to learn more about advances in theory
   ( ) I want to learn more about practical application of EDA
   ( ) I have interest in keynote speakers
   ( ) I have interest in specific technical presentation(s)
   ( ) I have interest in Special Sessions and Designers’ Forum
   ( ) I have interest in the technical program as a whole
   ( ) I have interest in networking and social interaction opportunities
   ( ) Other

4) How did you learn about ASP-DAC? (choose the two most significant factors)
   ( ) ASP-DAC web site ( ) Advance Program Brochure
   ( ) E-mail ( ) Previous Attendance
   ( ) Colleague/Advisor
   ( ) I have paper presentation at the conference
   ( ) Other

Registration (3/4)

Registration (4/4)

Note:
1. All payments must be in Japanese yen.
2. Bank drafts and personal checks will not be accepted.
3. If paying by credit card, please visit the Online Registration page (http://www.aspdac.com) or send this form by post mail.
4. The remitter’s name should be the same as the registrant’s name.
5. If paying by bank transfer using your company’s name, please advise us of the ID#, registrant’s name, and transfer date (the day you transfer the fee) by e-mail to aspdac2006@aspdac.com or by Fax at +81-3-5402-7605. If you don’t advise us above information within a week after you transfer the fee, we can’t confirm your payment.
6. Handling fees and other bank transfer fees are to be borne by the registrant.
7. If payment of the registration fee is unremitted, or the credit card charge cannot be authorized, please go to the accounting desk.
8. If registered contents are changed or added, please notify the ASP-DAC 2006 Secretariat by e-mail at aspdac2006@aspdac.com or by Fax at +81-3-5402-7605. (Please be sure to specify your ID#.)
Information

Proceedings:
ASP-DAC 2006 will be producing two versions of the ASP-DAC 2006 Proceedings: a bound paper version and a CD-ROM version. All papers will be included in both versions. Conference registration in any of the categories will include copies of both versions of the ASP-DAC 2006 Proceedings. Additional Proceedings will be available for purchase at the Conference. Prices are as follows:
- **Paper Form:** ¥5,000; **CD-ROM Form:** ¥2,000;
- Both versions of the proceedings will also be available for purchase after the conference; please contact IEEE for the bound version and ACM SIGDA for the CD-ROM version.

Banquet:
Conference registrants are invited to attend a banquet to be held on January 26, 2006. The banquet will be held from 18:30 to 20:30 at the fifth floor of conference center. Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students, Designers’ Forum-only registrants, and Tutorial-only registrants wishing to attend the banquet will be required to pay ¥5,000 for a ticket when they register on site.

Visa Application:
Without a legal visa, foreign participants may be denied entry into Japan. Please contact your nearest Japanese embassy in order to ensure entry. Notice that the ASP-DAC 2006 Organizing Committee issues the invitation letters and supports the VISA applications only for presenters of the conference papers. All the other attendees have to apply for VISA through their travel agents or by yourself. In some cases it may take two months to obtain a legal visa. The following Web page of Japanese embassy may be helpful.
http://www.mofa.go.jp/j/info/visit/visa/index.html

Customs:
Japanese customs are fairly lenient and allow bringing in items necessary for personal use. Duty-free imports are: 3 bottles of liquor; 400 cigarettes or 100 cigars; 2 ounces of perfume; gifts and souvenirs other than the above whose total market value does not exceed 200,000 yen. Strictly prohibited are firearms, other types of weapons and narcotics.

Insurance:
The organizer cannot accept responsibility for accidents which might occur. Delegates are encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home country prior to departure.

Climate:
The temperature in Yokohama during the period of the Conference ranges between 5°C and 12°C.

Currency Exchange:
Only Japanese Yen is accepted at ordinary stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can exchange your currency for Japanese Yen at foreign exchange banks and other authorized money exchange offices with your passport.

Electrical Appliances:
Electrical appliances are supplied on 100 volts in Japan. The frequency is 50 Hz in eastern Japan including Tokyo, Yokohama and 60 Hz in western Japan including Kyoto and Osaka.

Shopping:
The business hours of most department stores are from 10:00 to 20:00. They are open on Sundays and national holidays, but may close on some weekday. Business hours of retail shops differ from one another, but most shops operate from 10:00 to 20:00. Shops are open on Sundays and national holidays.

Sightseeing:
- Participants can get sightseeing information at the Nippon Express Co., Ltd. Travel desk in the Conference site during the Conference period.

Yokohama Bay Sightseeing Cruise
You can ride a cruise boat at Yamashita Park sightseeing Boat Terminal, Minato Mirai Pukanisanbashi Pier (MM21), etc. For more information, reference the home page at: [http://www.welcome.city.yokohama.jp/eng/tourism/walking/1070.html](http://www.welcome.city.yokohama.jp/eng/tourism/walking/1070.html)

CHINA TOWN
Being the largest Chinese settlement in Japan, Chinatown is always alive with people who come to enjoy Chinese food. It is also a fun place for shopping or just walking around its many streets and alleys lined with colorful restaurants, shops overflowing with Chinese goods and stores that sell exotic ingredients and Chinese medicines.

LANDMARK TOWER
296 meters high with 70 stories above ground and three levels underground. It is Japan’s tallest skyscraper. A 40-second ride on the world’s fastest elevator skylights you to the 69th floor’s Sky Garden, the highest observatory in Japan.

Hours: 10:00-21:00 Admission: ¥1,000
Access: 7 min. walk from Sakuragicho station

SANKEIEN GARDEN
A purely Japanese-style landscape garden. Accenting the main garden is an impressive three-story pagoda and graceful garden bridges. Inside contains several old houses and farm buildings as well as Important Cultural Properties such as Rinshunkaku Villa and Chosukaku House.

Hours: 9:00-16:00 Admission ¥300 for each garden
Access: From Sakuragicho Sta., take Bus NO.8 or No.125 to Honmoku-Sankeien-mae.

MARINE TOWER
106 meters, the tallest inland lighthouse in the world, with an observatory located 100 meters above ground.

Hours: 10:00-21:00 Admission: ¥700
Access: 15 min. Walk from JR Ishikawacho station

MARITIME MUSEUM
The site of the previous Nippon Maru, the former training ship for Japan’s Maritime Defense Force. The Yokohama Maritime Museum, which specializes in ports and ships, is located next to the Nippon Maru.

Hours: 10:00-17:00 (Closed Monday) Admission: ¥600
Access: 7 min. walk from JR Sakuragicho station

Other Information:

JAPANTOURIST ORGANIZATION
[http://www.jnto.go.jp](http://www.jnto.go.jp)

YOKOHAMA CONVENTION & VISITORS BUREAU

NARITA AIRPORT
[http://www.narita-airport.or.jp/airport_e/index.html](http://www.narita-airport.or.jp/airport_e/index.html)

YES ! TOKYO
## Accommodations

### HOTEL RESERVATION

Nippon Express has reserved blocks of rooms at hotels in Yokohama during the period. Please fill in the Hotel Reservation Form and submit it to Nippon Express by 16th December, 2005. Reservation will be made on a first-come, first-served basis. Please indicate your order of preference in the application form. If your desired hotel is fully booked, Nippon Express will reserve your second choice or a hotel in the same grade. Hotel charge should be paid directly to the hotel at checkout time. Confirmation of hotel reservation will be sent by fax. Hotel reservation will not be honored without this confirmation.

### Cancellation of Hotel Reservation

In the event of cancellation, written notification should be sent to Nippon Express Co., Ltd. The following cancellation fees will be charged to your credit card.

- Up to 9 days before the first night of stay: 2,000 yen
- 8 to 2 days before: 20% of daily room charge (minimum 2,000 yen)
- One day before or after: 100% of daily room charge
- No notice given: 100% of daily room charge

### Hotel Reservation Form

**ASPDAC 2006**

January 24 - 27, 2006, Yokohama Japan

Please complete and return this form to:

Nippon Express Co., Ltd.

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Deadline: Dec. 16, 2005

Note: You should send this form by postal mail or fax when you apply.

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Arrival Schedule:

Arriving at ____________(airport) on ____________(date) by ____________(flight number)
Hotel Reservation (2/2)

Hotel Accommodations:
Please select 2 hotels in order of preference and enter the name of the hotel and the hotel number (see hotel list in this program).

1st choice: ____________________________(No. )
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Room Choice: ( ) Single ( ) Twin

Breakfast: ( ) Yes ( ) No

Period of Stay: Check-in _____ Check-out _____ for ____ nights

Guarantee of Booking:
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Electronic Design and Solution Fair 2006

The Japan Electronics and Information Technology Industries Association (JEITA) will hold the Electronic Design and Solution Fair 2006 on January 26 and 27, 2006, in Pacifico Yokohama. When JEITA was known as the Electronic Industries Association of Japan (EIAJ), we held the EDA TechnoFair for seven consecutive years from 1993 to 2000. This exhibition showcased design solutions, design technologies, and EDA technologies required for the latest electronic systems or semiconductors.

In 2001, the EDA TechnoFair and the FPGA/PLD Design Conference and Exhibit were combined to form the Electronic Design and Solution Fair. The Fair will be held for the sixth time in 2006 as the only exhibition of its kind in Japan.

Today, semiconductors not only play a core supporting role throughout industry and the economy, but they are also an indispensable part of our daily lives. The emergence of computers, the Internet, digital communications, cellular telephones, and digital home appliances would not have been possible without advances in semiconductors. Progress in digital technology, underpinned by innovations in semiconductor technology, is bringing huge changes to society, culture, and lifestyles. In fact, we now stand on the threshold of a ubiquitous age, in which people can communicate anywhere and at any time.

Furthermore, the semiconductor industry will grow even more important as it embraces the challenge of new technological development to supply new products in its quest to remain at the vanguard of the digital networking age.

The theme of Electronic Design and Solution Fair 2006 is "Touch the 65 Nano-World." The Fair will feature a full range of events and exhibitions, which we will be widely publicizing in coming months. In addition to displays and content that meet demand for new solutions, we will open University Plaza to enhance technological interchange between industry, academia and government organizations. The Fair will also feature a special section for the exhibits of overseas emerging companies. Two conferences will be held simultaneously with the Fair: the FPGA/PLD Design Conference and System Design Forum 2006.

JEITA is confident that Electronic Design and Solution Fair 2006 will promote effective and meaningful discussions and interchange between exhibitors and visitors alike, and that it will provide unique opportunities for business development. All of us involved with the Fair look forward to seeing you there.

Tadashi Okamura
Chairman
Japan Electronics and Information Technology Industries Association
System Design Forum 2006 at EDS Fair

Friday, January 27, 10:00–12:00, 13:30-15:30
Annex Hall, Pacifico Yokohama

Registration: On line registration will be available in November, 2005 at http://www.edsfair.com.

System Design Forum 2006 will be held on January 27, 2006 at the Pacifico Yokohama, Kanagawa, Japan, organized by EDA Technical Committee (EDA-TC) of Japan Electronics and Information Technology Industries (JEITA). This year at this Forum two sessions are going to be held, focusing on the system level design language, SystemC and SystemVerilog. Up-date information about standardization of each language, tutorials, and design examples of the state-of-the-art SOC design using SystemC or SystemVerilog will be presented.

Session 1: SystemVerilog Users Forum 2006, 10:00-12:00
Chair: K. Hamaguchi (JEITA SystemVerilog Task Group)
SystemVerilog, successor language of VerilogHDL (IEEE Std-1364), is drawn LSI designer attention as next-generation LSI Design/Verification language. And, SystemVerilog was approved as IEEE Std-1800 in September. In this session, a member of IEEE P1800, SystemVerilog Standardization Working Group, will give an update of standardization and the use status of SystemVerilog. And members of JEITA SystemVerilog Task Group will explain the technical trends about SystemVerilog Assertions. This session also includes presentations about design/verification examples using SystemVerilog.

Session 2: SystemC Users Forum 2006, 13:30-15:30
Chair: T. Hasegawa (JEITA SystemC Task Group)
SystemC, C-based language, is widely used as system-level language. IEEE P1666, SystemC Standardization Working Group, is working on the standardization of SystemC for the final approval by the end of this December. A member of IEEE P1666 will give an update of standardization and the road map of SystemC. And members of JEITA SystemC Task Group will explain the technical trends, new features of SystemC 2.1, and compatibility issues with SystemC 2.0.1. This session also includes presentations about design examples using SystemC.

Note: Most of the presentations at the System Design Forum 2006 will be presented in Japanese.

Related to System Design Forum 2006, two paper sessions and two panel sessions are organized as Designers’ Forum in ASP-DAC 2006:

6D: Thursday, January 26, 16:30-18:00, Small Auditorium, 5F “Designers’ Forum Panel: Functional Verification—now and future—”
9D: Thursday, January 27, 16:30-18:00, Small Auditorium, 5F “Designers’ Forum Panel: Top 10 Design Issues by LSI Designers versus EDA Developers”

For more information, visit the following web site: http://www.edsfair.com.