Programmable
Fully-Integrated GPS
receiver in 0.18 \( \mu \text{m} \) CMOS
with Test Circuits

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Contents

- **GPS receiver RF section**
- GPS RF Blocks
- All of the probable problems
- GPS Design with Test Circuits
- Test Pins, Test Blocks, Test Modes
- The GPS receiver specifications
- Measurement results
- GPS-RF IC
**GPS receiver RF section**

- Low-IF architecture
- Low-power
- On-chip single-ended LNA
- IF poly-phase filter (image-rejection, complex to real conversion)
- IF-Amp VGA + linear IF real filter
- Not sensitive to the filter noise
- Power /area decreased during single filtering
- Low energy at the image frequency

\[ f_{RF} = 1574.42 \text{ MHz} \]
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Common source LNA with inductive degeneration:
  - High voltage gain
  - Low noise figure
  - Sufficient linearity
  - Lg & Ls are bond-wires inductor model

A single-ended LNA has been preferred to a balanced one to:
  - Reduce power consumption and silicon area
  - Substrate noise has been eliminated using deep N-Well

Features:
  - 2.5 dB noise figure at 1.57GHz
  - 18dB voltage gain
  - 250MHz bandwidth
  - S11 better than 12dB at the LNA passband
  - $I_{ss} = 2.5mA$
I & Q mixers

- Single-balanced mixers in comparison with double-balanced mixers
  - Lower input noise
  - Leakage of LO frequency to the output
    - LO frequency is much higher than the IF, the output LO frequency would be eliminated completely
- Mixer load is a simple resistor
- Features:
  - $I_{SS} = 1.26mA$ for each mixer
  - Mixer gain = 16dB
  - LO rejection = -32dB
A second-order poly-phase filter

- Recombine I and Q signal paths.
  - Single real path decreases the power consumption and the chip area
- RC structure with inputs and outputs symmetrically disposed
- Zero power consumption
- High image rejection
- Low sensitivity to mismatching in components
- High linearity
- The average image noise rejection = 20dB.
**Active RC filter**

- High linearity
- High dynamic range
- Variable gain
  - Programmable capacitor and the resistor banks
  - No effect the frequency response and bandwidth
- Filter noise is high, (No effect on the receiver input noise due to the high gain of the LNA, mixer, and IF amplifier chain)

- Filter gain changes from -3dB to 52dB
- A cascade of a band-pass and a low-pass filter is used to implement a fourth-order transfer function
- Filter is centered a 4f0
- Bandwidth = 5MHz (considering process variation, temperature range between -40 to 125 degree, 10% variation on the L and C values)
• Low phase noise fully-integrated quadrature LC VCO
• 4nH square inductors with a Q of 6
• MOS varactors
• Frequency tuning range = 450 MHz (considering process variation, temperature range between –40 to 125 degree, 10% variation on the L and C values).
• Minimum signal output amplitude = 0.2 Vp-p, the mixer conversion gain drops in the smaller amplitude
Frequency Synthesizer

- $f_{LO} = 1536 \times f_0 = 128 \times 12 \times f_0$
- $f_{ref} = 12 \times f_0$
- Divided-by-128 = 7 * Divided-by-2
  - Divide-by-2 block consists of two master slave flipflop implemented by CML logic with resistive loads
- Charge pump sends 0.3mA current pulses to the off-chip loop filter
- Filter BW = 1.4MHz
- Settling Time = 10 uSec
- $I_{SS} = 9.3 \text{ mA}$
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## All of the Probable Problems

<table>
<thead>
<tr>
<th>Defective Block</th>
<th>Problem</th>
<th>Solutions to check the rest of the chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>-Gain value wrong</td>
<td>-High gain: Reduce the input signal Level (m0)</td>
</tr>
<tr>
<td></td>
<td>-Noise Figure is high</td>
<td>Low gain: Increase the input signal Level (m0)</td>
</tr>
<tr>
<td></td>
<td>-Input mismatch!</td>
<td>-Measure the NF at the IF output (m0)</td>
</tr>
<tr>
<td></td>
<td>-Oscillates!!</td>
<td>-Can be compensated by an external matching (m0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-Turn off the LNA input bias current, Increase the input signal level (m0)</td>
</tr>
<tr>
<td>Mixer</td>
<td>-I &amp; Q mismatch!</td>
<td>-Not critical (m0&amp;6&amp;7)</td>
</tr>
<tr>
<td></td>
<td>-Low conversion gain</td>
<td>-Change the mixer bias current (m0&amp;6&amp;7)</td>
</tr>
<tr>
<td>Polyphase</td>
<td>-RC error causes low image rejection</td>
<td>Measure the polyphase frequency response (image rejection &amp; loss) by inputting I &amp; Q signals to the polyphase and measuring its output signal (m4&amp;5)</td>
</tr>
<tr>
<td></td>
<td>-High loss</td>
<td></td>
</tr>
<tr>
<td>Filters</td>
<td>-Oscillation!</td>
<td>Measure the filters frequency response by inputting signal to it and measuring its output signal (m0&amp;4)</td>
</tr>
<tr>
<td></td>
<td>-Frequency response is out of spec, has peaking</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-Low noise rejection, high spurs</td>
<td></td>
</tr>
</tbody>
</table>
## All of the Probable Problems

<table>
<thead>
<tr>
<th>Component</th>
<th>Problem</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantizer</td>
<td>False threshold voltage levels</td>
<td>Use an external quantizer from the IFamp3 output (m0)</td>
</tr>
<tr>
<td>VCO</td>
<td>Output frequency is off</td>
<td>Use external LO signal (m1&amp;7)</td>
</tr>
<tr>
<td></td>
<td>Does not oscillate</td>
<td>Use external LO signal (m1&amp;7)</td>
</tr>
<tr>
<td></td>
<td>Low output amplitude</td>
<td>Increase the VCO bias current (m0&amp;2&amp;6)</td>
</tr>
<tr>
<td>PLL Loop</td>
<td>Does not lock</td>
<td>Check divider, VCO, PFD separately (m2&amp;6)</td>
</tr>
<tr>
<td>Divider</td>
<td>Does not work</td>
<td>Use external Lo signal, check the divider output (m6)</td>
</tr>
<tr>
<td>PFD</td>
<td>Does not work</td>
<td>Use of the PFD input signal, check the charge pump output (m5)</td>
</tr>
<tr>
<td>Charge pump</td>
<td>Bias current changed</td>
<td>Compensate it by changing the loop filter element values (m5)</td>
</tr>
</tbody>
</table>
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- *GPS Design with Test Circuits*
- Test Pins, Test Blocks, Test Modes
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- Measurement results
- GPS-RF IC
1) Normal.
2) VCO OFF.
3) BEI&BEQ OFF / DoSen OFF / PFDF OFF.
4) DPQ&DPI ON / Mixer & IFamp1 OFF / OMI&OMQ OFF.
5) DoSen OFF / IFamp2 OFF / FiltF ON.
6) DoSen OFF / Divider OFF / PFDF ON / DPI&DPQ ON / IFamp1 OFF / FiltF OFF / IFamp2 OFF.
7) IFamp1 OFF / OMI&OMQ ON / BEI&BEQ OFF.
8) BEI&BEQ ON / VCO OFF / OMI&OMQ ON / IFamp1 ON.
Test circuits for testing blocks
Contents

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Test Pins

- 6 input bias current test pins to control the main circuit blocks. Bias current for LNA, Mixer, IFAmps, Filter OpAmps, VCO, Dividers are programmable
- 2 External input LO pins
- 4 input pins for I & Q IF signals
- 2 output pins to check the mixers output
- 2 input/output pins to check polyphase outputs or IF input signal for the filter
- 2 output pins to check IFAmp3 output
- 2 input/output pins to check the divider output or 12 MHz input signal for PFD
Test Blocks

• **Input drivers for the test modes:**
  DPI & DPQ (4 MHz quadrature inputs), FiltF (4 MHz filter input), PFDF (12 MHz PFD inputs).

• **Output drivers for the test modes:**
  OMI & OMQ (4 MHz Mixer outputs), PoSen (4 MHz Polyphase outputs), DoSen (12 MHz Divider-by-128 outputs).

• **LO drivers:**
  BEI & BEQ (1.57 GHz Mixer LOs)
Test Modes

1: 000  Normal
2: 001  Ext. VCO
3: 010  VCO Test
4: 011  IF Test
5: 100  RC Filter
6: 101  PFD Test / IFamp2
7: 110  Mixer / VCO Test
8: 111  Mixer / Ext. VCO
Mode 1, Normal

- Normal mode of GPS receiver
- All test circuit blocks is off
• Fault detecting blocks:
  – VCO, Divider
Mode 3, VCO Test

- Fault detecting blocks:
  - VCO
• Fault detecting blocks:
  – IFamp2, Quantizer
Fault detecting blocks:
- RC Filter, Quantizer
Mode 6, PFD Test/ IFamp2

- Fault detecting blocks:
  - PFD, Charge Pump, IFamp2, Quantizer
• Fault detecting blocks:
  – VCO, LNA, Mixers
Mode 8, Mixer/ Ext. LO

• Fault detecting blocks:
  - LNA, Mixers, Divider
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# The GPS receiver specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.8 volt</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18 um, CMOS</td>
</tr>
<tr>
<td>Architecture</td>
<td>Low IF</td>
</tr>
<tr>
<td>Input RF Frequency</td>
<td>1575.42 MHz, GPS L1</td>
</tr>
<tr>
<td>LO Frequency</td>
<td>1571.328 MHz</td>
</tr>
<tr>
<td>Input Matching</td>
<td>&lt;-12dB ( 50Ω )</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>3 dB</td>
</tr>
<tr>
<td>Total Voltage Gain</td>
<td>120 dB</td>
</tr>
<tr>
<td>VGA Range</td>
<td>55 dB</td>
</tr>
<tr>
<td>Image Rejection</td>
<td>-20 dB</td>
</tr>
<tr>
<td>Output Format</td>
<td>1, 1.5 and 2 bit (FSample=4f0 MHz)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>19.5 mA at 1.8 volt</td>
</tr>
<tr>
<td>Chip Area</td>
<td>6.61 mm²</td>
</tr>
</tbody>
</table>
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## Current Consumption

<table>
<thead>
<tr>
<th>Section name</th>
<th>Block name</th>
<th>Current Consumption (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF section</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LNA</td>
<td>5.086</td>
</tr>
<tr>
<td></td>
<td>Mixer</td>
<td>2.504</td>
</tr>
<tr>
<td>IF section</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IF</td>
<td>6.252</td>
</tr>
<tr>
<td></td>
<td>Digital section</td>
<td>5.929</td>
</tr>
<tr>
<td>Synthesizer</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCO</td>
<td>0.323</td>
</tr>
<tr>
<td></td>
<td>Synth-HF section</td>
<td>6.711</td>
</tr>
<tr>
<td></td>
<td>Synth-LF section</td>
<td>2.096</td>
</tr>
<tr>
<td></td>
<td>1.339</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.276</td>
<td></td>
</tr>
<tr>
<td>Bias</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>BG-Bias</td>
<td>1.041</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>19.09</td>
</tr>
</tbody>
</table>
IF filter frequency response and variable gain range
1-bit quantizer output

2-bit quantizer output
Synthesizer Lock Range

VCO Frequency vs. Reference Frequency
Close loop

Reference freq (MHz) | VCO freq (GHz)
---------------------|--------------
21.00                | 1.344        
24.55                | 1.571        
27.00                | 1.728
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Marble-IC2 Pinout

GND_LNA2 1
GND_LNA1 2
IN_RF 3
GND_BG 4
ILNAcont 5
IMIXcont 6
IRCFcont 7
IIFA12cont 8
VCC_BG 9
OMIXn 10
OMIXp 11
IFTNp_I 12
IFTNp_Q 13
IFTNq_Q 14
RCFTOp 15
RCFTOn 16
VCC_IF 17
GND_IF 18
IFA3Op 19
IFA3On 20
CLOCK 21
DATA 22
IBIAST 23
24
30 DivPFDn
31 DivPFDp
32 GND_HF
33 EXT_IDiv
34 EXT_IVCO
35 GND_LF
36 Frefn
37

43 EXT_LOp
44 EXT_LOn
45 VCC_Mix
46 GND_Mix
47 GND_MixI
48 VCC_LNA

50 DATA
51 IBIAST
52 IFTA3Op
53 IFTA3On
54 EXT_LOn
55 EXT_LOp
56 GND_MixQ
57 VCC_Mix
58 GND_MixQ
59 VCC_Mix
60 GND_MixI
61 VCC_LNA
62 GND_LFA
63 IN_RF
64 GND_LNA2
65 IGA12cont
66 IMIXcont
67 IRCFcont
68 VCC_BG
69 GND_BG
70 GND_LNA1
71 GND_LNA2
72 IN_RF
73 GND_BG
74 ILNAcont
75 IMIXcont
76 IRCFcont
77 IIFA12cont
78 VCC_BG
79 OMIXn
80 OMIXp
81 IFTNp_I
82 IFTNp_Q
83 IFTNq_Q
84 RCFTOp
85 RCFTOn
86 VCC_IF
87 GND_IF
88 IFA3Op
89 IFA3On
90 CLOCK
91 DATA
92 IBIAST
93 24
94 23
95 22
96 21
97 20
98 19
99 18
100 17
101 16
102 15
103 14
104 13
105 12
106 11
107 10
108 9
109 8
110 7
111 6
112 5
113 4
114 3
115 2
116 1
117 36
118 35
119 34
120 33
121 32
122 31
123 30
124 29
125 28
126 27
127 26
128 25
129 24
130 23
131 22
132 21
133 20
134 19
135 18
136 17
137 16
138 15
139 14
140 13
141 12
142 11
143 10
144 9
145 8
146 7
147 6
148 5
149 4
150 3
151 2
152 1

Marble-IC2
Die Size : 2573.200 * 2571.015 (μm*μm) = 6.61 mm²
Die Photograph

- LNA Mixer
- Synthesizer
- IF Path: Amp/IMR filter/Ch select filter/Quantizer
Marble-IC2 Package

Package type for the GPS-RF chip is TQFP-48 pin.
Thank You...