Programmable Fully-Integrated GPS receiver in 0.18 μ m CMOS with Test Circuits
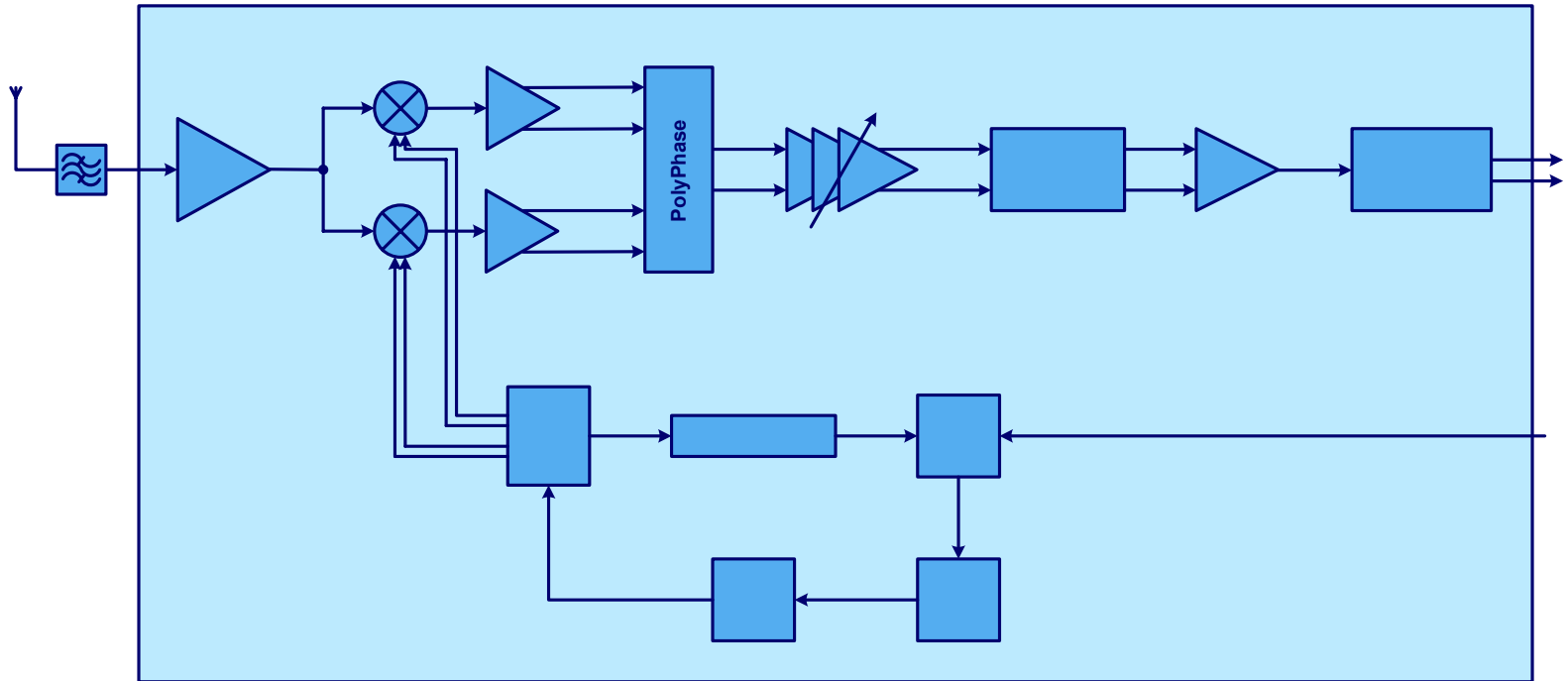
24 Janaury 2007

M. Jenabi, N. Riahi, A. Fotowat

Contents

- *GPS receiver RF section*
- GPS RF Blocks
- All of the probable problems
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GPS receiver RF section

- •Low-IF architecture
- •Low-power
- •On-chip single-ended LNA
- •IF poly-phase filter (image-rejection, complex to real conversion)

- •IF-Amp VGA + linear IF real filter
- •Not sensitive to the filter noise
- •Power /area decreased during single filtering
- •Low energy at the image frequency

f_{RF}=1574.42 MHz

M

LNA

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LNA

•Common source LNA with inductive degeneration:
   •High voltage gain
   •Low noise figure
   •Sufficient linearity
   •Lg & Ls are bond-wires inductor model
•A single-ended LNA has been preferred to a balanced one to:
   •Reduce power consumption and silicon area
   •Substrate noise has been eliminated using deep N-Well
•Features:
   •2.5 dB noise figure at 1.57GHz
   •18dB voltage gain
   •250MHz bandwidth
   •S11 better than 12dB at the LNA passband
   •I_{ss}= 2.5mA
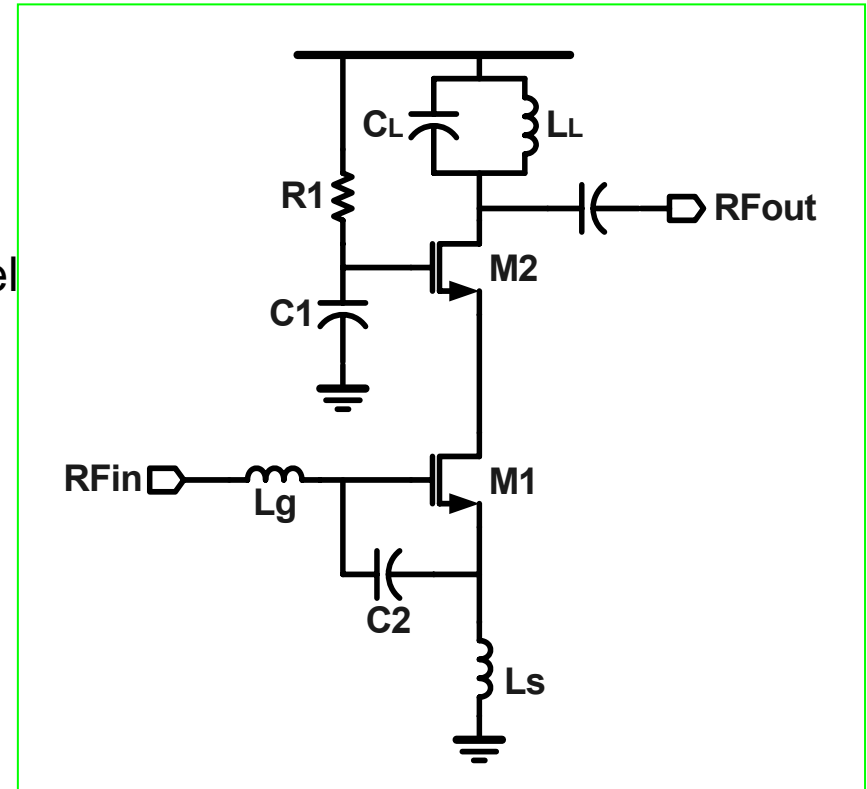
I & Q mixers

- Single-balanced mixers in comparison with double-balanced mixers
    - Lower input noise
    - Leakage of LO frequency to the output
        - LO frequency is much higher than the IF, the output LO frequency would be eliminated completely
- Mixer load is a simple resistor
- Features:
    - I_{SS}= 1.26mA for each mixer
   - Mixer gain = 16dB
    - LO rejection = -32dB
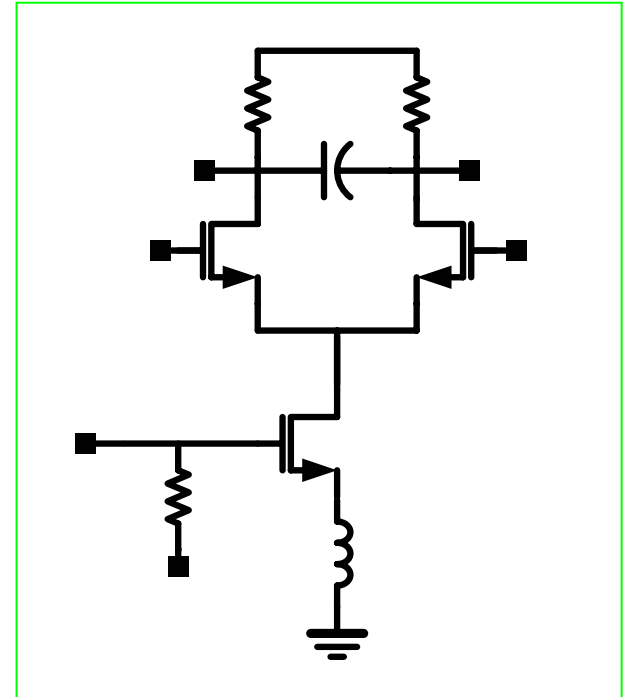
A second-order poly-phase filter
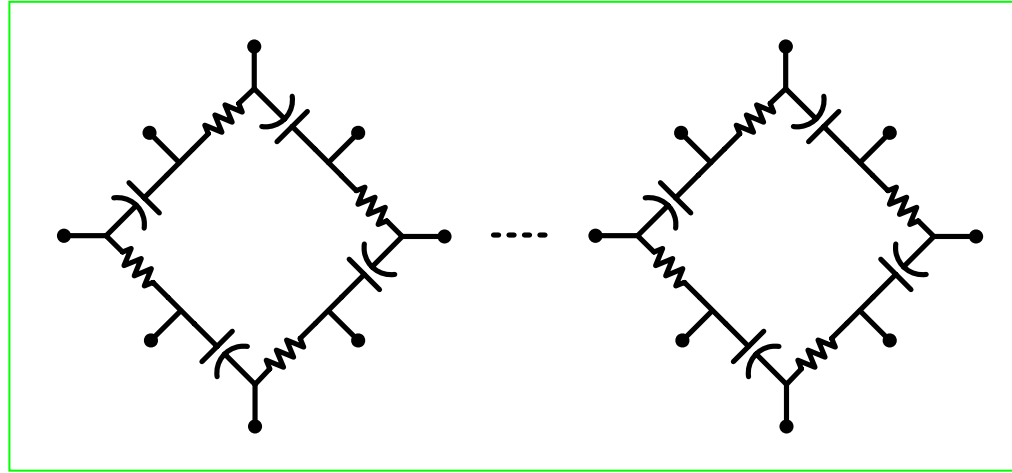
- Recombine I and Q signal paths.
  - Single real path decreases the power consumption and the chip area
- RC structure with inputs and outputs symmetrically disposed
- Zero power consumption
- High image rejection
- Low sensitivity to mismatching in components
- High linearity
- The average image noise rejection = 20dB.

Active RC filter


Band Pass   Low Pass
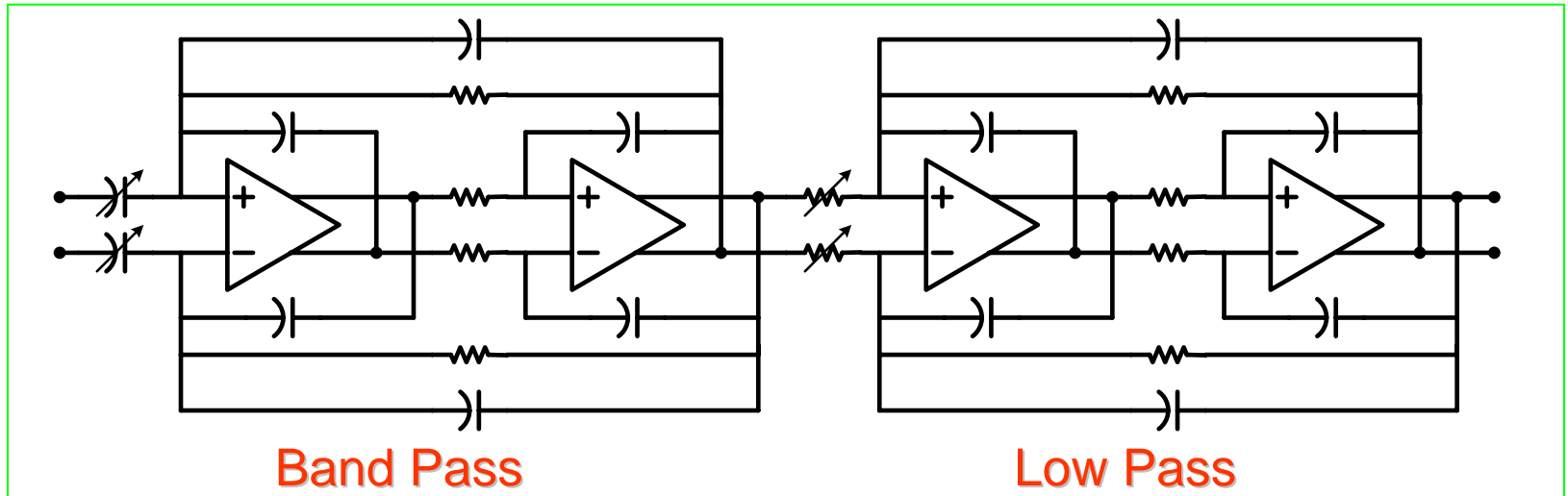
- High linearity
- High dynamic range
- Variable gain
  - Programmable capacitor and the resistor banks
  - No effect the frequency response and bandwidth
- Filter noise is high, (No effect on the receiver input noise due to the high gain of the LNA, mixer, and IF amplifier chain)

- Filter gain changes from -3dB to 52dB
- A cascade of a band-pass and a low-pass filter is used to implement a fourth-order transfer function
- Filter is centered a 4f0
- Bandwidth = 5MHz (considering process variation, temperature range between –40 to 125 degree, 10% variation on the L and C values)

Cin

INp

A quadrature LC VCO
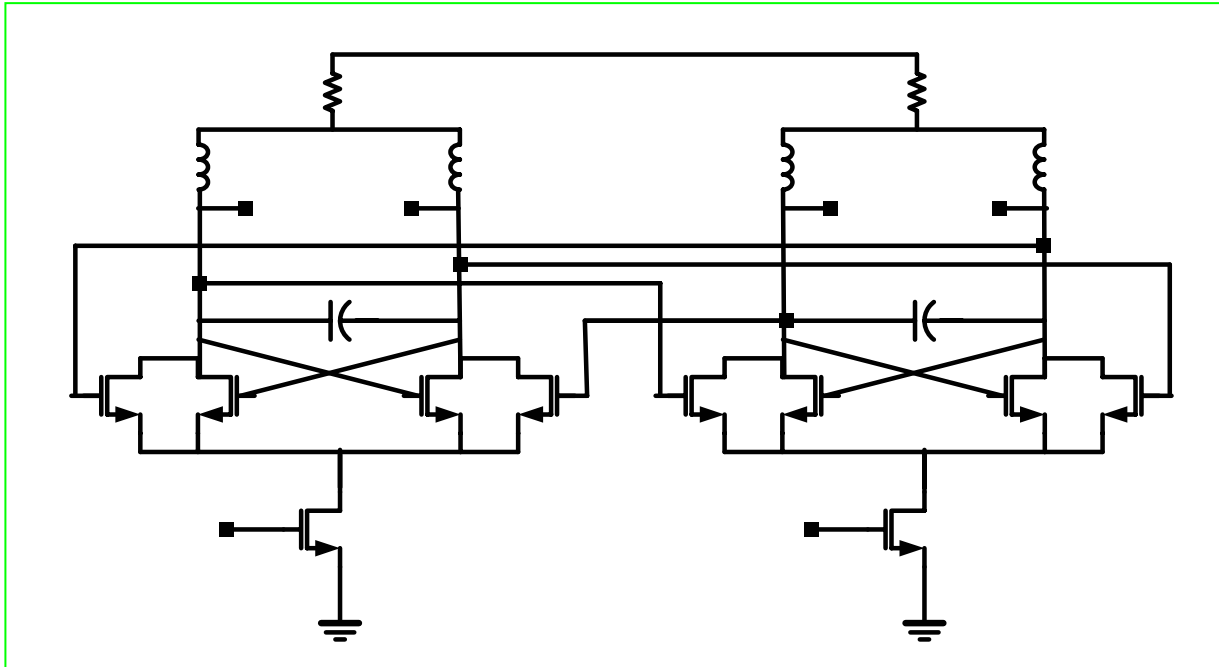
- Low phase noise fully-integrated quadrature LC VCO
- 4nH square inductors with a Q of 6
- MOS varactors
- Frequency tuning range = 450 MHz (considering process variation, temperature range between –40 to 125 degree, 10% variation on the L and C values).
- Minimum signal output amplitude = 0.2 Vp-p, the mixer conversion gain drops in the smaller amplitude

Frequency Synthesizer
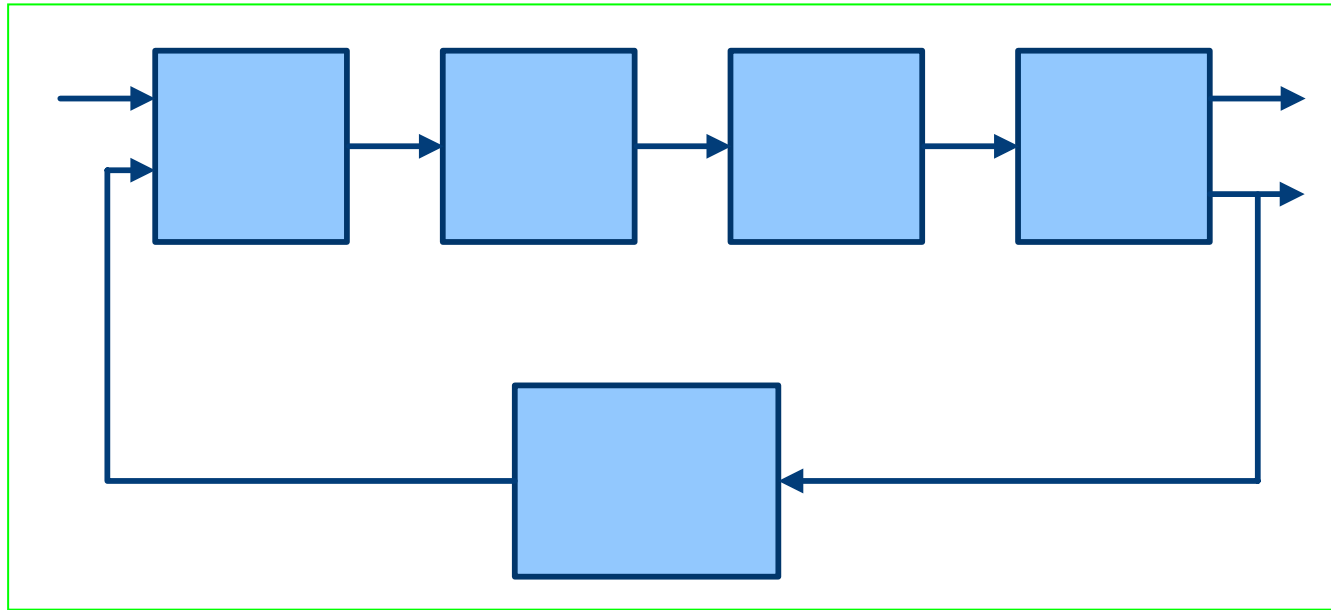
- f_{LO} = 1536 f0 = 128 * 12 f0
- f_{ref} = 12 f0
- Divided-by-128=7*Divided-by-2
    - Divide-by-2 block consists of two master slave flipflop implemented by CML logic with resistive loads
- Charge pump sends 0.3mA current pulses to the off-chip loop filter
- Filter BW=1.4MHz
- Settling Time=10 uSec
- I_{SS} = 9.3 mA

Fref

Frequ

/Ph

Dete

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All of the Probable Problems

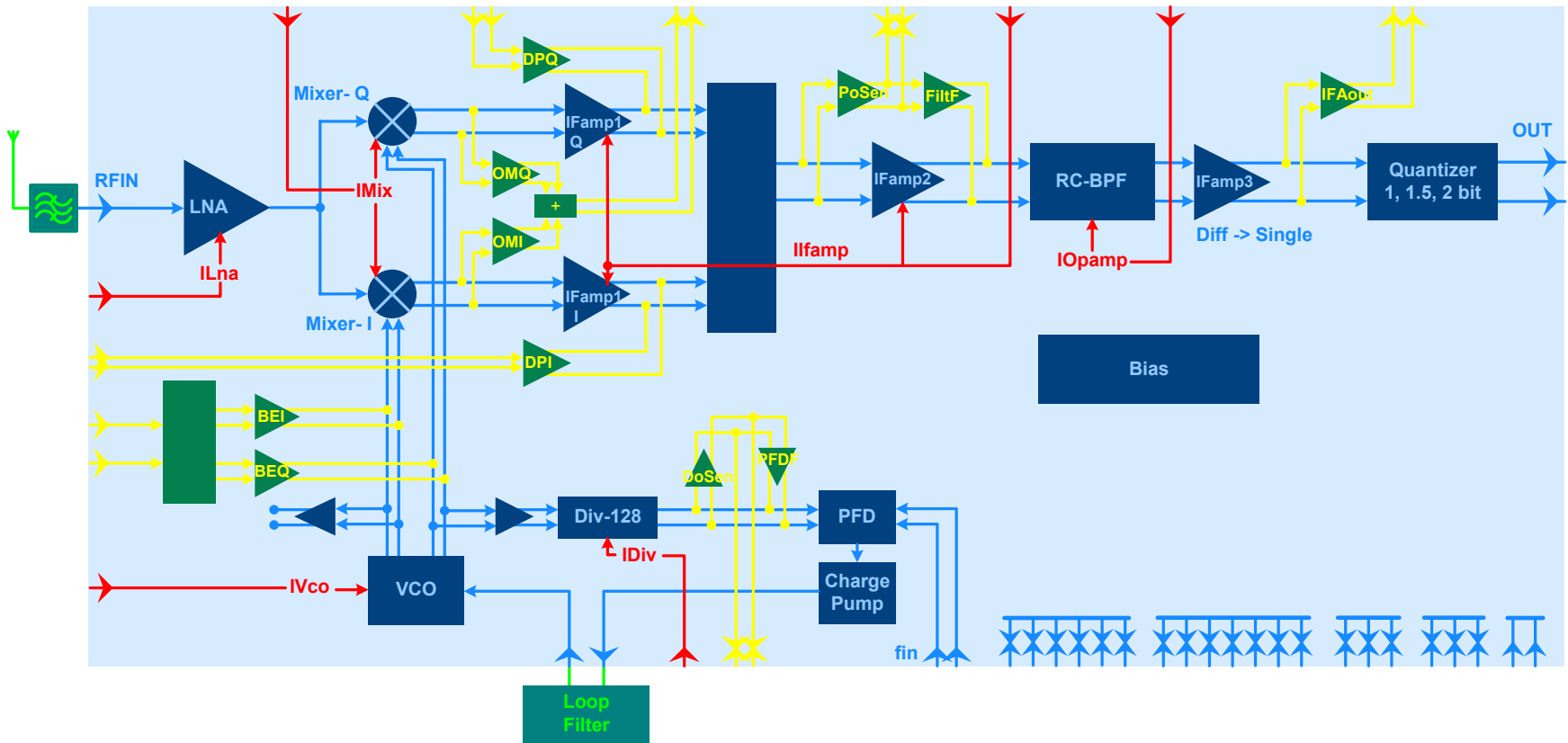| Defective Block	Problem	Solutions to check the rest of the chip
LNA	-Gain value wrong -Noise Figure is high -Input mismatch! -Oscillates!!!	-High gain: Reduce the input signal Level (m0) Low gain: Increase the input signal Level (m0) -Measure the NF at the IF output (m0) -Can be compensated by an external matching (m0) -Turn off the LNA input bias current, Increase the input signal level (m0)
Mixer	-I & Q mismatch! -Low conversion gain	-Not critical (m0&6&7) -Change the mixer bias current (m0&6&7)
Polyphase	-RC error causes low image rejection -High loss	Measure the polyphase frequency response (image rejection & loss) by inputting I & Q signals to the polyphase and measuring its output signal (m4&5)
Filters	-Oscillation! -Frequency response is out of spec, has peaking -Low noise rejection, high spurs	Measure the filters frequency response by inputting signal to it and measuring its output signal (m0&4)

All of the Probable Problems

Quantizer	-False threshold voltage levels	-Use an external quantizer from the IFamp3 output (m0)
VCO	-Output frequency is off -Does not oscillate -Low output amplitude	-Use external LO signal (m1&7) -Use external LO signal (m1&7) -Increase the VCO bias current (m0&2&6)
PLL Loop	-Does not lock	-Check divider, VCO, PFD separately (m2&6)
Divider	-Does not work	-Use external Lo signal, check the divider output (m6)
PFD	-Does not work	-Use of the PFD input signal, check the charge pump output (m5)
Charge pump	-Bias current changed	-Compensate it by changing the loop filter element values (m5)

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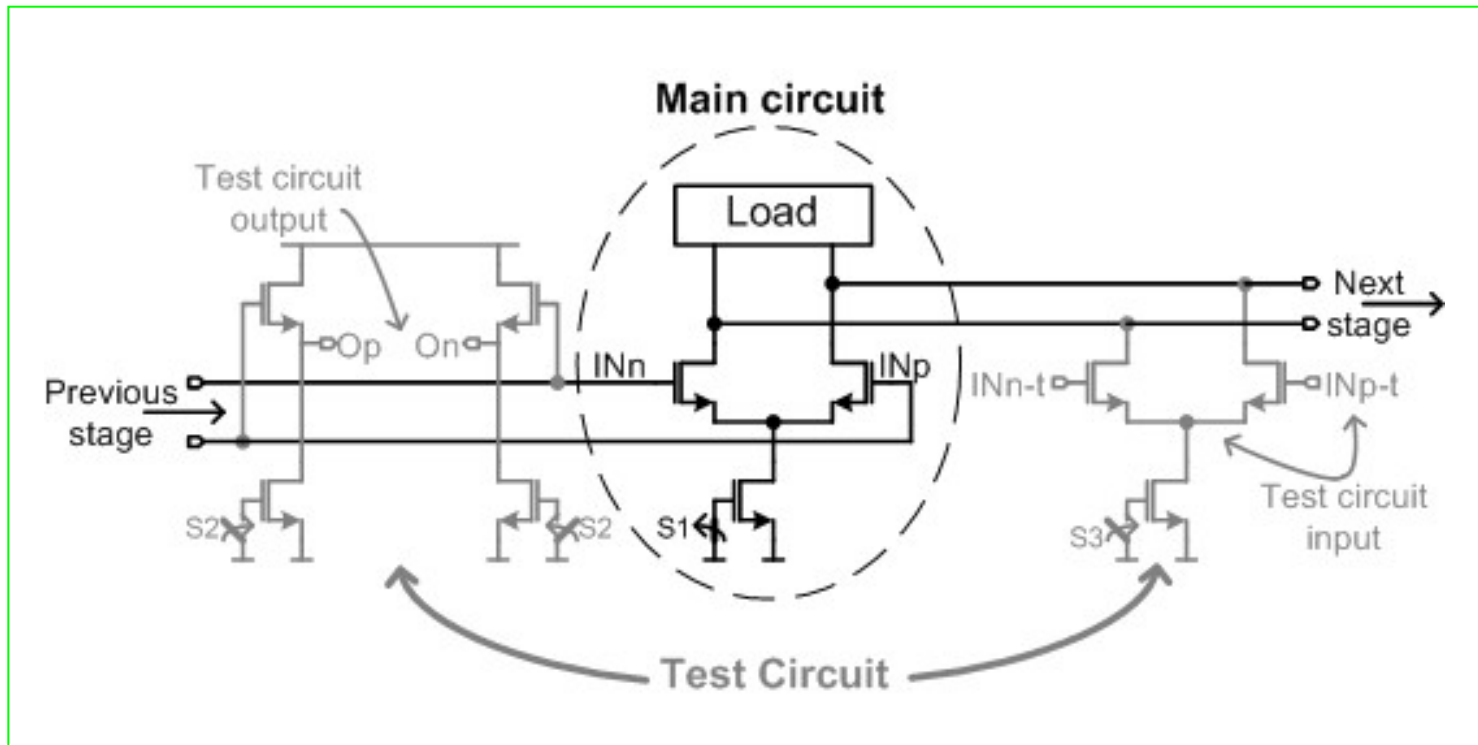- Measurement results
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GPS Design with Test Circuits

1:	000	Normal	1) Normal.
2:	001	Ext. VCO	2) VCO OFF.
3:	010	VCO Test	3) BEI&BEQ OFF / DoSen OFF / PFDF OFF.
4:	011	IF Test	4) DPQ&DPI ON / Mixer & IFamp1 OFF / OMI&OMQ OFF.
5:	100	RC Filter	5) DoSen OFF / IFamp2 OFF / FiltF ON.
6:	101	PFD Test / IFamp2	6) DoSen OFF / Divider OFF / PFDF ON / DPI&DPQ ON / IFamp1 OFF / FiltF OFF / IFamp2 OFF.
7:	110	Mixer / VCO Test	7) IFamp1 OFF / OMI&OMQ ON / BEI&BEQ OFF.
8:	111	Mixer / Ext. VCO	8) BEI&BEQ ON / VCO OFF / OMI&OMQ ON / IFamp1 ON.

Test circuits for testing blocks

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Test Pins

- **6 input bias current test pins to control the main circuit blocks. Bias current for LNA, Mixer, IFAmps, Filter OpAmps, VCO, Dividers are programmable**

- **2 External input LO pins**

- **4 input pins for I & Q IF signals**

- **2 output pins to check the mixers output**

- **2 input/output pins to check polyphase outputs or IF input signal for the filter**

- **2 output pins to check IFAmp3 output**

- **2 input/output pins to check the divider output or 12 MHz input signal for PFD**

Test Blocks

- **Input drivers for the test modes:**

  DPI & DPQ (4 MHz quadrature inputs), FiltF (4 MHz filter input), PFDF (12 MHz PFD inputs).

- **Output drivers for the test modes:**

  OMI & OMQ (4 MHz Mixer outputs), PoSen (4 MHz Polyphase outputs), DoSen (12 MHz Divider-by-128 outputs).

- **LO drivers:**

  BEI & BEQ (1.57 GHz Mixer LOs)

Test Modes

1: 000 Normal
2: 001 Ext. VCO
3: 010 VCO Test
4: 011 IF Test
5: 100 RC Filter
6: 101 PFD Test / IFamp2
7: 110 Mixer / VCO Test
8: 111 Mixer / Ext. VCO

Mode 1, Normal
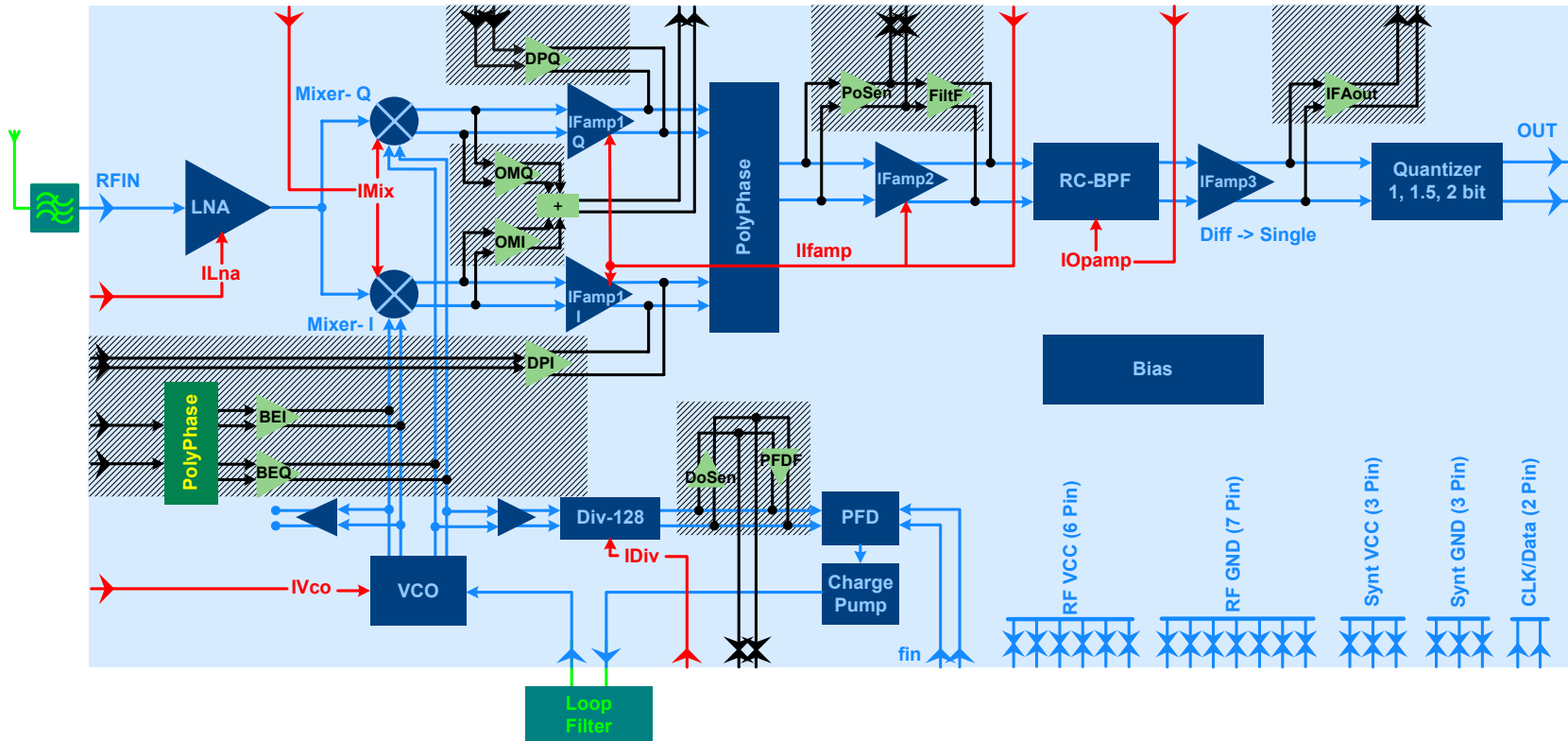
- Normal mode of GPS receiver
- All test circuit blocks is off

Mode 2, Ext. LO
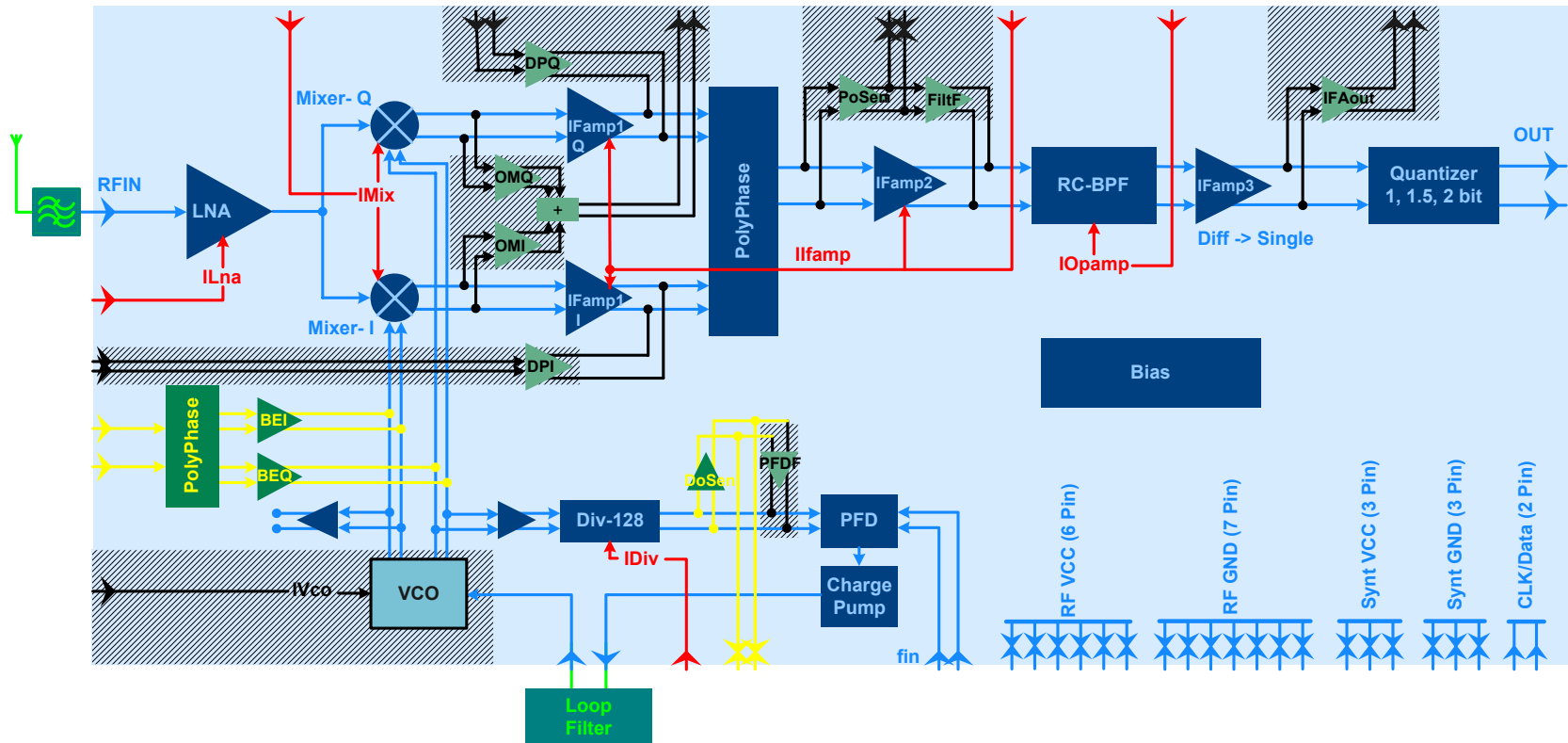
- Fault detecting blocks:
  - VCO, Divider

Mode 3, VCO Test
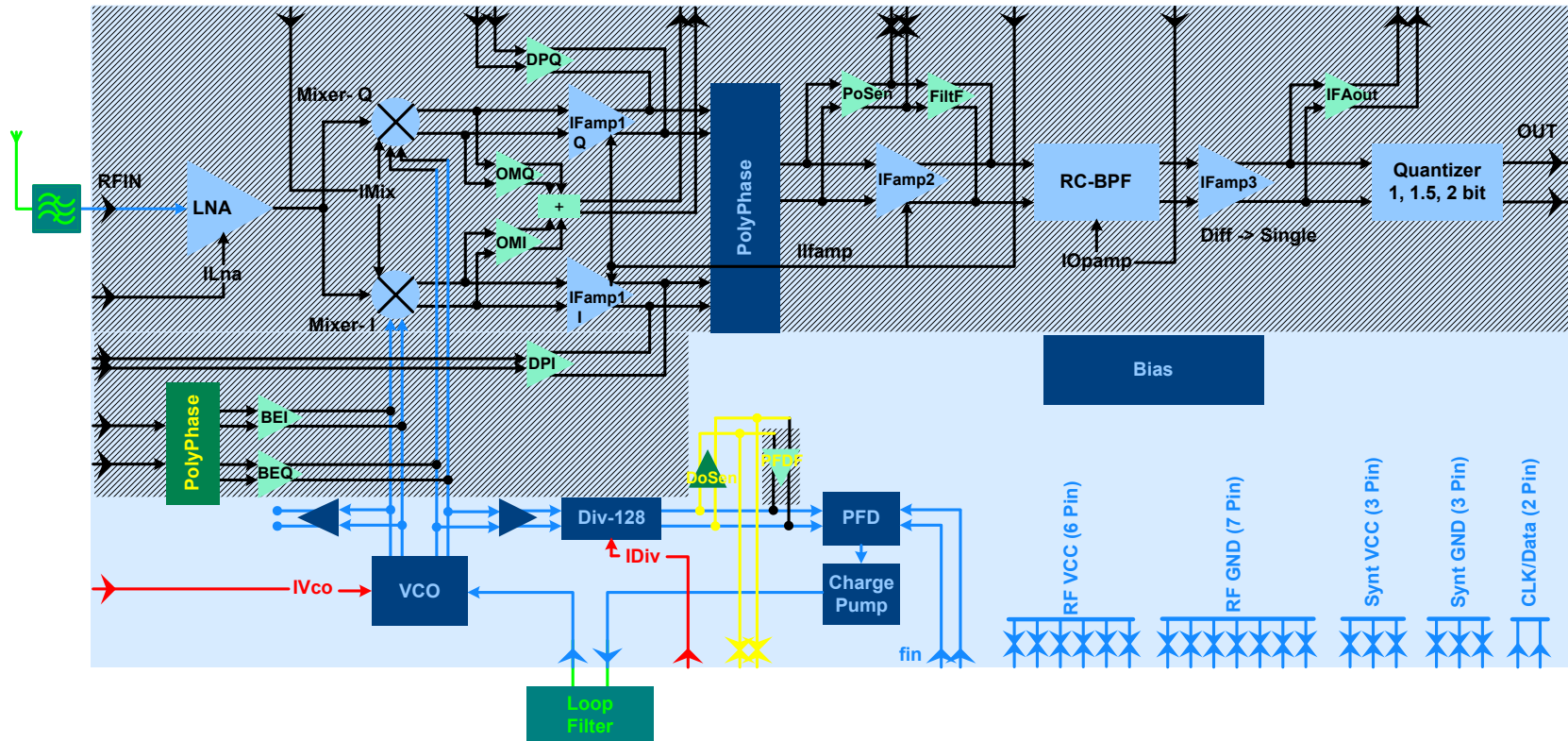
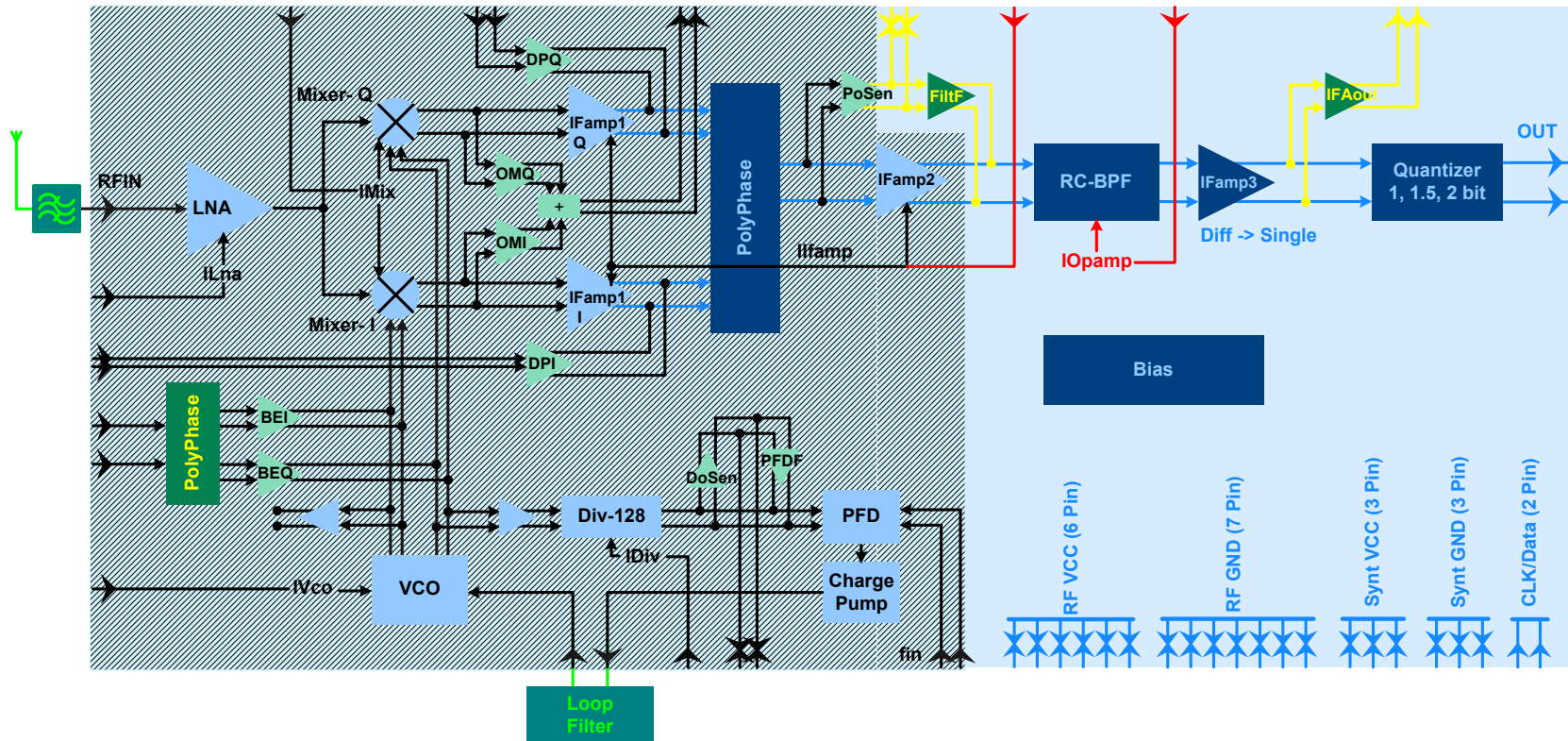
- Fault detecting blocks:
  - VCO

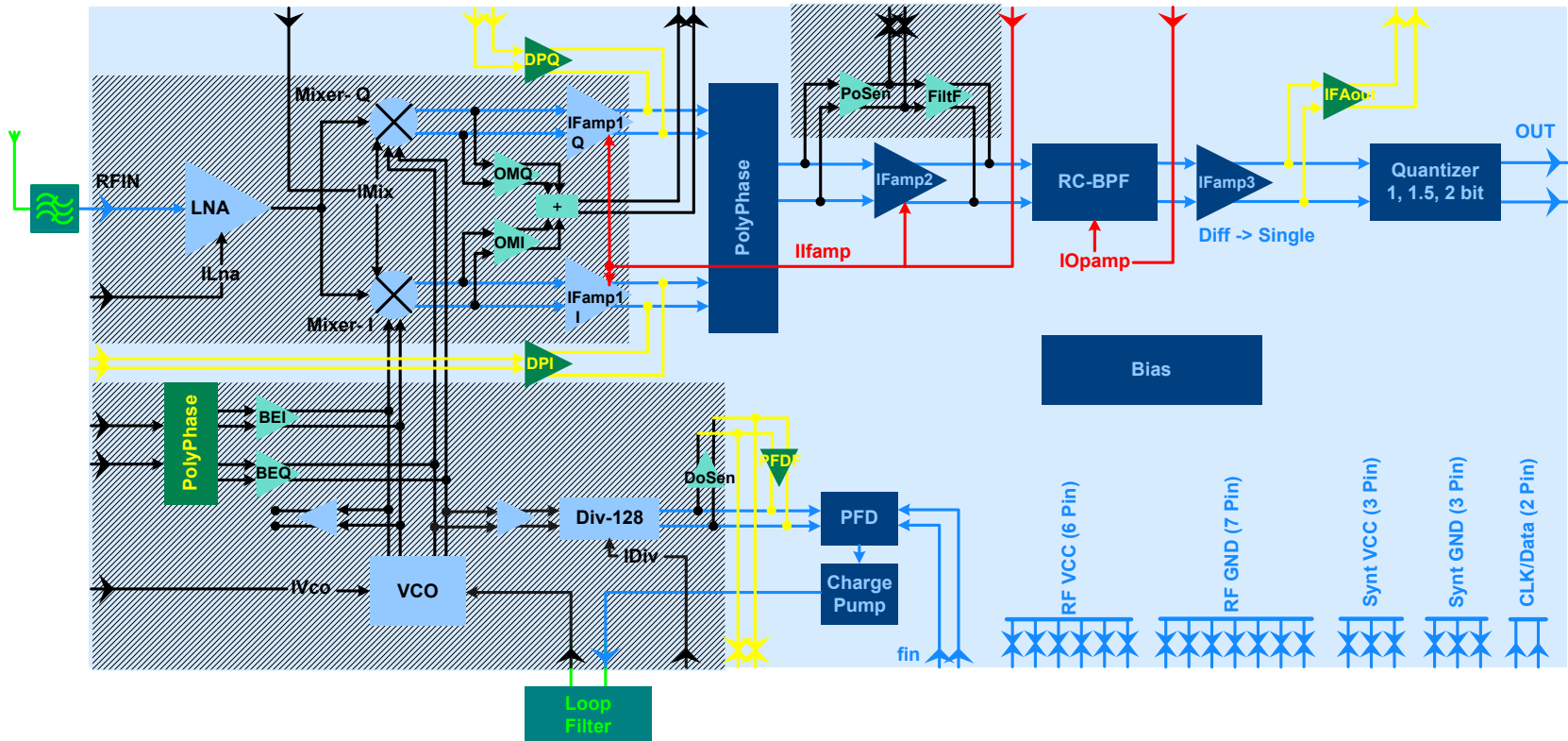# *Mode 4, IF Test*
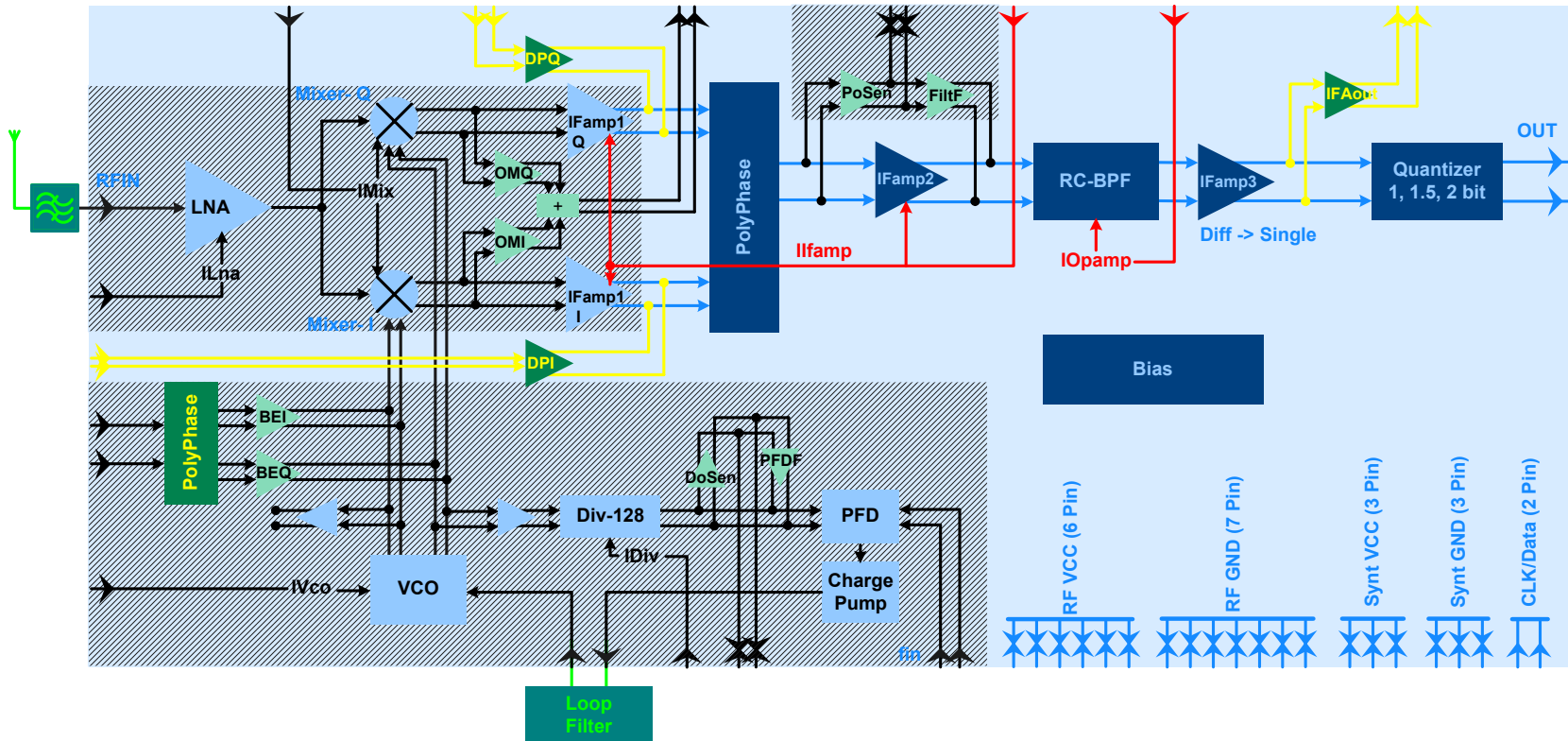
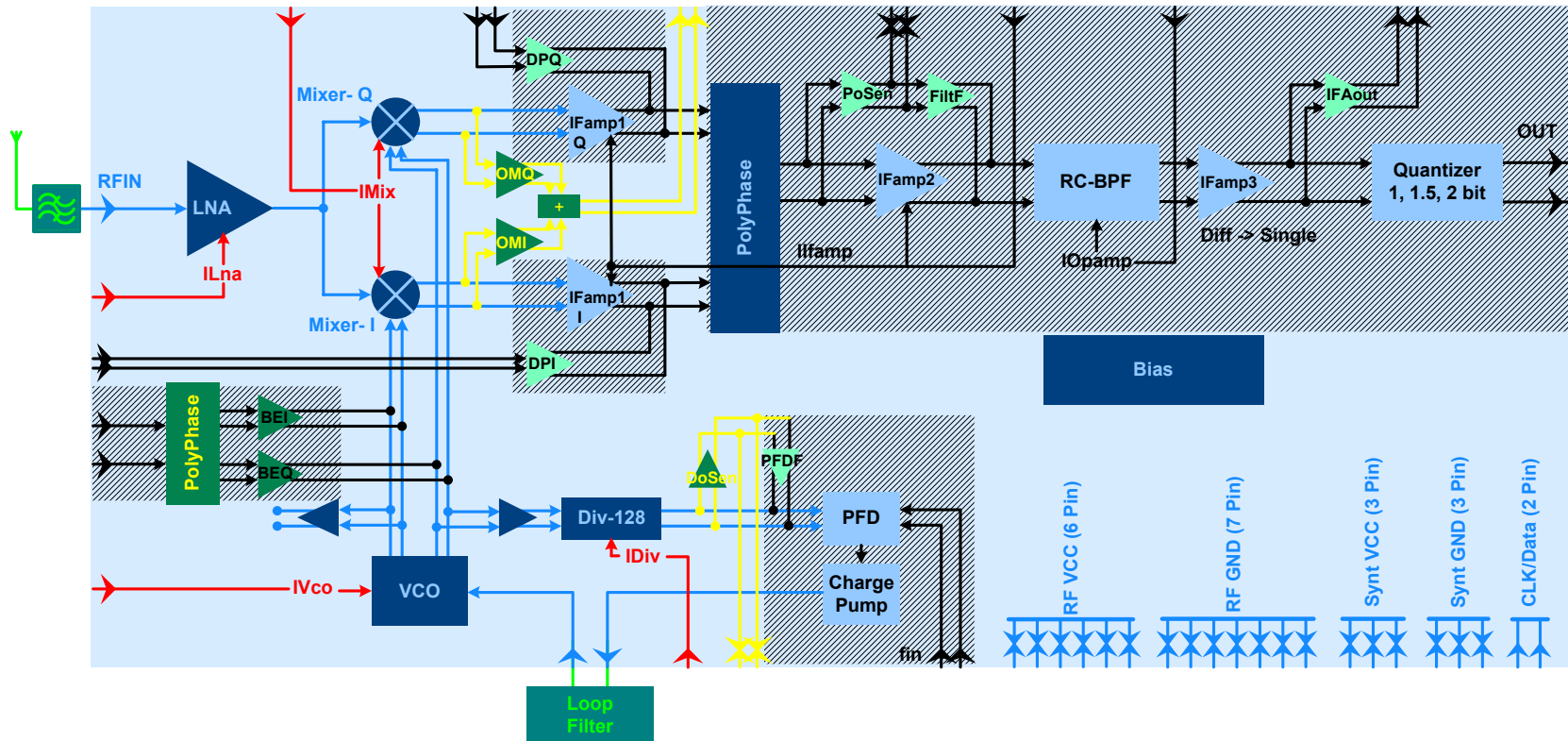- Fault detecting blocks:
  - IFamp2, Quantizer

Mode 5, RC Filter

- Fault detecting blocks:
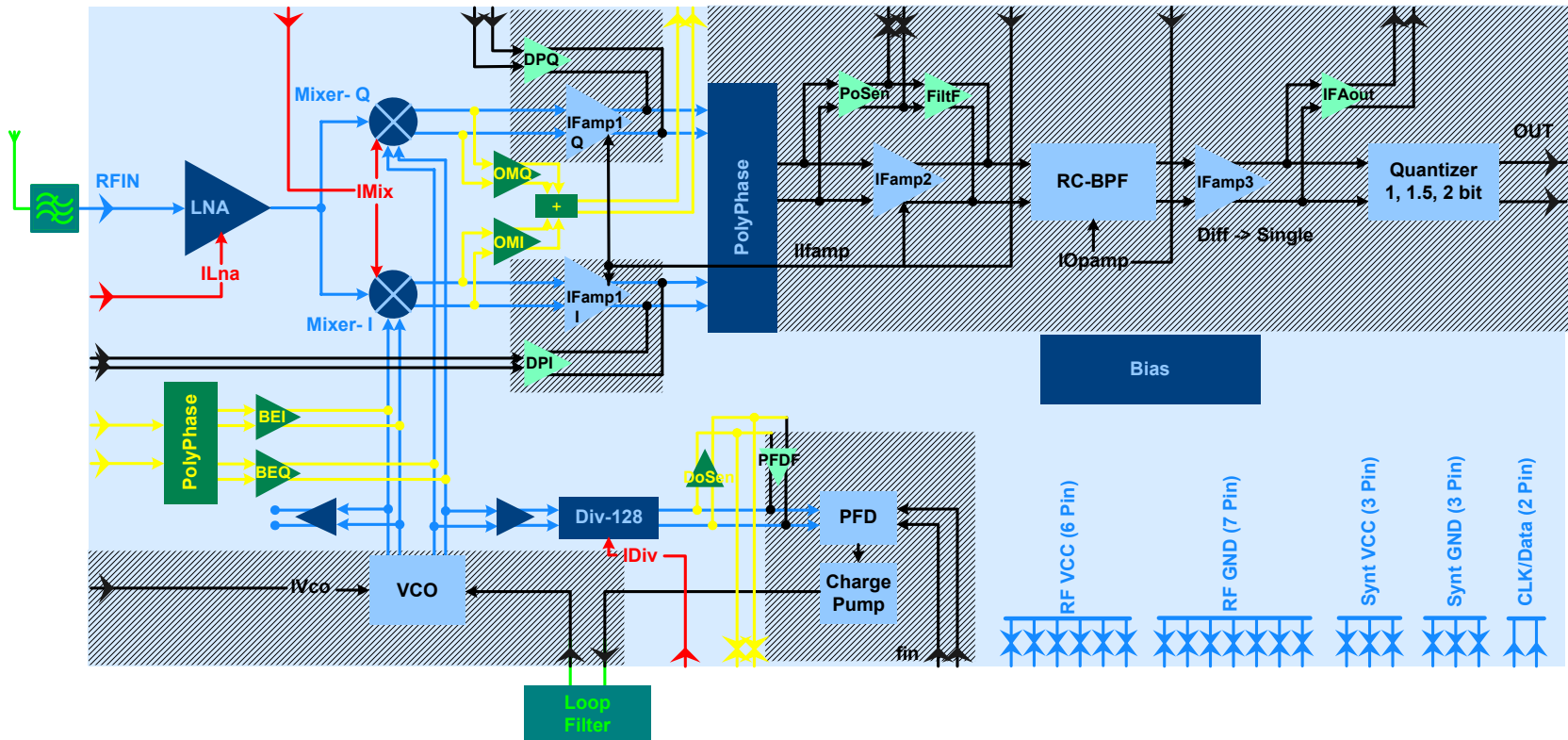 - RC Filter, Quantizer

Mode 6, PFD Test/ IFamp2

- Fault detecting blocks:
  - PFD, Charge Pump, IFamp2, Quantizer

Mode 7, Mixer/ VCO Test

- Fault detecting blocks:
  - VCO, LNA, Mixers

Mode 8, Mixer/ Ext. LO

- Fault detecting blocks:
  - LNA, Mixers, Divider

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The GPS receiver specifications

|	
Supply Voltage	**1.8 volt**
Technology	**0.18 um, CMOS**
Architecture	**Low IF**
Input RF Frequency	**1575.42 MHz, GPS L1**
LO Frequency	**1571.328 MHz**
Input Matching	**<-12dB （50Ω）**
Noise Figure	**3 dB**
Total Voltage Gain	**120 dB**
VGA Range	**55 dB**
Image Rejection	**-20 dB**
Output Format	**1, 1.5 and 2 bit (FSample=4f0 MHz)**
Power Consumption	**19.5 mA at 1.8 volt**
Chip Area	**6.61 mm2**

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Current Consumption

| Section name	Block name	Current Consumption (mA)
RF section		5.086
	LNA	2.504
	Mixer	1.291
IF section		6.252
	IF	5.929
	Digital section	0.323
Synthesizer		6.711
	VCO	2.096
	Synth-HF section	1.339
	Synth-LF section	3.276
Bias		1.041
	BG-Bias	1.041
Total		**19.09**

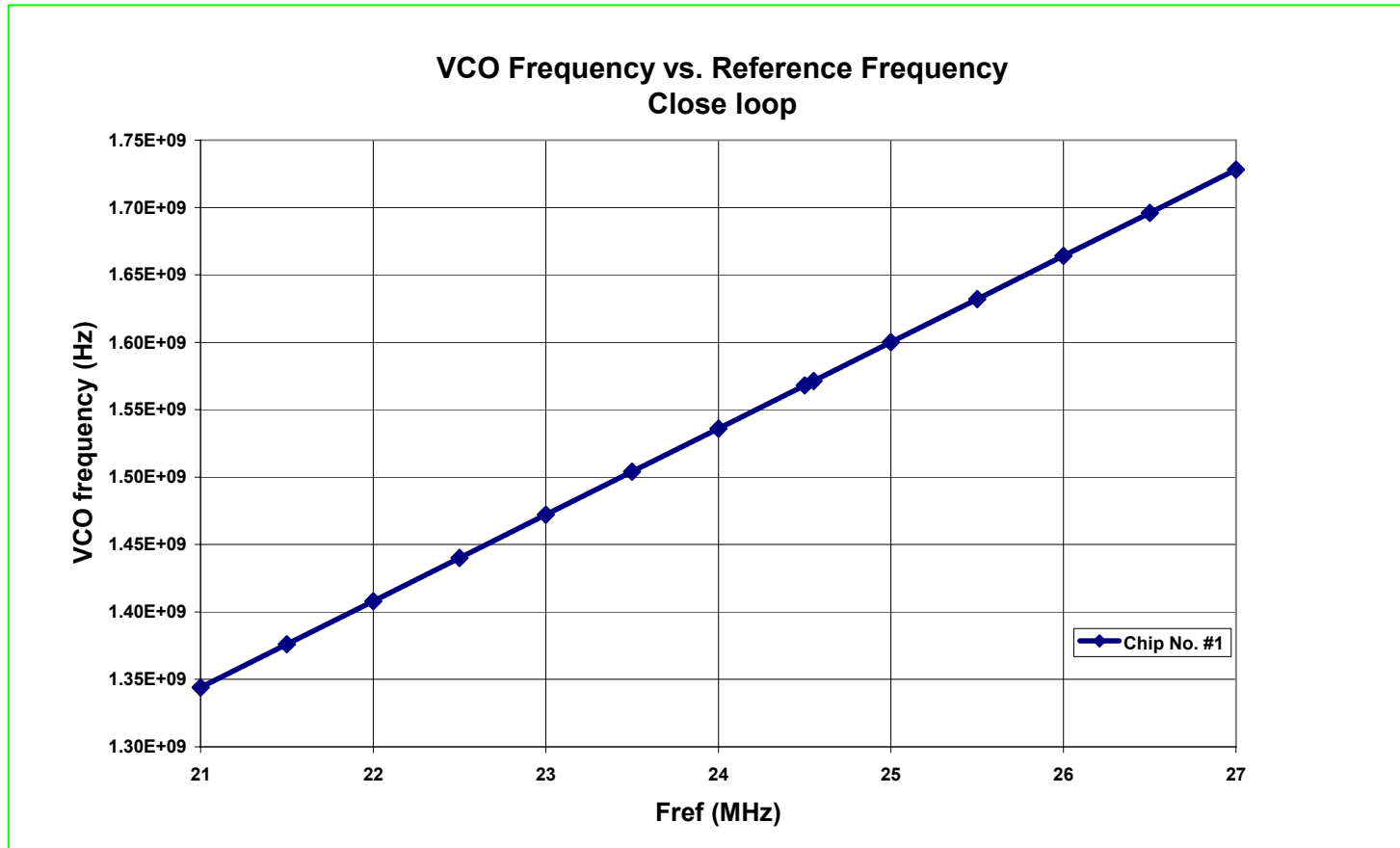# IF filter frequency response and variable gain range
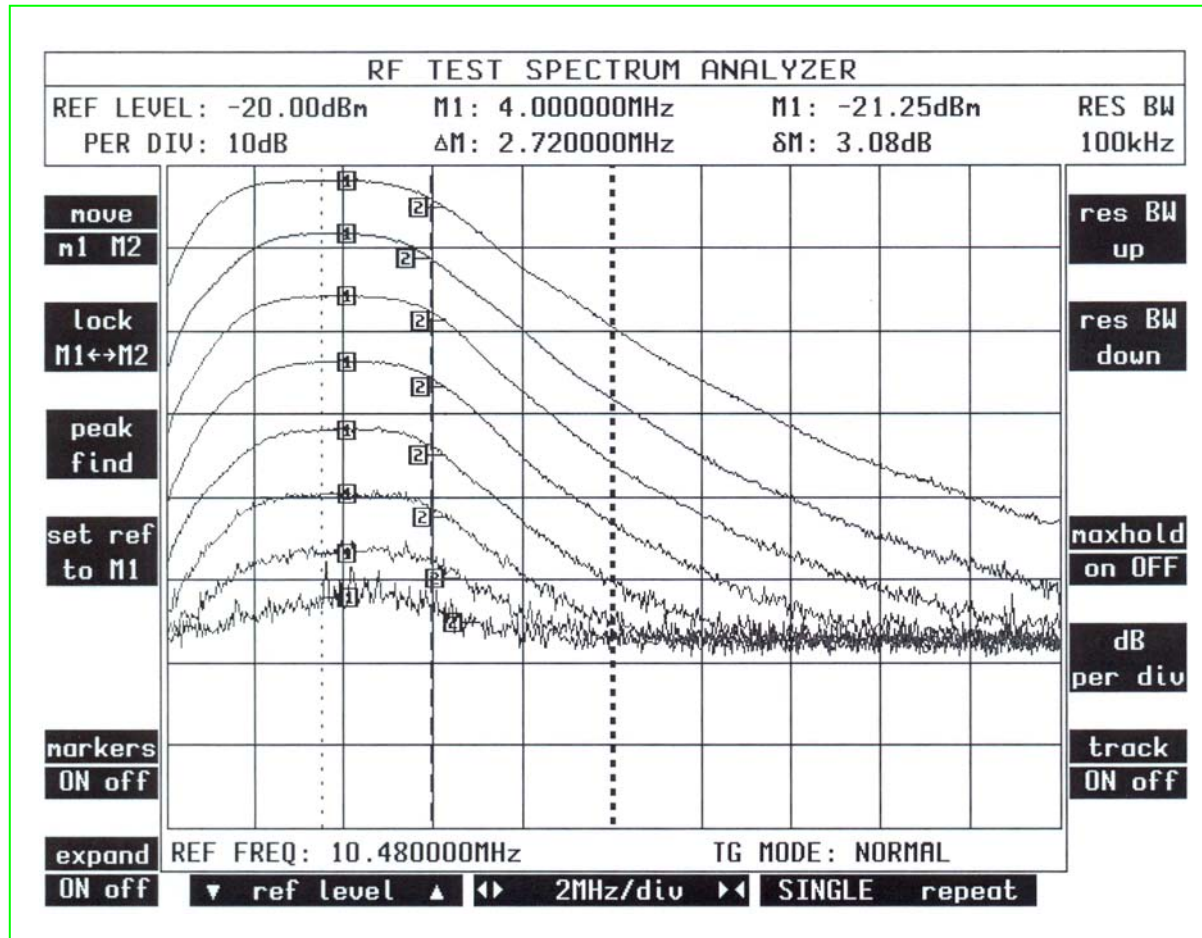
1-bit quantizer output

2-bit quantizer output

Synthesizer Lock Range

VCO Frequency vs. Reference Frequency
Close loop
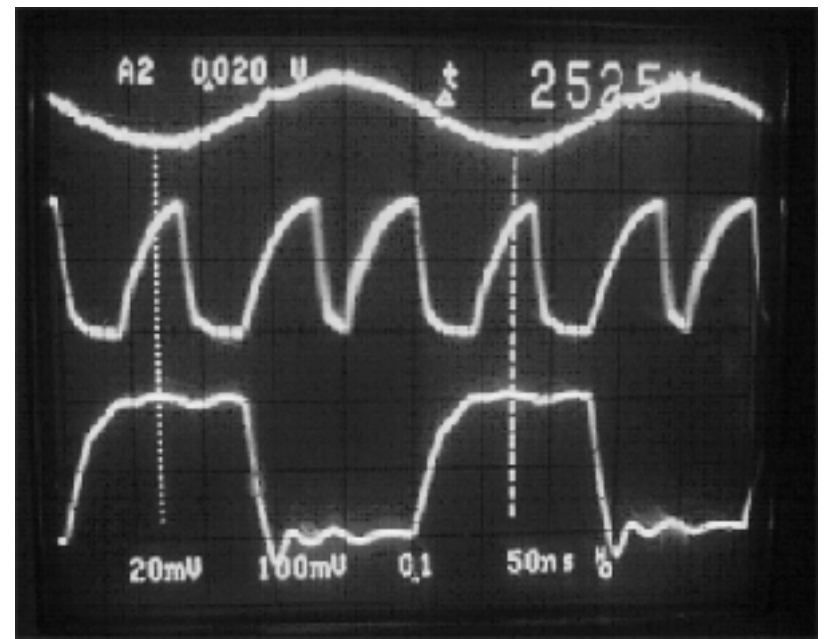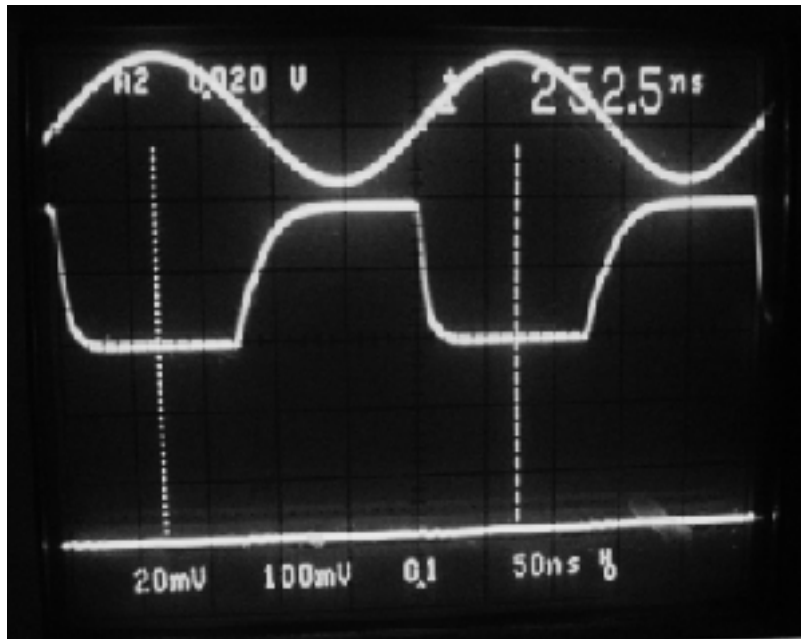
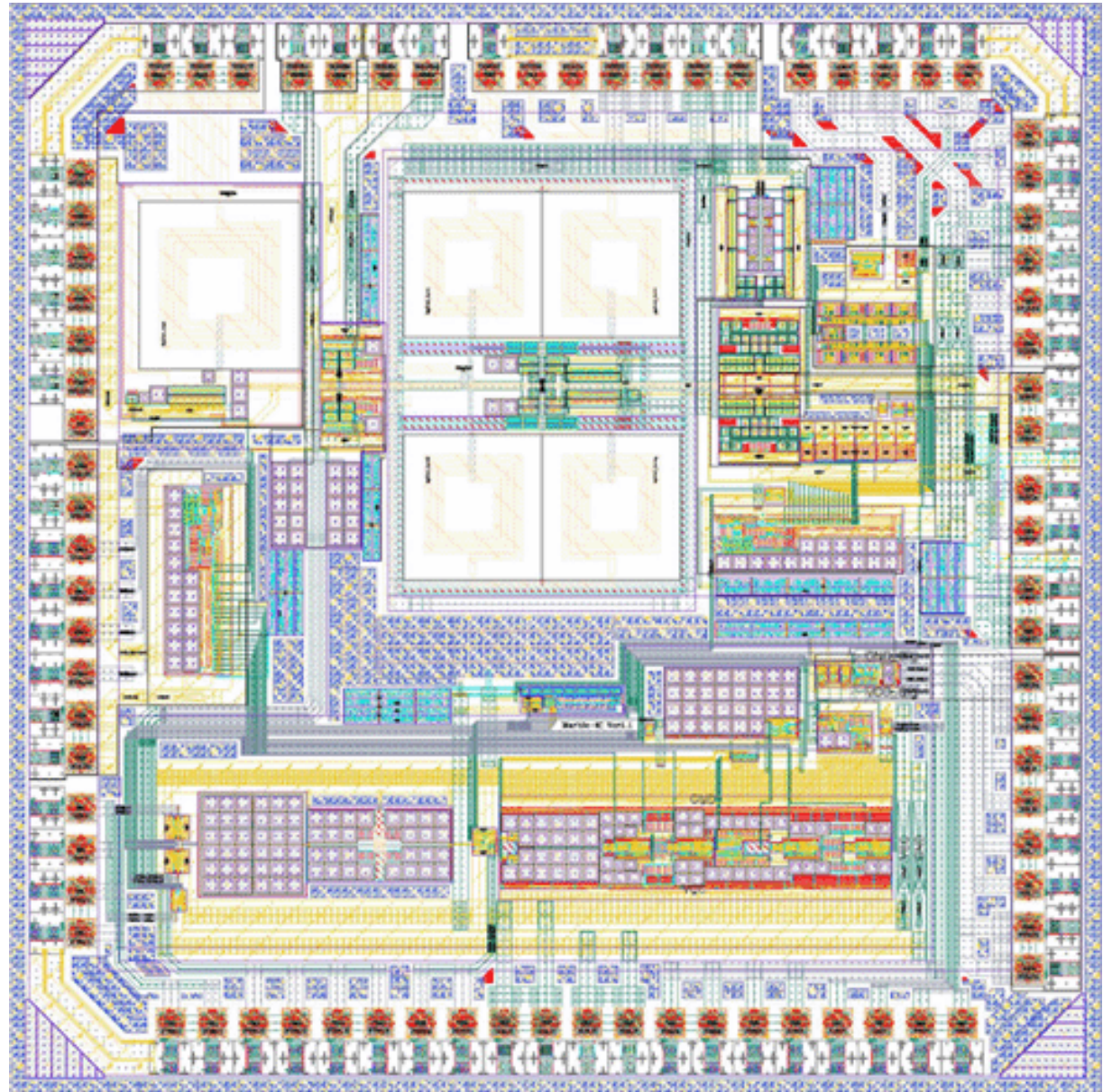| Reference freq (MHz)	VCO freq (GHz)
21.00	1.344
24.55	1.571
27.00	1.728

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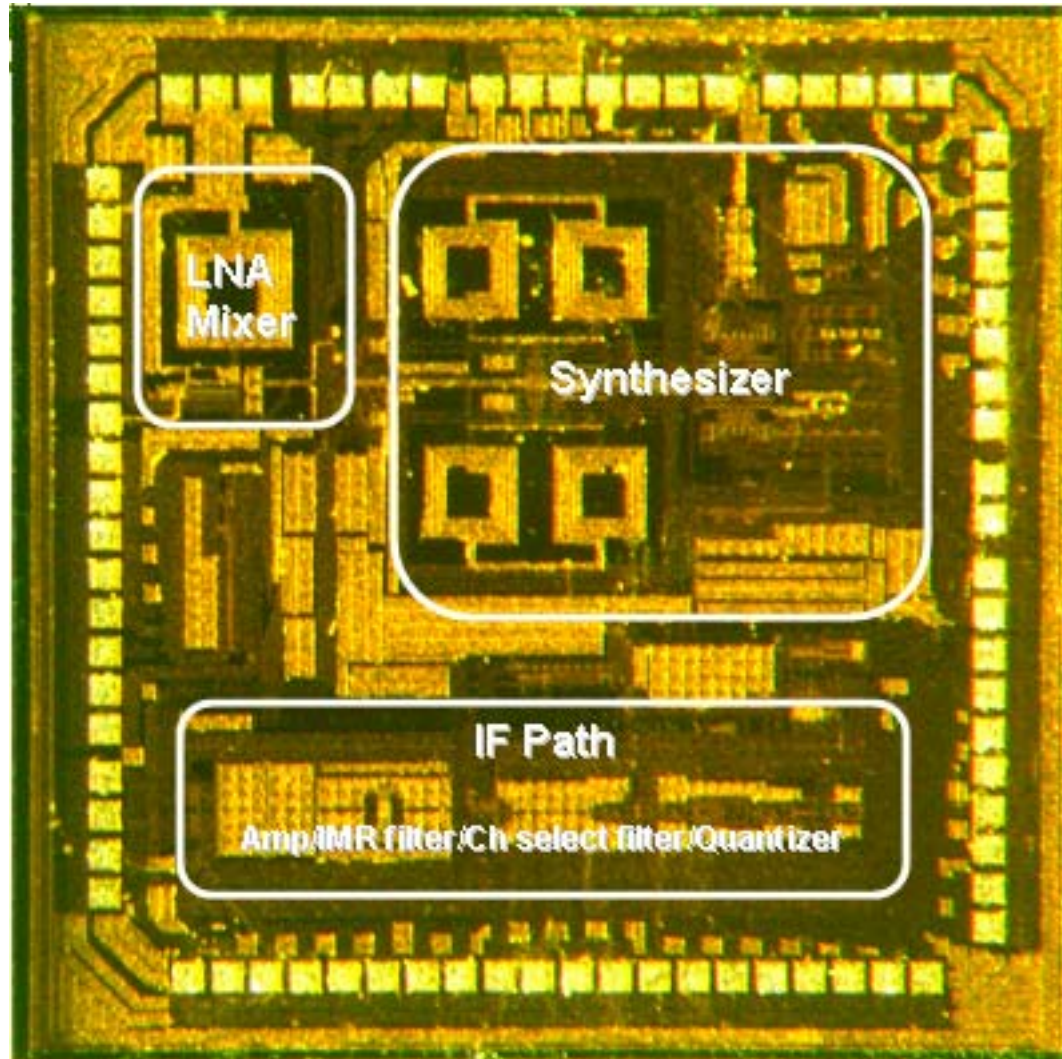- Measurement results
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Marble-IC2 Pinout

MARBLE-IC2

Top pins (left to right):
- 48 VCC_LNA
- 47 GND_MixI
- 46 VCC_Mix
- 45 GND_MixQ
- 44 FilterOUT
- 43 EXT_LOp
- 42 EXT_LOn
- 41 VCC_VCO
- 40 GND_VCO
- 39 FilterIN
- 38 VCC_LF
- 37 Frefp

Left pins (top to bottom):
- 1 GND_LNA2
- 2 GND_LNA1
- 3 IN_RF
- 4 GND_BG
- 5 ILNAcont
- 6 IMIXcont
- 7 IRCFcont
- 8 IIFA12cont
- 9 VCC_BG
- 10 OMIXn
- 11 OMIXp
- 12 IFTNp_I

Right pins (top to bottom):
- 36 Frefn
- 35 GND_LF
- 34 EXT_IVCO
- 33 EXT_IDiv
- 32 GND_HF
- 31 DivPFDp
- 30 DivPFDn
- 29 VCC_HF
- 28 GND_Dig
- 27 OUT_0
- 26 OUT_1
- 25 VCC_Dig

Bottom pins (left to right):
- 13 IFTINp_Q
- 14 IFTINn_Q
- 15 IFTNn_Q
- 16 RCFTIOp
- 17 RCFTIOn
- 18 VCC_IF
- 19 GND_IF
- 20 IFA3Op
- 21 IFA3On
- 22 CLOCK
- 23 DATA
- 24 IBIAST

Layout

Die Size : 2573.200 * 2571.015 (μm*μm) = 6.61 mm^2

Die Photograph

Marble-IC2 Package

Package type for the GPS-RF chip is
TQFP-48 pin.

Thank You...