A Multi-Drop Transmission-Line Interconnect in Si LSI

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1. **Background and purpose**

**Global Interconnect**

Delay & Power consumption: The enduring obstacles

**Transmission Line Interconnect**

- Signals can propagate at near speed-of-light.
- The conventional on-chip TL interconnects are peer-to-peer ones.

We propose the on-chip TL interconnect with branches.
2. Branching structure

A brute-force branch

Impedance mismatch causes reflection.

Used branching structure

※$Z_0$: Characteristic impedance

Branches contribute to reduce the area of Tx and wiring and the power of Tx.

$Z_0$ is hardly changed by branching.
3. Test circuit for branches

Transistors at branching nodes are modeled as capacitors.

- 0.18 μm CMOS process
- Line width: 2.4 μm
- Z₀ = 50 Ω

Assumption: Acceptable degradation of eye-height is 5%.

→ 75 fF can be connected to the single-ended transmission line.

\[ C_{\text{total}} = 5C \]
4. Measurement results

The proposed interconnect achieves the lowest power and delay although it has a branch.

Simulated results

<table>
<thead>
<tr>
<th></th>
<th>Delay [ps/cm] @4Gbps</th>
<th>Power [mW] @4Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>The proposed (with a branch)</td>
<td>144</td>
<td>6.3</td>
</tr>
<tr>
<td>RC line[1] (no branches)</td>
<td>500</td>
<td>15</td>
</tr>
</tbody>
</table>

5. Conclusion

- We have proposed an on-chip transmission-line interconnect with branches.
- In the measurement result, the proposed interconnect realizes 4Gbps signal transmission.
- Transmission line interconnects can improve delay and power of a branching global-interconnect as well as a peer-to-peer interconnect, which will contribute speeding-up and power saving of LSI.