A 0.35um CMOS 1,632-gate count Zero-Overhead Dynamic Optically Reconfigurable Gate Array VLSI

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Dynamic Reconfiguration Advantage

Drawback of Conventional Programmable Devices

- LUT structure
- D-Flip Flop structure
- Transmission Gate

Drawback is based on LUT and transmission gate structure

Conventional Implementation
- Multi-Functions Unit or General purpose Unit

Dynamic reconfiguration Implementation
- Single Function Unit
- Parallel computation
Overview of optically reconfigurable gate array

Holographic Memory (virtual gates)

Laser Diodes Array

Large bandwidth - optical connections

ORGA- VLSI (real gates) which has a programmable gate array with photodiodes

Holographic Memory


2) According to the prospect of a future holographic memory, one cubic centimeter holographic memory will store 1 terabit, corresponding to about 250 billion gate count.
Improved Dynamic Optical Reconfiguration Circuit

- New circuit consists of a DORC and a pass transistor.
- The pass transistor is used for blocking off the connection between reconfiguration circuit and gate array circuit.
- The load capacitance is used for keeping the gate array state.
- The load capacitance is sufficient to maintain the state of gate array while reconfiguring.
An ORGA takes Island-Style gate array. The basic structure is same as that of current FPGAs. However, each programming element of the gate array is connected to a photodiode. Thereby, all state of the gate array can be programmed in perfectly parallel.
1,632 gate count ZO-DORGA-VLSI

Specification of a DORGA-VLSI

<table>
<thead>
<tr>
<th>Specification</th>
<th>Details</th>
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</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.35 μm double-poly triple-metal CMOS process</td>
</tr>
<tr>
<td>Chip size</td>
<td>4.9 × 4.9 [mm]</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>Core 3.3V, I/O 3.3V</td>
</tr>
<tr>
<td>Photodiode size</td>
<td>9.5 × 8.8 [μm]</td>
</tr>
<tr>
<td>Horizontal Distance between Photodiodes</td>
<td>34.5 [μm]</td>
</tr>
<tr>
<td>Vertical Distance between Photodiodes</td>
<td>33.0 [μm]</td>
</tr>
<tr>
<td>Number of Photodiodes</td>
<td>6,213</td>
</tr>
<tr>
<td>Av. Aperture Ratio</td>
<td>4.24%</td>
</tr>
<tr>
<td>Number of Logic Blocks</td>
<td>48</td>
</tr>
<tr>
<td>Number of Switching Matrices</td>
<td>63</td>
</tr>
<tr>
<td>Number of Wires in a Routing Channel</td>
<td>8</td>
</tr>
<tr>
<td>Number of I/O bits</td>
<td>24</td>
</tr>
<tr>
<td>Gate Count</td>
<td>1,632</td>
</tr>
</tbody>
</table>

Photograph of a DORGA-VLSI
Design of a future high density DORGA

Specifications of a ZO-ORGA

- **Technology**: 0.35 μm 3-metal CMOS process
- **Chip size**: 9.8 × 9.8 [mm²]
- **Photodiode size**: 9.5 × 8.8 [μm²]
- **Horizontal distance**: 34.5 [μm]
- **Vertical distance between photodiodes**: 33.0 [μm]
- **Number of Photodiodes**: 38,591
- **Number of Logic Blocks**: 336
- **Number of Switching Matrices**: 375
- **Number of I/O Blocks**: 8 (32-bit)
- **Wiring channel**: 8
- **Gate Count**: 11,424 gates
Conclusion

• This presentation presents

(a) the design of a fabricated world’s largest 1,632 gate count ZO-DORGA-VLSI,
(b) an over 10,000 gate count VLSI by using 9.8mm square CMOS process chip and same logic blocks and switching matrices.

Acknowledgments
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