Low-Power High-Speed 90-nm CMOS Clock Drivers

T. Enomoto, S. Nagayama and N. Kobayashi
Chuo University, Tokyo, Japan
ASP-DAC’2007, Yokohama, Japan, Jan. 24, 2007
Register Array Modules

Technology: 90-nm, Triple-Well, 6-Layer, Cu, CMOS

Gate Lengths: $L_n = L_p = 0.1$ mm

Channel Widths (Logic): $W_n = 1.08 \mu W$, $W_p = 1.64 \mu W$

Channel Widths (Switch): $W_n = 0.54 \mu W$, $W_p = 0.82 \mu W$

Threshold Voltages: $V_{tn} = 0.222$ V, $V_{tp} = -0.241$ V

No. of D-FF ($M = m \times n$) = 40

<table>
<thead>
<tr>
<th>$m$</th>
<th>$n$</th>
<th>$M/m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>
Power Dissipation and Signal Propagation Delay of a Single Logic Gate

Power due to dynamic current

\[ p_D(n) = (An + B) \cdot V_D^2 \cdot f \]

Power due to short-circuit current

\[ p_S(m, n) = \frac{E(m + F)^G \cdot (V_D - 2V_T)^3 \cdot f}{(1 + Hn)^J} \]

Signal Propagation Delay

\[ t_d \approx \frac{(C_m + C_n)V_D^2}{\beta (V_D - V_{th})^2} \approx \frac{2(C_m + C_n)}{\beta(V_D - V_{th})} \]

\[ \propto (Am + B) + (An + B) = A(m + n) + 2B \]

\[ = A(m + \frac{M}{m}) + 2B \]

at \( m = 1 \) & \( m = M \)

\[ t_d \propto A(M+1)+2B \]

at \( m = n \)

\[ t_d \propto 2AM^{0.5}+2B \]
Signal Propagation Delay of 90-nm Register Array Modules (SPICE Simulation)

\[ m = 1 \quad m = 10 \]
\[ n = 40 \quad m = 4 \]

\[ t_T = 0.26 \text{ ns} \quad t_T = 0.95 \text{ ns} \]

No. of D-FF \( (M = m \times n) = 40 \)

\( t_T \) is considerably reduced
As $m$ increases, $t_1$ increases, $t_{2-1}$, $t_{2-2}$ decrease, $t_3$ is constant.
Signal Propagation Delay ($t_T$) & Optimized $m$ for Minimum $t_T$ of 90-nm Register Array Modules (SPICE Simulation)

$t_T$ is minimized at $m \approx 1.5M^{1/2}$
Power Dissipation of 90-nm Register Array Modules

(SPICE Simulation)

As $m$ increases
$P_3$ decreases
Others increase.
Power Dissipation ($P_T$) & Optimized $m$ for Minimum $P_T$ of 90-nm Register Array Modules (SPICE Simulation)

$P_T$ is minimized at $m \approx 1.5M^{1/2}$
90-nm CMOS LSI Chip with 6 Register Array Modules

Technology:
90-nm, Triple-Well, 6-Layer, Cu, CMOS

Chip Size:
2.5 mm × 2.5 mm

No. of D-FF \( (M = m \times n) = 40 \)

\[
\begin{array}{cc}
m & n = M/m \\
1 & 40 \\
5 & 8 \\
8 & 5 \\
10 & 4 \\
20 & 2 \\
40 & 1 \\
\end{array}
\]
Power Dissipation of 90-nm Register Array Modules
(Experimental Results)

- Signal Propagation Delay ($t_T$)
  
  $0.95$ nsec ($m = 1$)
  
  $0.26$ nsec ($27.4\%$) ($m = 10$)

- Power Dissipation ($P_T$)
  
  $293.1$ µW ($m = 1$)
  
  $159.6$ µW ($54.5\%$) ($m = 10$)

$t_T$ and $P_T$ are minimized at $m \approx 1.5M^{1/2}$