A 2.8V Multibit Complex Bandpass Delta-Sigma AD Modulator in 0.18μm CMOS

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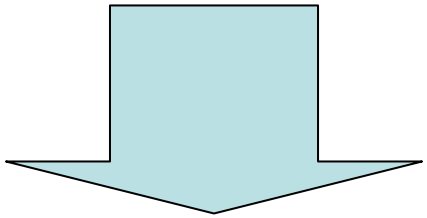
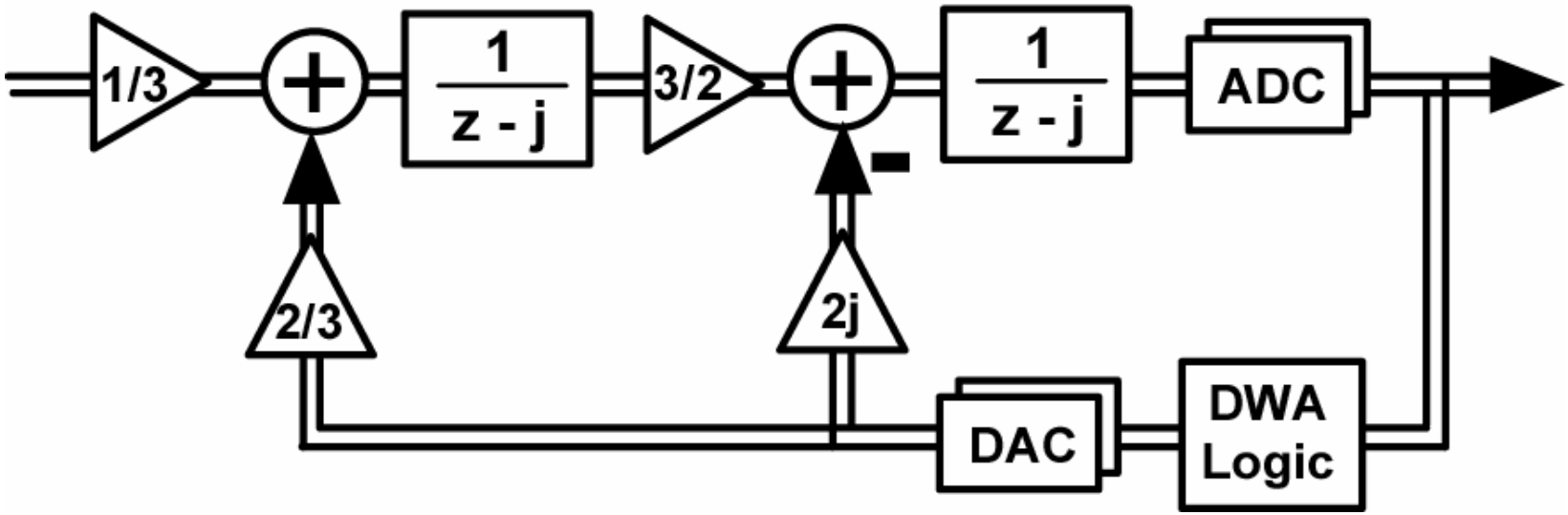
Motivation

Low power ADC in low-IF receiver targeted for wireless system.



Complex bandpass Delta-Sigma AD modulator

Proposed Architecture

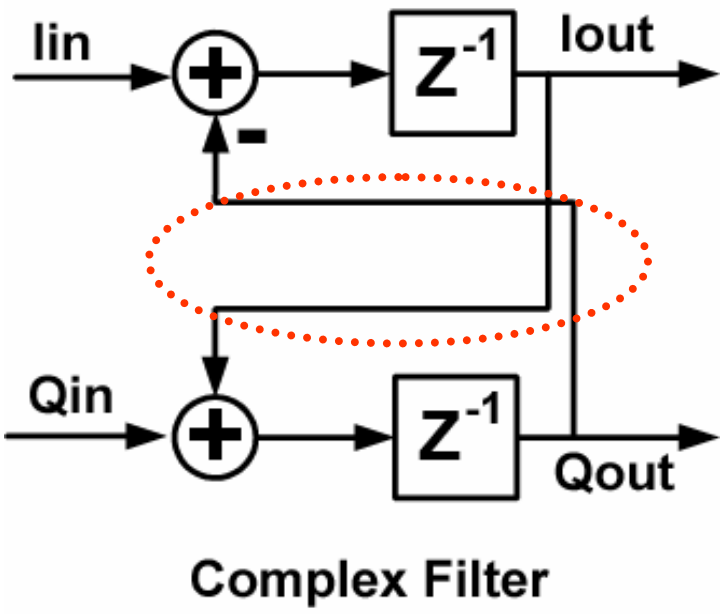


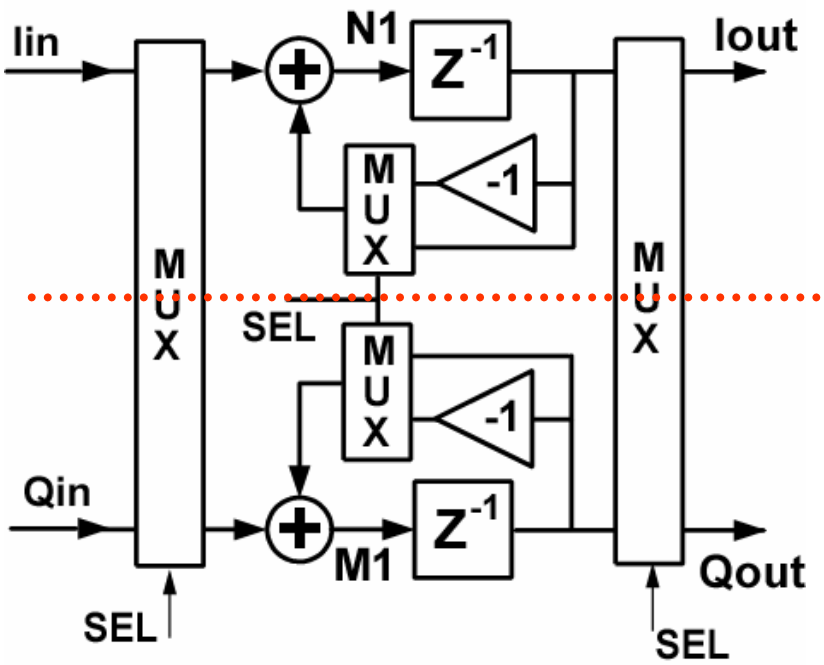
- 2nd-order modulator
- New complex bandpass filter
- Multi-bit ADCs/DACs
- Complex DWA algorithm

Complex BPDSM with Low-power

- 2nd order modulator
  - Less hardware, low power
- 9-level ADCs/DACs
  - Stability improvement
  - Low quantization error
  - Power reduction of amplifiers
- Problems
  - I,Q mismatch ⇨ I,Q Dynamic Matching
  - Nonlinearities of multibit DAC ⇨ DWA

I,Q Dynamic Matching of Complex Filter





Conventional complex filter

I &Q crossing paths

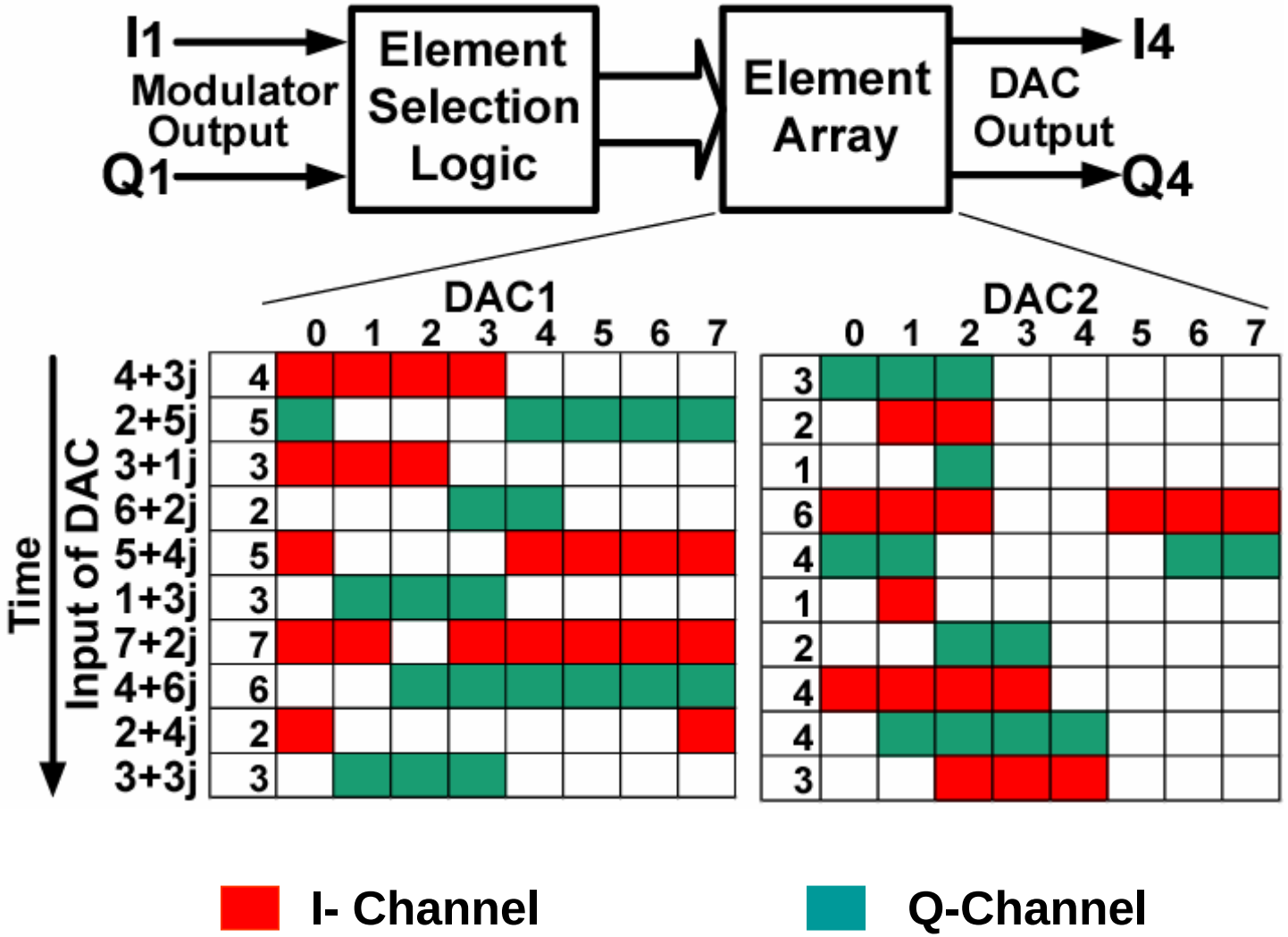
$$H_1(z) = \frac{1}{z - j}$$

Proposed complex filter

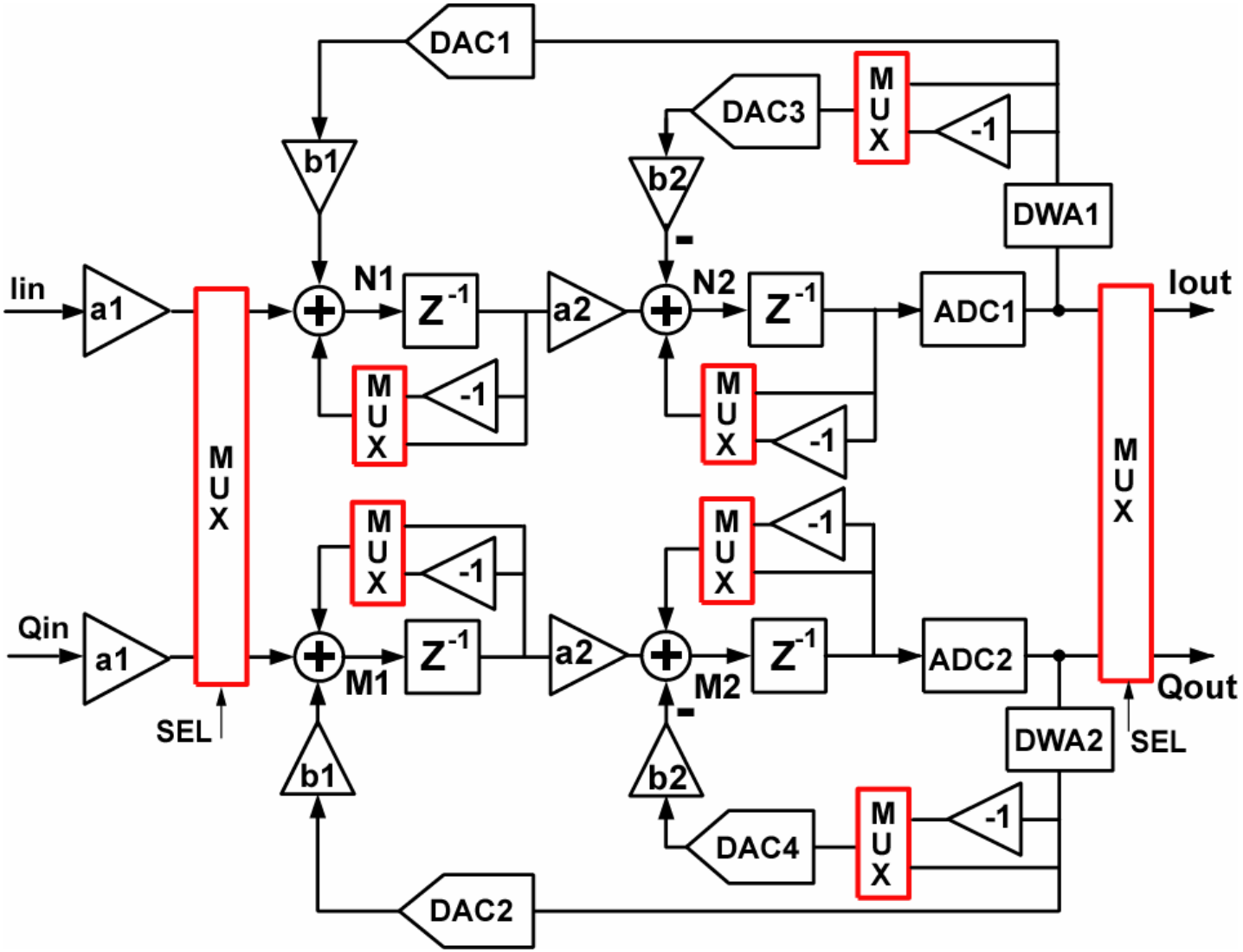
Upper, lower separated paths

- **I,Q mismatch reduction.**
- **Layout simplification.**

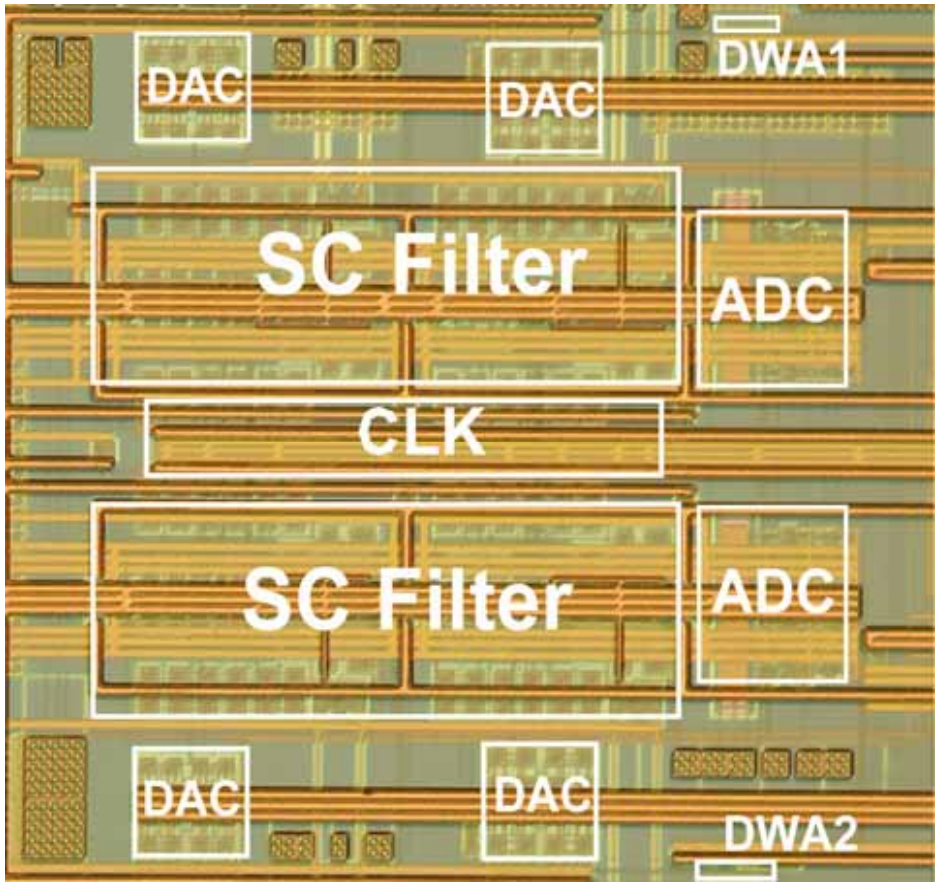
Selected segment in Complex DWA



Proposed Structure

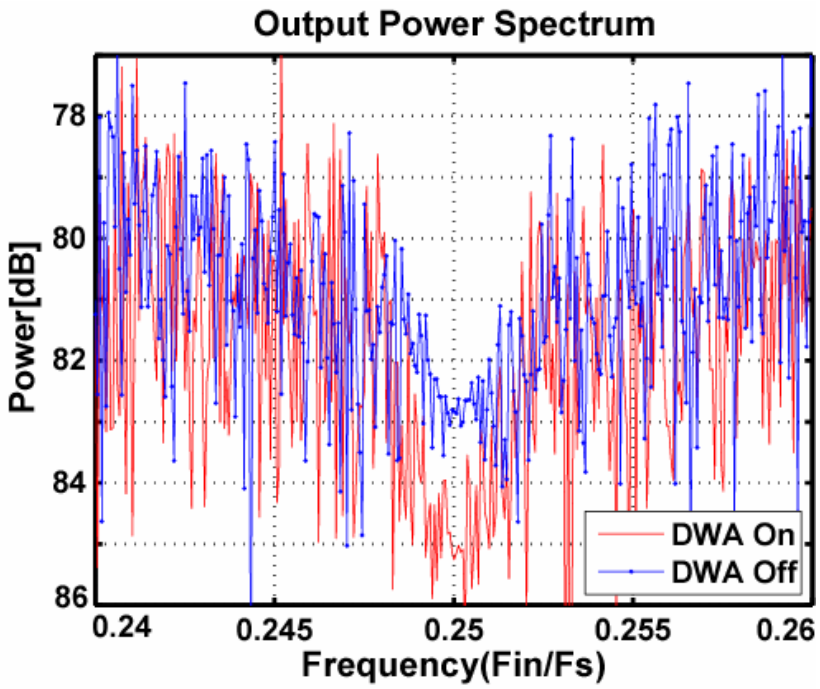


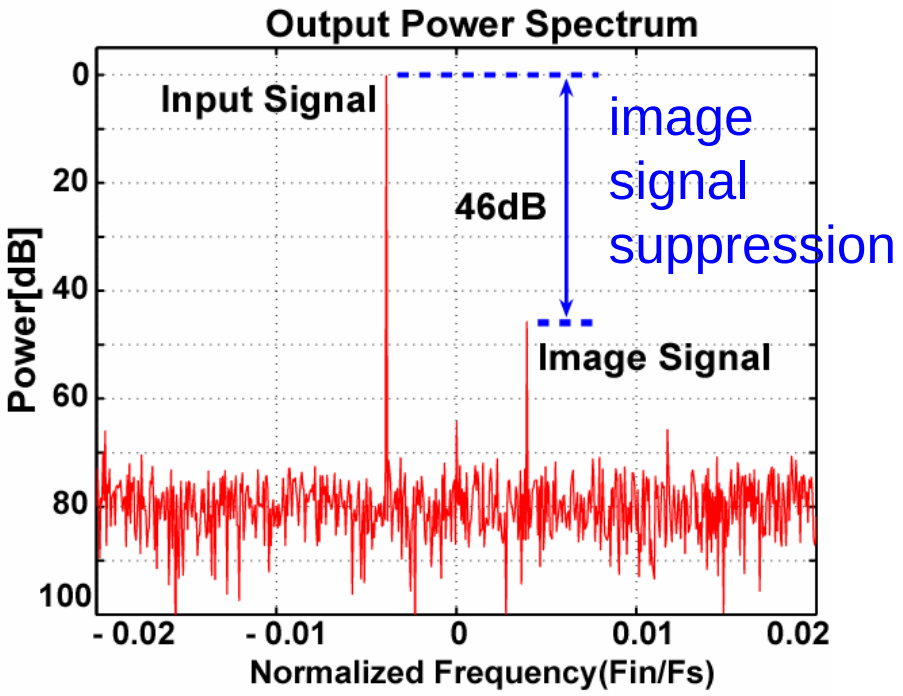
Chip Implementation



- 1P6M 0.18μm CMOS Process
- Core size 1.4 *1.3mm^2.

Measured Results

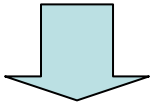




Supply voltage	**2.8V**
Sampling Frequency	**20MHz**
SNDR	**64.5dB @ BW=78kHz**
Power consumption	**28.4mw**

Conclusion

- A 2nd-order multi-bit complex bandpass delta-sigma modulator



- Complex filter with dynamic matching
  - I,Q mismatch reduction
  - Layout simplification
- Complex DWA
  - Suppression of multibit DACs nonlinearities
- Chip measurements demonstrated these