A 2.8V Multibit Complex Bandpass Delta-Sigma AD Modulator in 0.18µm CMOS

H. San, Y. Jingu, H. Wada, H. Hagiwara, A. Hayakawa, H. Kobayashi, M. Hotta

1) Gunma University
2) Musashi Institute of Technology
Motivation

Low power ADC in low-IF receiver targeted for wireless system.

Complex bandpass Delta-Sigma AD modulator
Proposed Architecture

- 2\textsuperscript{nd}-order modulator
- New complex bandpass filter
- Multi-bit ADCs/DACs
- Complex DWA algorithm
Complex BPDSM with Low-power

- 2\textsuperscript{nd} order modulator
  - Less hardware, low power

- 9-level ADCs/DACs
  - Stability improvement
  - Low quantization error
  - Power reduction of amplifiers

- Problems
  - I,Q mismatch $\rightarrow$ I,Q Dynamic Matching
  - Nonlinearities of multibit DAC $\rightarrow$ DWA
I,Q Dynamic Matching of Complex Filter

Conventional complex filter
I & Q crossing paths

Proposed complex filter
Upper, lower separated paths

\[ H_1(z) = \frac{1}{z - j} \]

- I,Q mismatch reduction.
- Layout simplification.
Selected segment in Complex DWA

![Diagram showing element selection logic and digital-analog converters (DACs) for I- and Q-channels. The diagram illustrates the mapping of input values to output segments for both channels.]
Chip Implementation

- 1P6M 0.18μm CMOS Process
- Core size 1.4 *1.3mm².
Measured Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>2.8V</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>20MHz</td>
</tr>
<tr>
<td>SNDR</td>
<td>64.5dB @ BW=78kHz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>28.4mw</td>
</tr>
</tbody>
</table>
Conclusion

• A 2\textsuperscript{nd}-order multi-bit complex bandpass delta-sigma modulator

• Complex filter with dynamic matching
  – I,Q mismatch reduction
  – Layout simplification

• Complex DWA
  – Suppression of multibit DACs nonlinearities

• Chip measurements demonstrated these