Substrate noise degrades performance of analog circuits

The techniques for suppression of substrate noise are not effective at high frequency

Design of feedfoward active substrate noise canceller is demonstrated

$L_{\text{gnd}}(\text{di/dt})$ is dominant in substrate noise

Power line $\text{di/dt}$ detector generates the anti-phase signals, and injected into the substrate
Results

- The chip is fabricated by 0.35um CMOS process (1P3M VDD=3.3V)
- Measurement results show that the minimum point of substrate noise exists when the canceller is on
- Measurement results show that 10-62% of the substrate noise reduction is achieved from 100MHz to 600MHz range