A 20Gbps Scalable Load Balanced Birkhoff-von Neumann Symmetric TDM Switch IC with SERDES Interface

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Outline

- High Speed **Scalable** Switch Architecture
- System Integration Results
- Sub-block Verification
  - TDM Switch Core with 8B10B CODEC
  - 16/20:1 SERDES Interface
  - Patent CML I/O Buffer
- Summary
Introduction

- Output-buffered switch: memory access limitation
- Input-buffered switch: 58% throughput

- Maximum matching: $O(N^{2.5})$
- Maximum weighted matching: $O(N^3\log(N))$
- Matching requires heavy computation as well as communication overheads
  ✓ SLIP, iSLIP algorithms and etc.
Load balanced Birkhoff-von Neumann switch

- 100% throughput
- Low average delay in heavy or bursty traffic
- Better buffer utilization
- Low hardware complexity
- Scalability

**LB-BvN Switch Architecture (2002)**

- **Impacts**
  - Quoted by many papers in last 3 years *(80%)*
  - Adopted by Prof. N. McKeown (Stanford University) to build a **100 Tbps** optical router
  - Prof. J. Chao (IEEE fellow) said this architecture opened a new avenue in high speed switching
  - Bell-Lab’s optical implementation

- **Folded version with symmetric patterns**

- **Scalability**: 64X64 or higher by banyan network
TDM Switch + CML SERDES Interface

- **Digital:** TDM switch core with 8B10B CODEC
  An 8x8 load balanced TDM switch module with 160MHz clock
  Symmetric and configurable patterns
  Pattern driver and monitor mode
- **Analog:** SERDES Interface (8 channels)
  Per channel supports 2.56Gbps data rate
  1:16/20 dual mode CML SERDES interface
  On-Chip PLL
- **Full chip switching rate 20Gbps**
Switch Core With 8B10B CODEC

<table>
<thead>
<tr>
<th>mode</th>
<th>Driver-to-Monitor</th>
<th>Bypass CODEC</th>
<th>CODEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Performance</td>
<td>300MHz</td>
<td>150MHz</td>
<td>148MHz</td>
</tr>
</tbody>
</table>

38.4Gbps !!
Dual Mode 16/20:1 SERDES

- **Dual Mode** SERDES was developed for 8B10B CODEC
- Compared with 8/10:1, 16/20:1 scheme reduces system core freq. by half for low power (50mW)
- **Half-rate** scheme are also introduced in SERDES itself
- In Half-rate, all static CMOS are used to replace SCL for low power (360mW)
CML Wide-band Techniques

- PMOS active load inductive-peaking (patent pending)
- Active feedback with current buffers
- Equalizer using Cheery-Hopper topology
- Negative Miller capacitance
Summary of Features

- 100% throughput
- Low average delay in heavy or bursty traffic
- Better buffer utilization
- Low hardware complexity
- Scalability
- Symmetric and configurable TDM pattern
- Using Folded version
- Using Banyan network technology
- BIST Mode & bypass CODEC mode
- Using dual mode 16/20:1 SERDES interface
- Using half-rate technology for power saving
- Active load inductive-peaking CML (patent pending)