Reconfigurable CMOS Low Noise Amplifier Using Variable Bias Circuit for Self Compensation

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1. Background

Si CMOS process technology

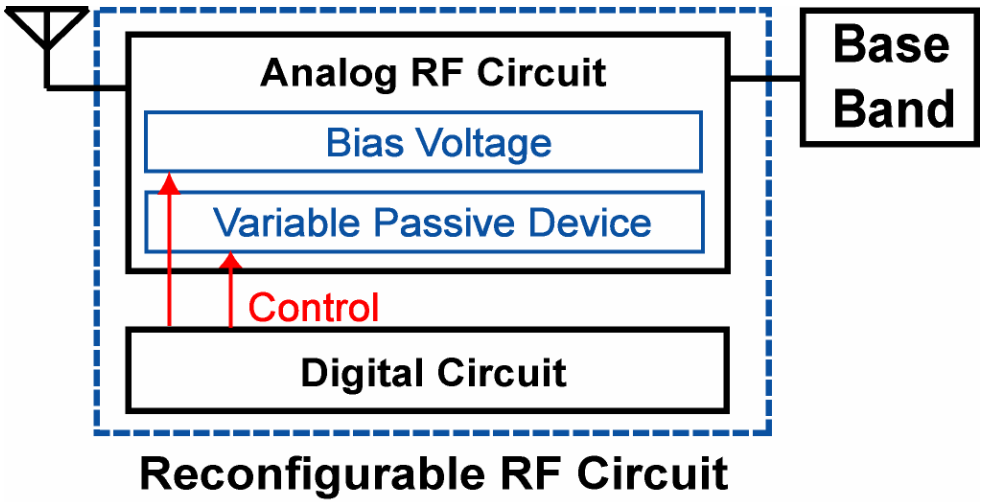
advantage

- **Low power**
- **Low cost**
- **Small size**
- **Mixed signal…**

disadvantage

- PVT variation
- Modeling error
- Noise condition…

We are aiming at reconfigurable RF circuits



We proposed the scheme for compensation of these disadvantages.

2. Purpose of this work

Purpose of this work

Realization of self compensation technique for reconfigurable RF circuits

Target : Low Noise Amplifier (LNA)

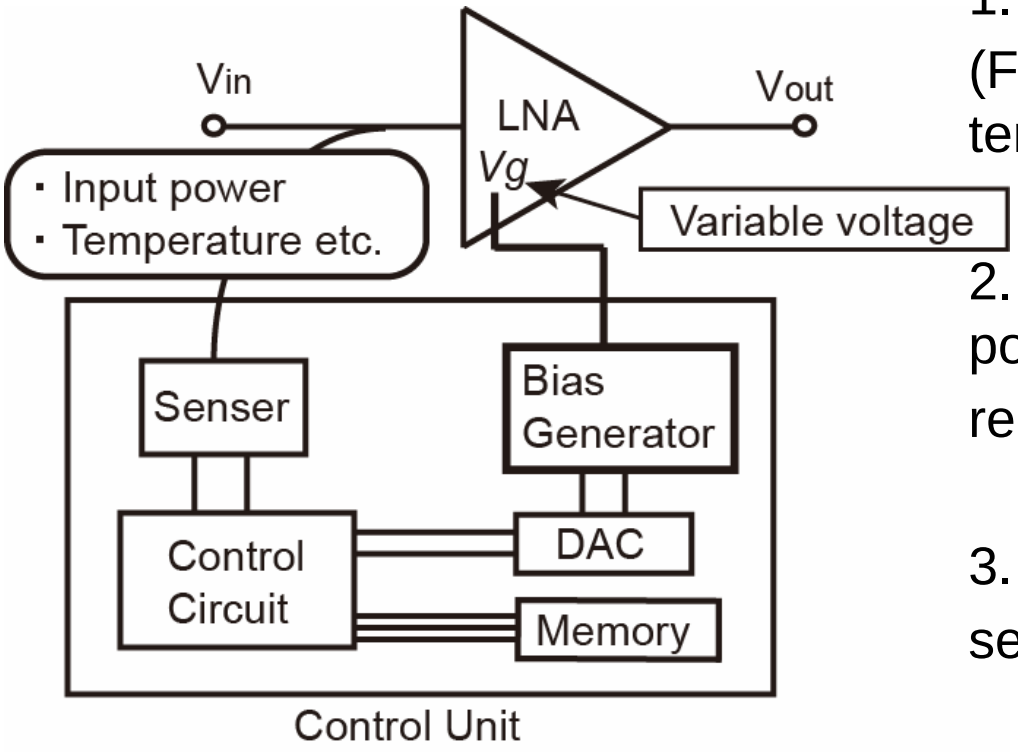
Proposed LNA

Circuit performance can be reconfigured by bias voltage

- Compensation of distortion
- Dynamic power reduction

Self compensation

3. Concept of the proposed LNA



1. Sensing characteristics
(For example input power, and temperature etc.)

2. According to temperature or input power, control circuit reads reconfigurable table from RAM.

3. DAC makes bias generator send proper bias voltage to the LNA.

4. The LNA characteristics change.

4. Proposed LNA design

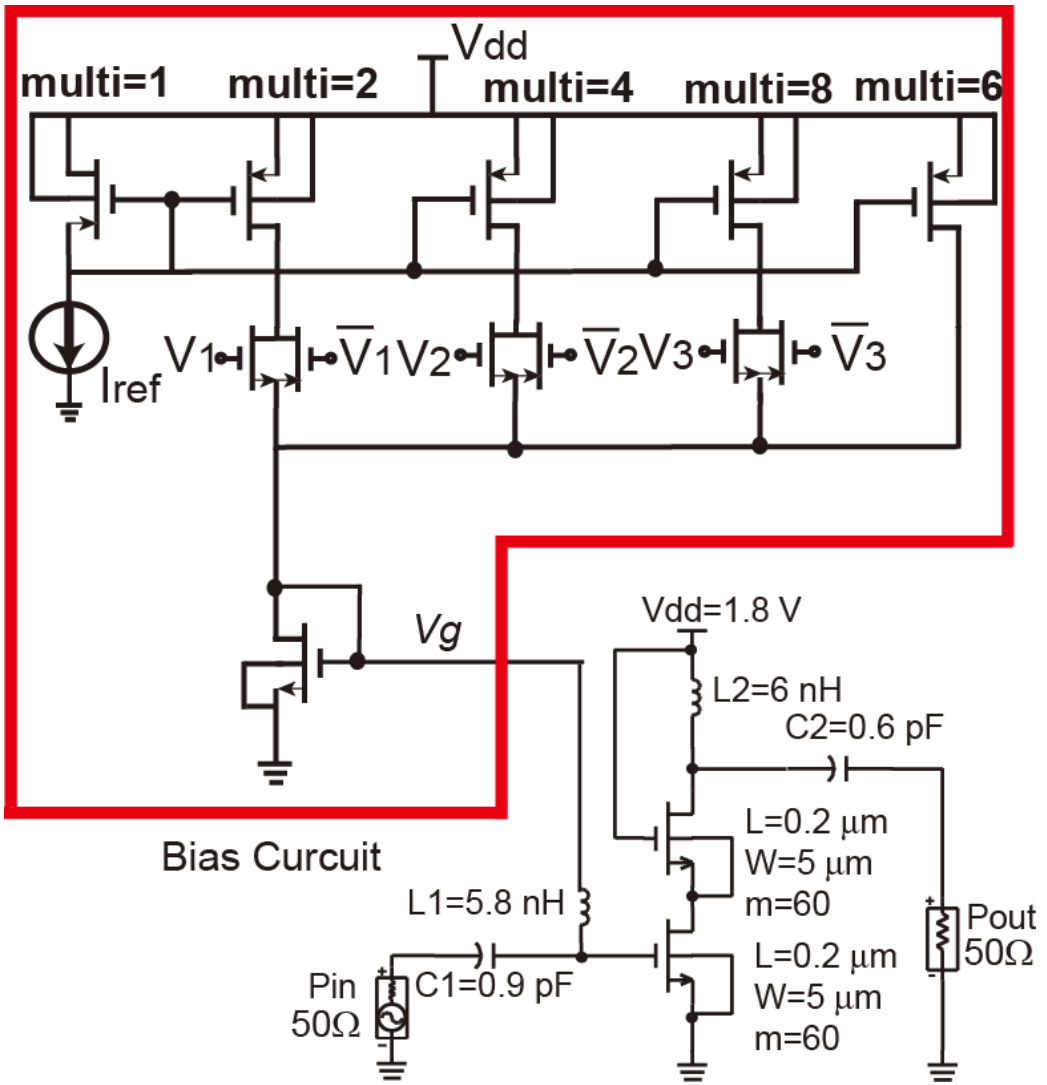
Proposed design

・LNA and Variable bias circuit for self compensation

・Controlling gate bias voltage Vg of input-stage transistor

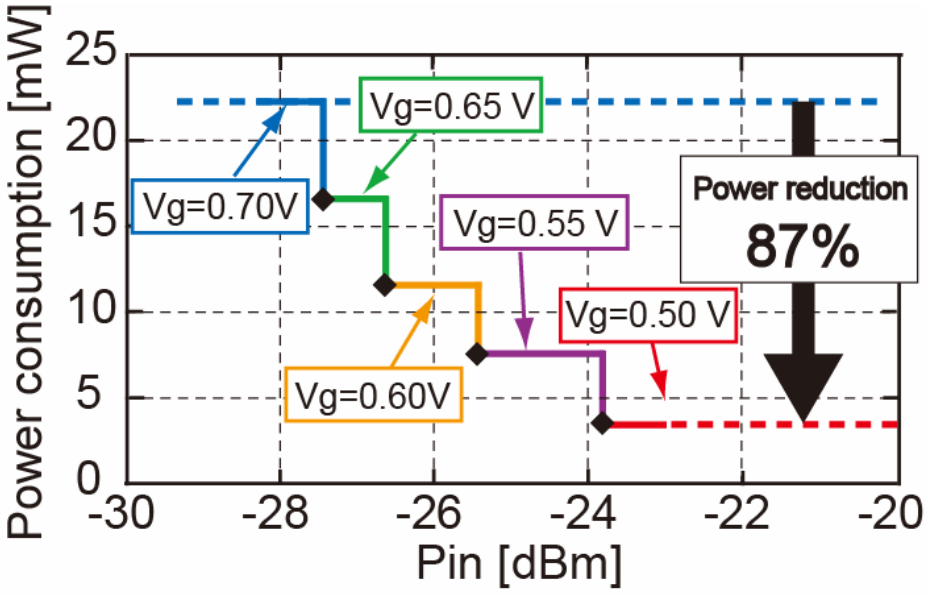
Supply current control (3bit)

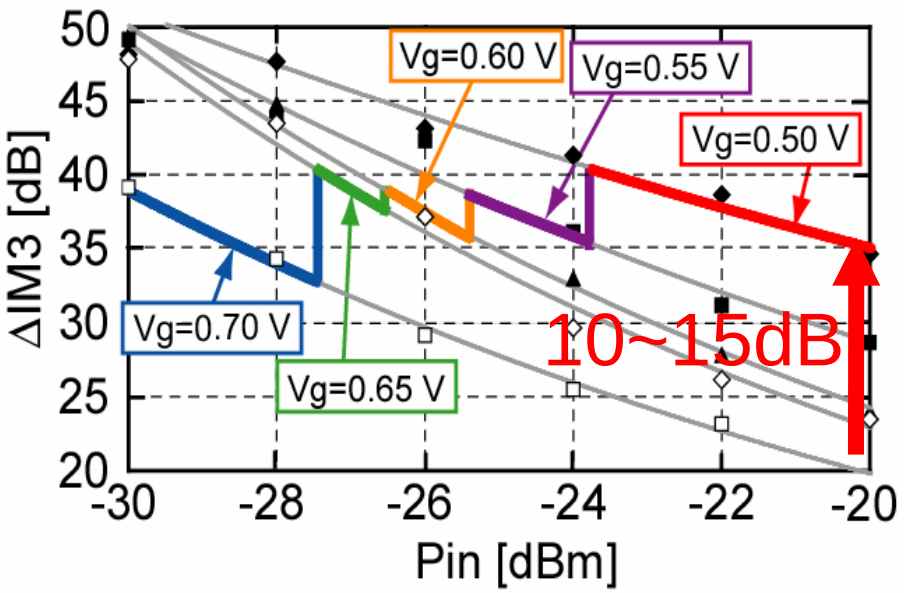
Simulated by ADS(Agilent)



5. Linearity and power consumption

Freq.=1.9GHz





Power consumption is reduced by 80%

Self compensation for linearity

Vgs is decreased.

6. Summary and conclusion

We proposed self compensation technique for LNA.

Bias voltage of the LNA is tuned

Self compensation technique is evaluated by measurement.

- Measured results
  - Linearity (ΔIM3) ΔIM3 is improved by over 10dB
  - Power consumption Dynamic power reduction (87%)

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