Application Specific Network-on-Chip Design with Guaranteed Quality Approximation Algorithms

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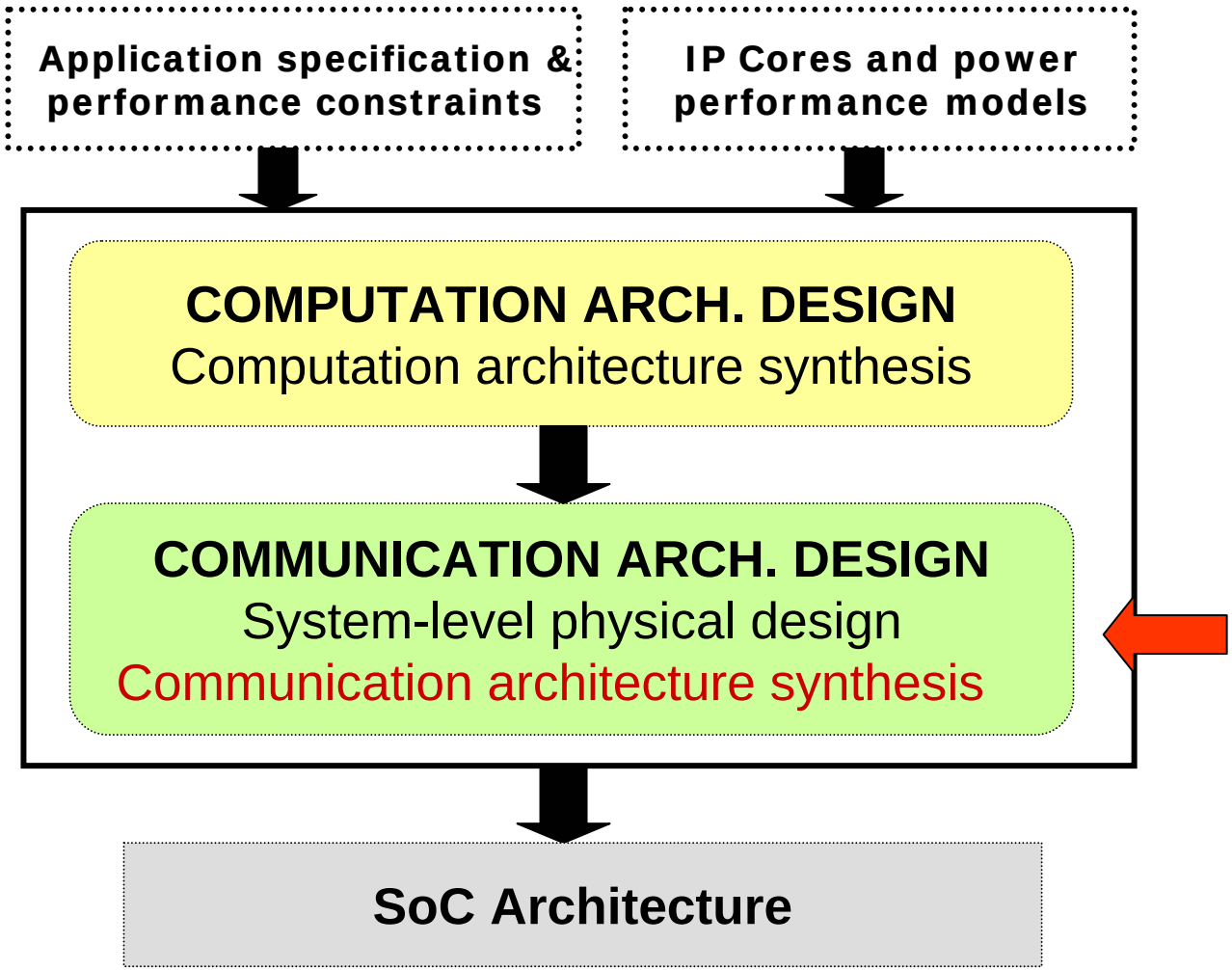
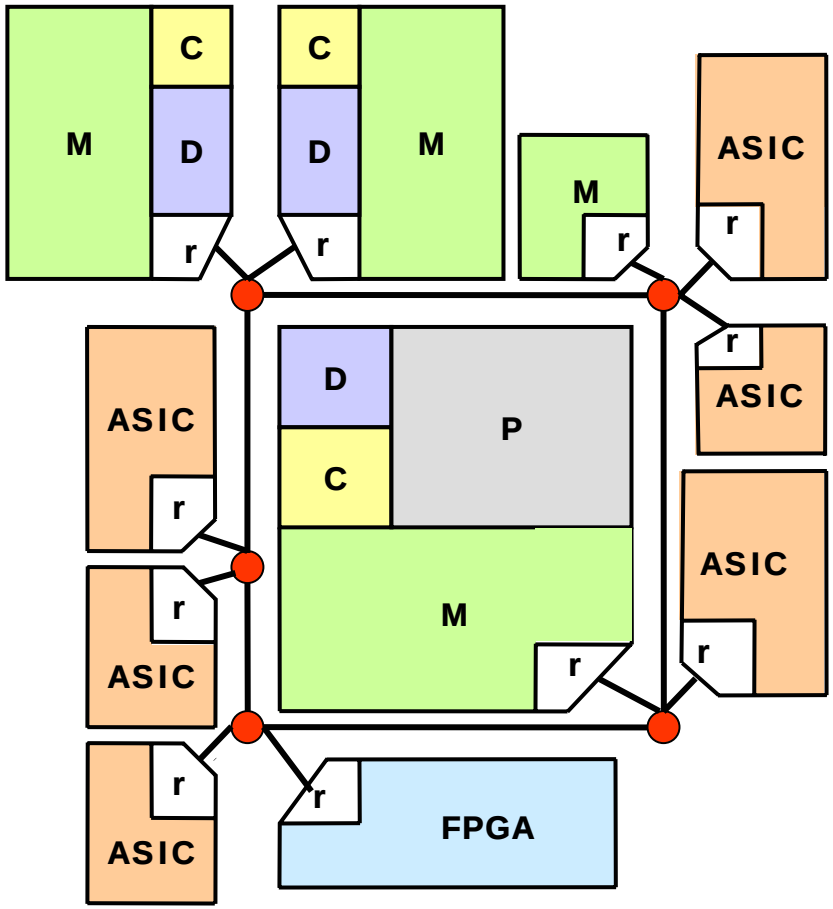
Network-on-Chip (NoC)

- Solution to global communication challenges
- Packet switching based asynchronous communication
- Inherently scalable
- Supports high bandwidth
  - Distribution of signal delay among routers
  - Isolation and support of concurrent communication

Application specific SoC design flow



SoC architecture with NoC



r = resource network interface

C = cache

P = processor

M = memory

D = DSP

= Routers

= Physical links

System-level NoC design issues

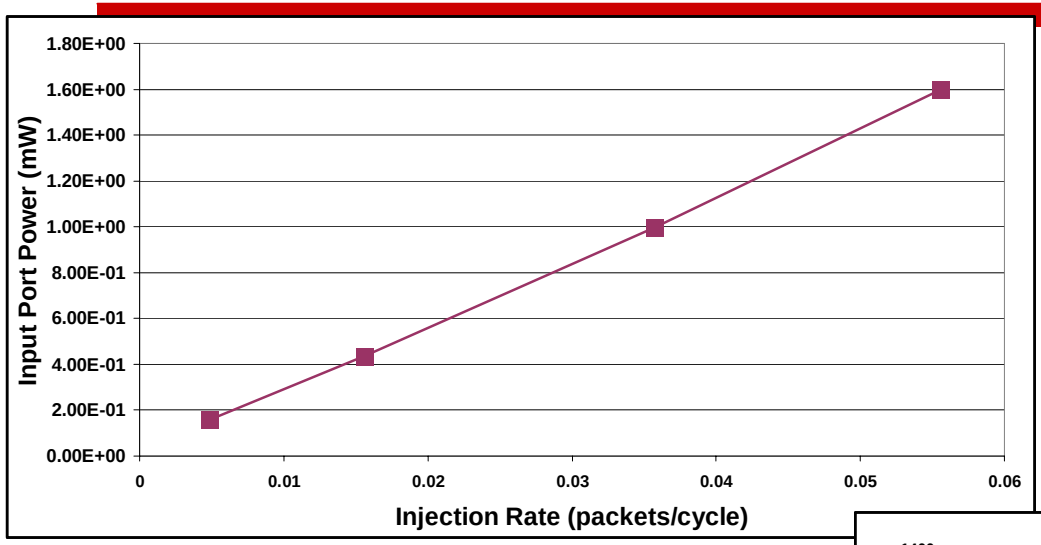
- NoC structure (or topology)
  - Regular versus custom topologies
- Low power and router consumption requirements
- Performance requirements

Regular versus custom topology

Regular Topologies	Custom Topologies
Mesh, Torus	Irregular topologies
General purpose SoC	Application specific SoC
Homogeneous routers	Heterogeneous routers
Reuse of topology	Design reuse of routers
Lower design time	Longer design time
Lower performance	Higher performance
Higher power	Lower power

- Focus of this work
  - Application specific SoC
    - Custom topologies
  - Power minimization is an important design goal
    - Minimize NoC power consumption subject to performance constraints

NoC power/performance characterization



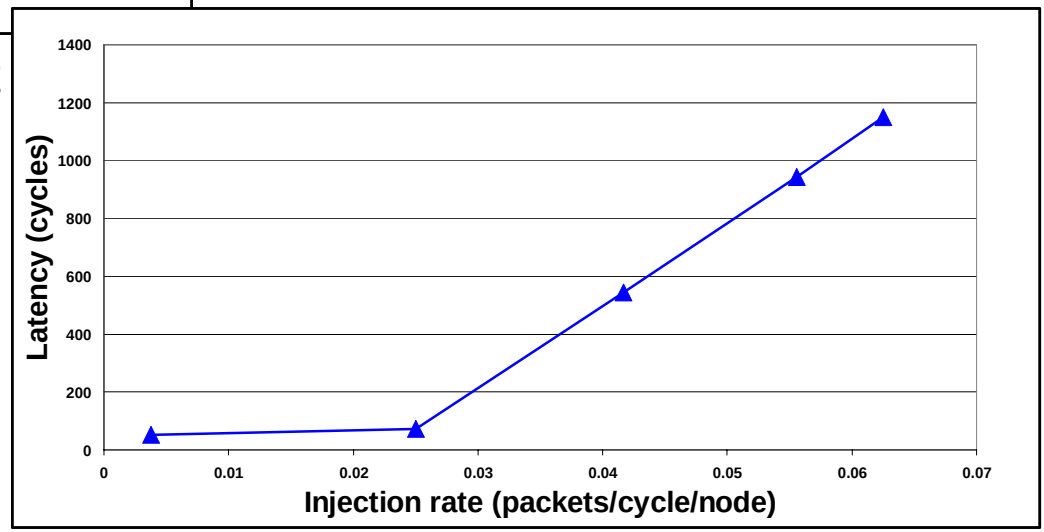
Power Consumption of an i/p port

$$\rho(input\ \ port) \propto bandwidth$$

$$\rho(output\ \ port) \propto bandwidth$$

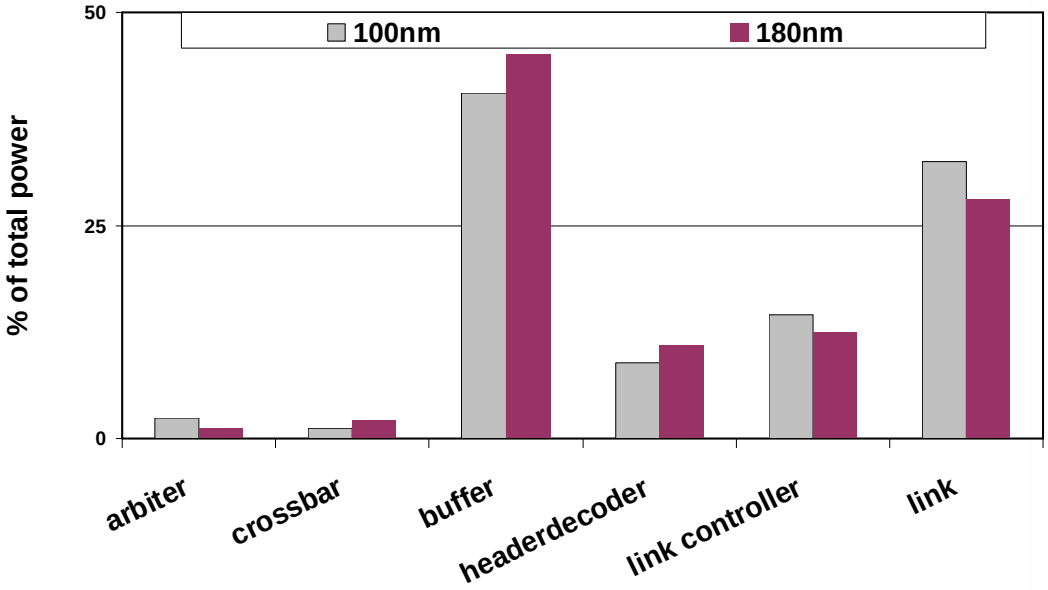
Network should be operated below the point of congestion.

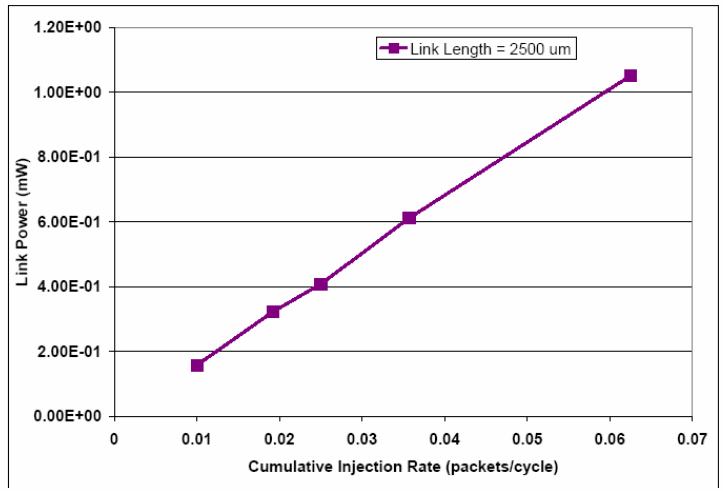
Impose bandwidth constraints on router ports

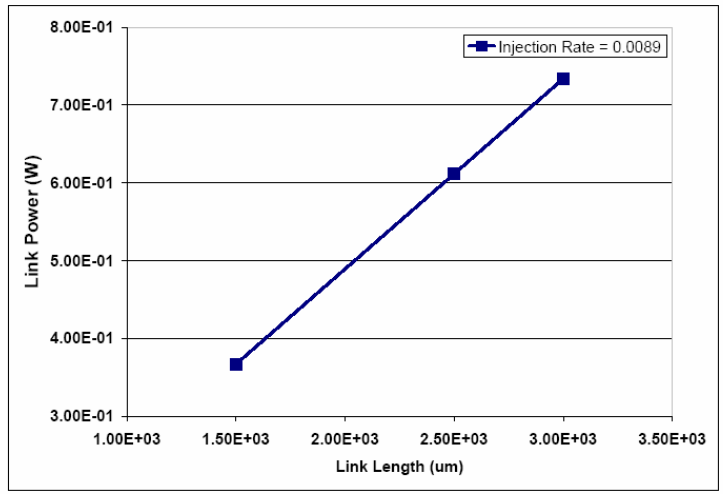


Average latency of 4x4 mesh NoC, XY routing, all processors are injecting

Power consumption in NoC physical links



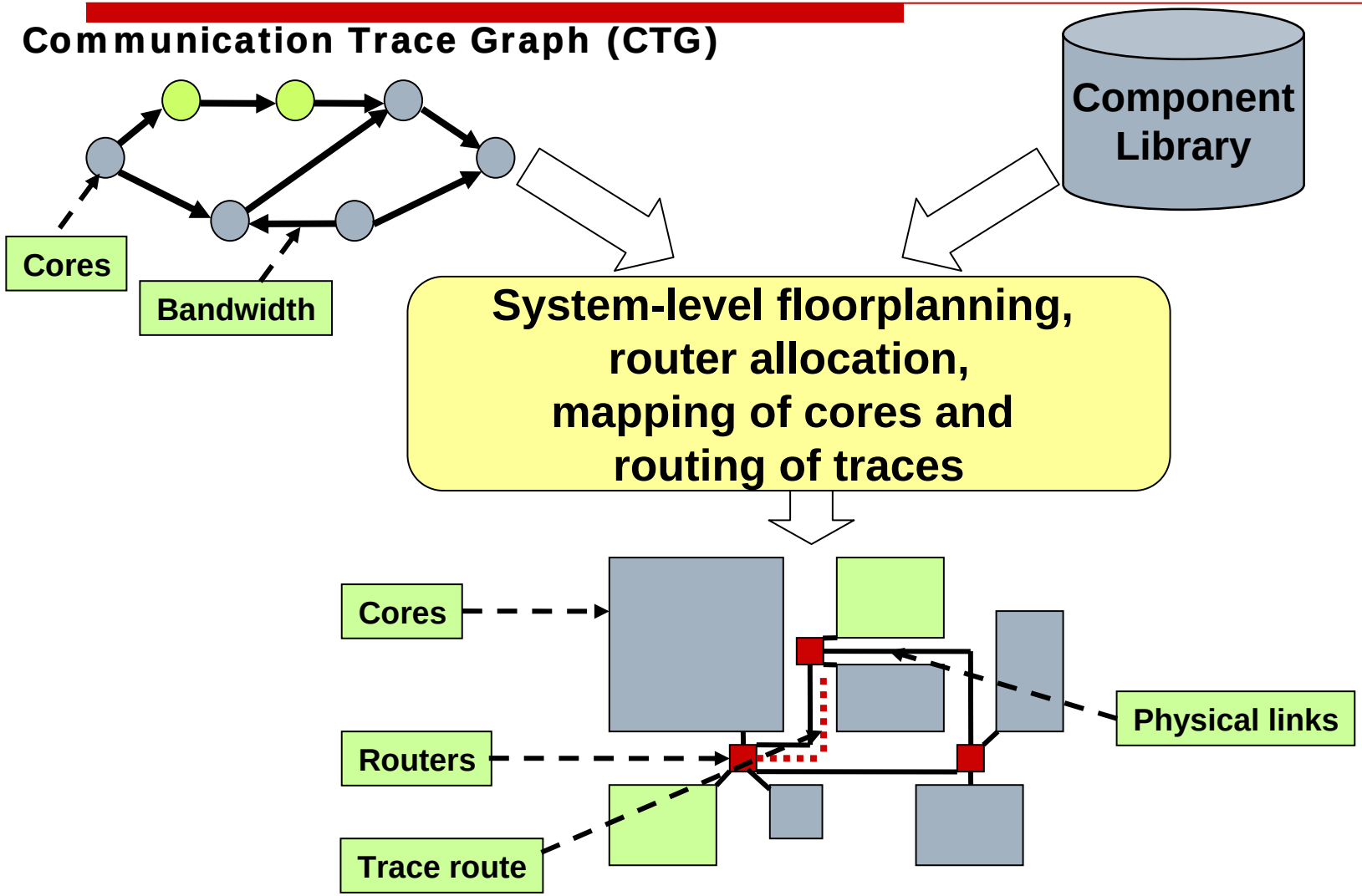




$$\rho(\textit{physical link}) \propto \textit{bandwidth}$$

$$\rho(\textit{physical link}) \propto \textit{link length}$$

Low Power Custom NoC Design



Problem definition

- Given
  - Communication Trace Graph (CTG) G(V,E)
  - Bandwidth requirements on communication traces
  - Physical dimensions of cores
  - Power and performance characterization of router ports and physical links
  - Maximum inter-router and core-router distance to ensure single clock cycle data transfer
- Objective
  - System-level floorplan
  - Topology of NoC with core mapping
  - Generate a route for each trace
- Such that
  - Communication power is minimized subject to performance constraints on CTG and bandwidth constraints on routers

NoC : Related work

- Automated design techniques for regular architectures
  - Hu et al (ASPDAC 03)
    - Branch and Bound technique
  - Murali et al (DATE 04)
    - Iterative mapping and routing
  - Srinivasan et al (ISLPED 05)
    - Slicing tree based recursive partitioning
    - Lower complexity than existing heuristics, and high solution quality
  - Srinivasan et al (CODES 06)
    - Layout aware mesh based NoC design
    - Layer based mapping of cores to infer logical mesh from floorplan

- Automated design techniques for application specific architectures
  - Srinivasan et al.
    - ICCD 04, ISQED 06, TVLSI : Integer linear programming
    - ICCAD 05 : Integer relaxation and quadratic programming
    - ASPDAC 07 : Approximation algorithms
    - DATE 06 : Low complexity heuristics
    - VLSI 05 : Genetic algorithm based technique
  - Ogras et al (DATE 05, ICCAD 05)
    - Heuristics based on graph decomposition, and long range link insertions

Approximation algorithm for NoC design

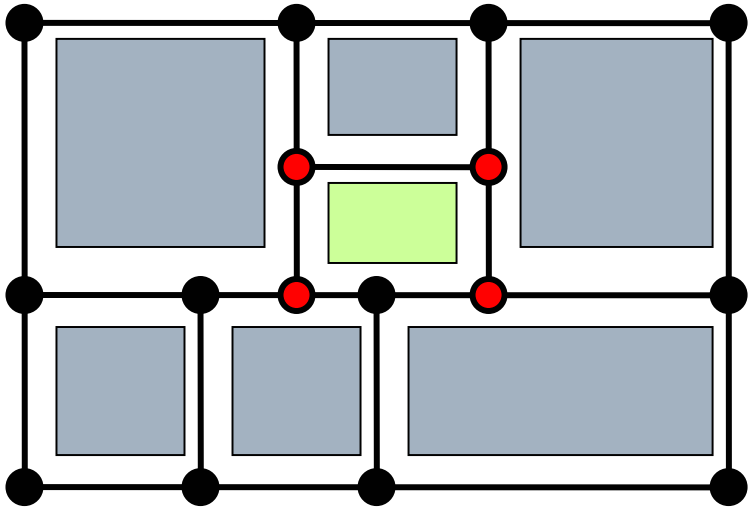
- 3 stage approach
  - Linear programming approximations for Stages 2 and 3
- Stage 1: System-level floorplanning

$$Minimize \sum w_{i,j} \times d_{i,j} + \alpha \times area$$

- Stage 2: Allocation of routers and mapping of cores
  - Objective: minimize power
- Stage 3: Route and topology generation
  - Objective: minimize number of routers
  - Subject to shortest paths and router bandwidth constraints

Custom NoC topology Stage 2: Router allocation and core mapping

- Dimensions of routers << cores
  - Router locations: nodes of channel intersection graph



- Core mapped to one router at its four corners
  - Objective function

$$\sum_{\forall (i,k) \in E} \omega(i,k) \times dist(r_i, r_k)$$

Custom NoC topology Stage 2: Core mapping

- Problem formulation
  - Let $X_{i,j,k,l}$ denote
    - core “i” is assigned to router “j” and
    - core “k” is assigned to router “l”
  - Let $A_{i,j,k,l}$ denote corresponding power consumption

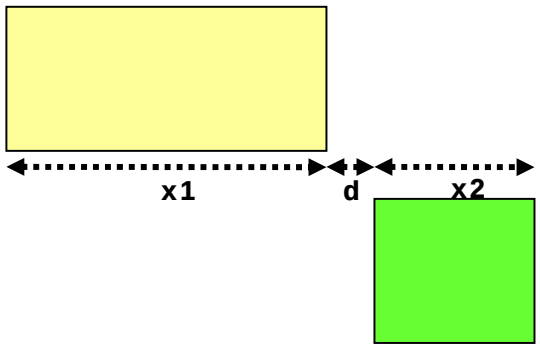
$$A_{i,j,k,l} = X_{i,j,k,l} \times \omega(i,k) \times dist(j,l)$$

$$dist(j,l) = dist_x(j,l) + dist_y(j,l)$$

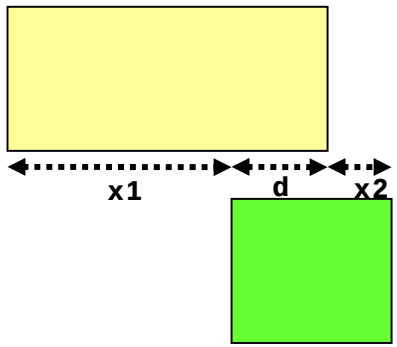
$$A(i,j,k,l) = X_{i,j,k,l} \times \omega(i,k) \times dist_x(j,l) + X_{i,j,k,l} \times \omega(i,k) \times dist_y(j,l)$$

  - Divide problem into X-offset and Y-offset
    - X-offset determines the X-coordinate of the router
    - Y offset determines the Y-coordinate of the router

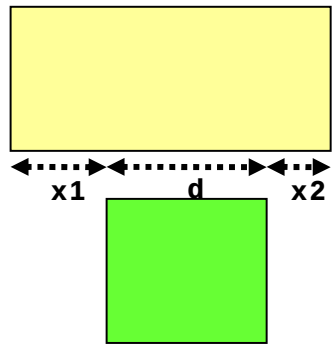
Proof of optimality



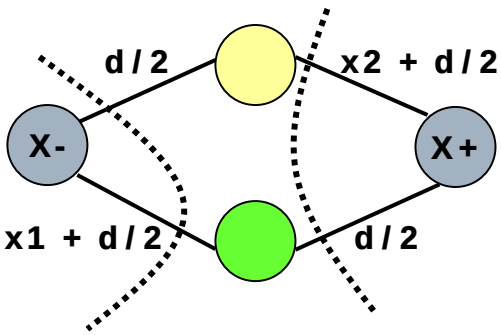
Two cores do not overlap

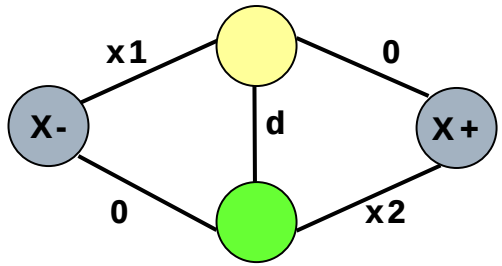


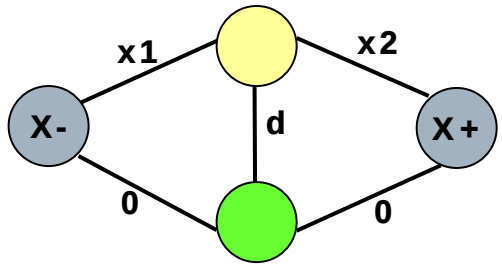
Two cores partially overlap



Two cores fully overlap



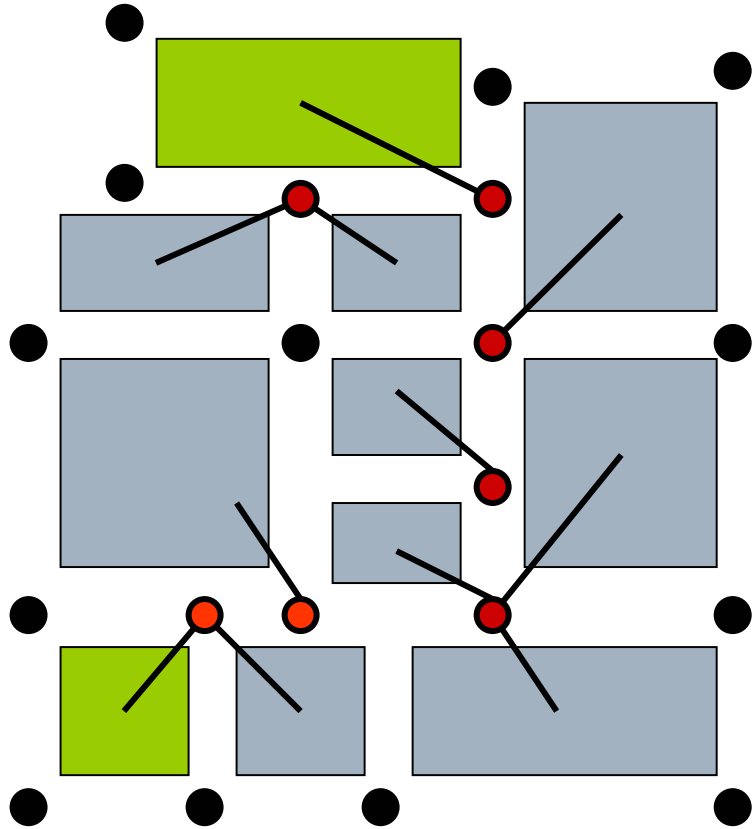




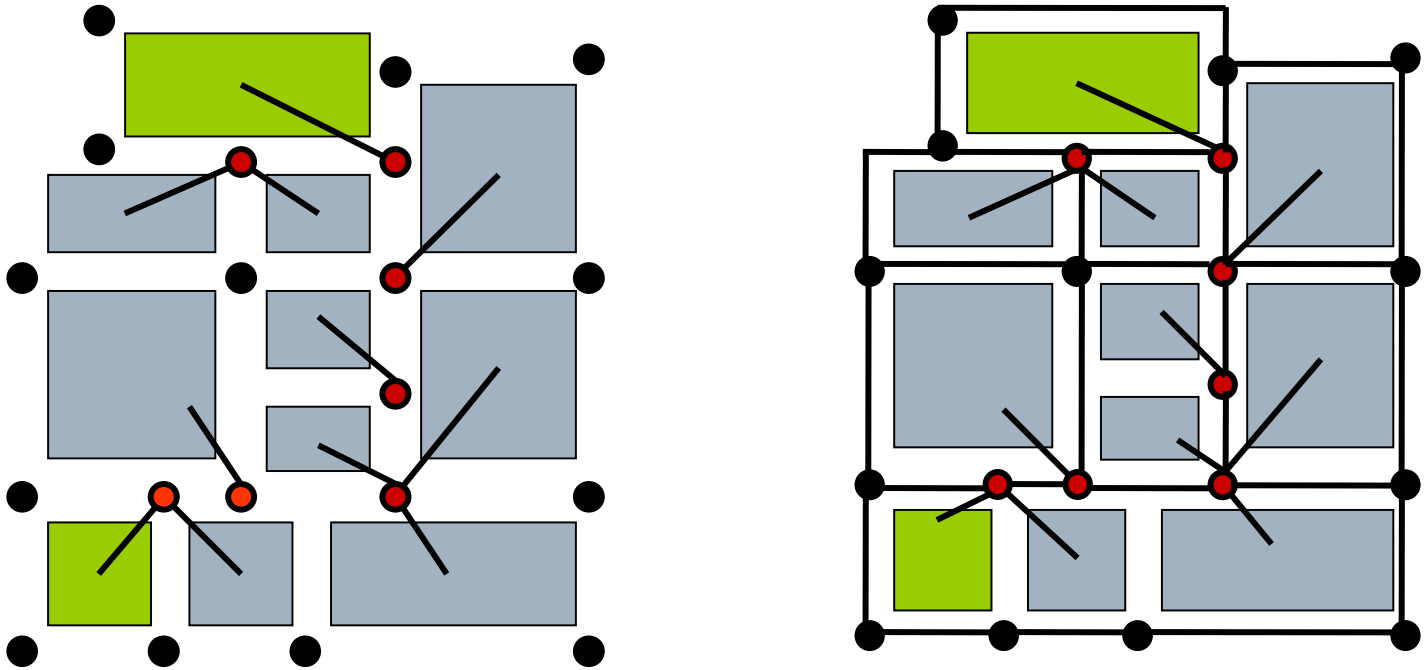
- Solve each part by reducing it to a max-flow min cut problem
  - Push relabel algorithm : $O(n^3)$

Custom NoC topology Stage 3: Topology design and route generation

- Generate a route such that
  - Topology utilizes minimum number of routers.
  - Subject to shortest path routes for the traces
- Similar to Generalized Steiner Forest problem
- Formulate it as an ILP
  - Objective is to minimize routers
  - Solve LP relaxation
  - Utilize iterative rounding

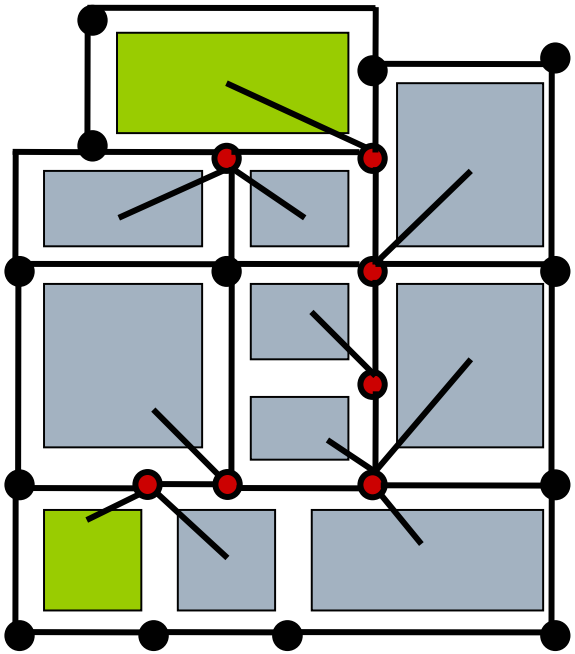


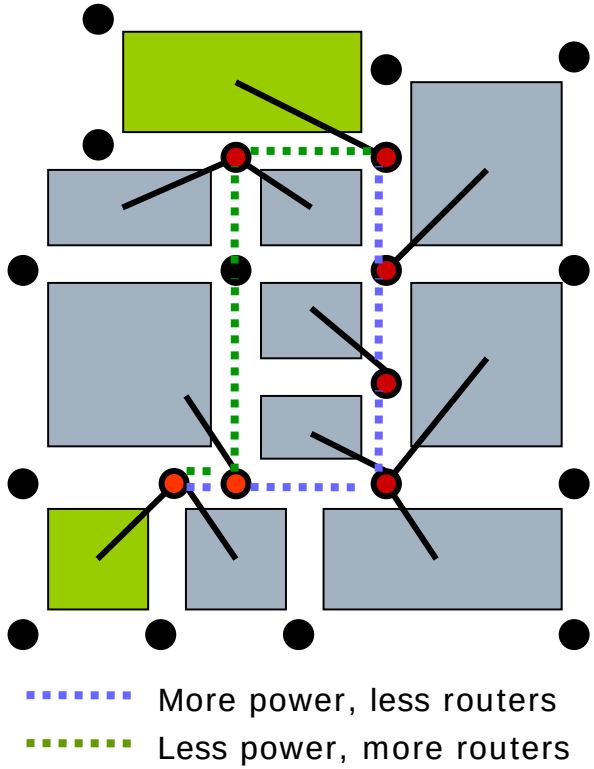
Stage-3: Input to the ILP



- Input to the ILP is a graph G_r where
  - Node set : cores and routers
  - Edge set :
    - Edge between two routers if Manhattan distance is less than designer specified distance between the routers
    - Edge between the core and the router mapping the core

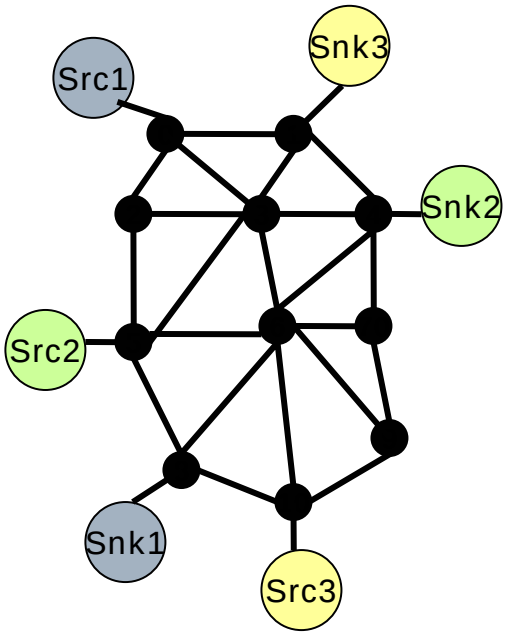
Stage-3: Fewer routers versus lesser power consumption

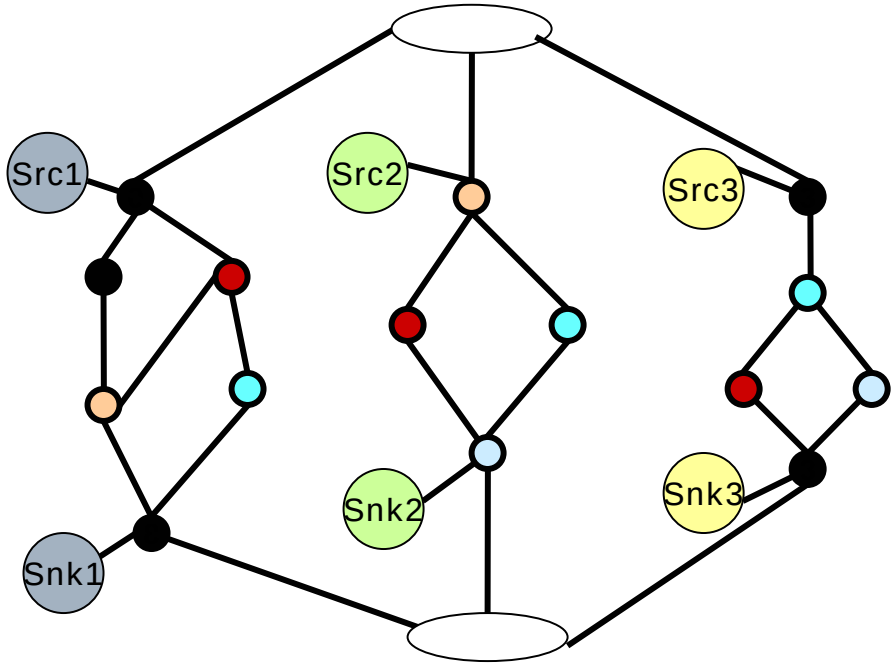




- Invoking the ILP on G_r may result in non-shortest paths for some traces

Stage-3: Graph transformation for router minimization subject to least power consumption





- Generate shortest path trees for all traces
  - Edge weight = Router power per Mbps + Link power per Mbps * length
- Add source and sink to generate transformed graph
- Invoke ILP on transformed graph

Custom NoC topology Stage 3: Topology design and route generation

- Formulate a cut based ILP formulation
  - Formulation based on number of edges crossing each cut in the graph
- Theorem: Cut based formulation generates a 2-approximation
- Cut based formulation has exponential number of inputs

Custom NoC topology Stage 3: Topology design and route generation

- Formulate flow based LP
  - Formulation based on network flow
- Theorem: Cut based and flow based LP are equivalent
- Conclusion: Flow based LP with iterative rounding generates a 2-approximation solution
  - All traces consume minimum power
  - Number of routers is no more than twice optimal

Experimental Results

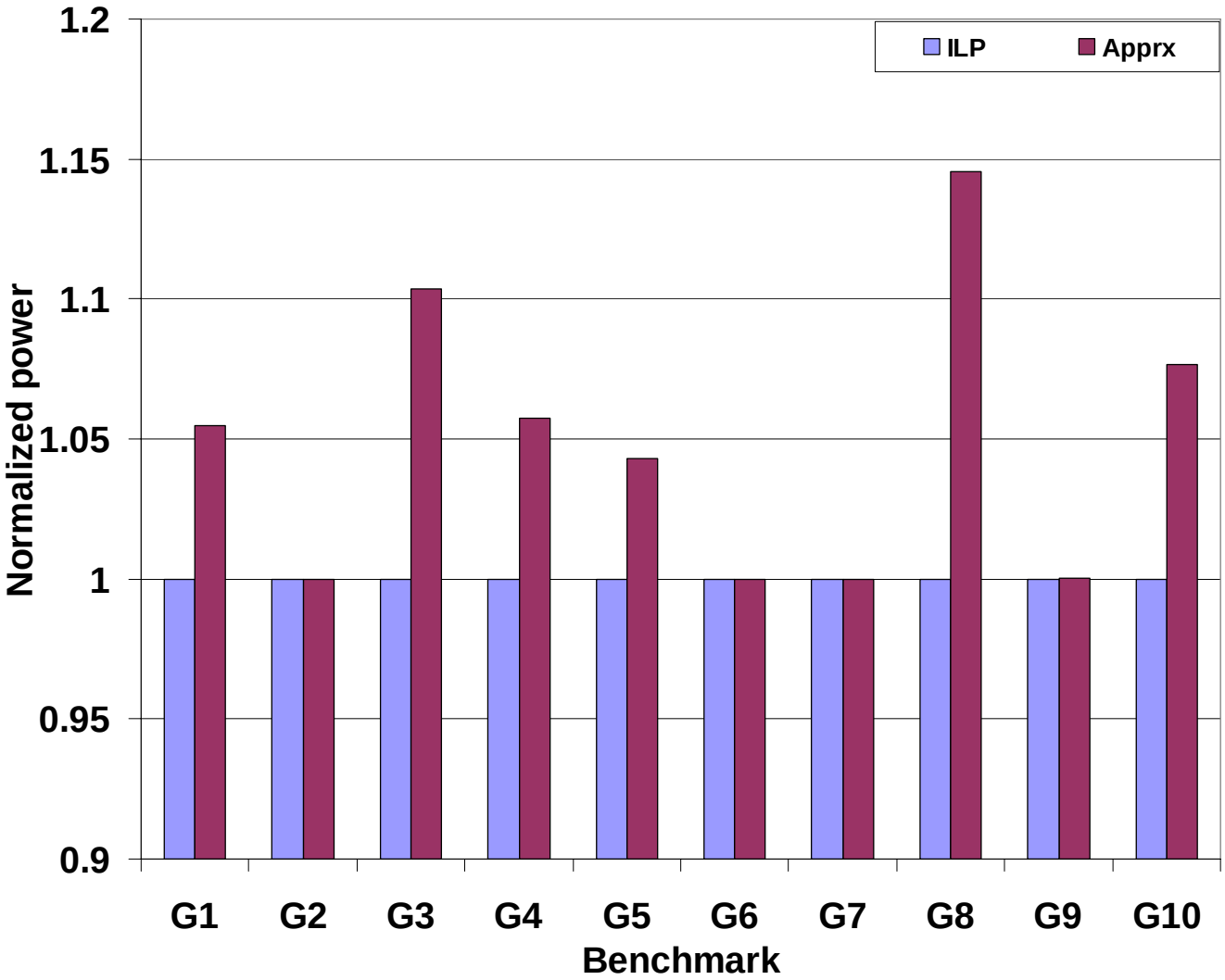
- Several multimedia and network processing benchmarks
  - Jalabert et al. (MPEG-4, VOPD, MWD)
  - Hu et al. (Set-top box)
  - Pasricha et al. (Network Processing)
  - Ramamurthi et al. (Diffserv, IPV4)
  - Srinivasan et al. (JPEG encoder)

- Benchmark sizes
  - Smallest benchmark
    - Diffserv
    - 9 nodes, and 8 edges
  - Largest benchmark
    - Network processing
    - 24 nodes, and 42 edges

Experimental results

- XPress-MP solver for ILP formulations
- Power model
  - 65 nm TSMC low power library
  - Input port power of 204 nW/Mbps
  - Output port power of 94 nW/Mbps
  - Link power of 89 nW/Mbps
- Benchmark sizes
  - 3x3 mm^2 for ARM core
  - Other cores varied from 0.5 mm^2 to 25 mm^2
  - Maximum distance of 6mm between routers
  - Router area of 0.37 mm^2
    - FIFO depth 16, Virtual channels 2, Width 32, 9 ports
- Parquet floorplanner to obtain SoC layout

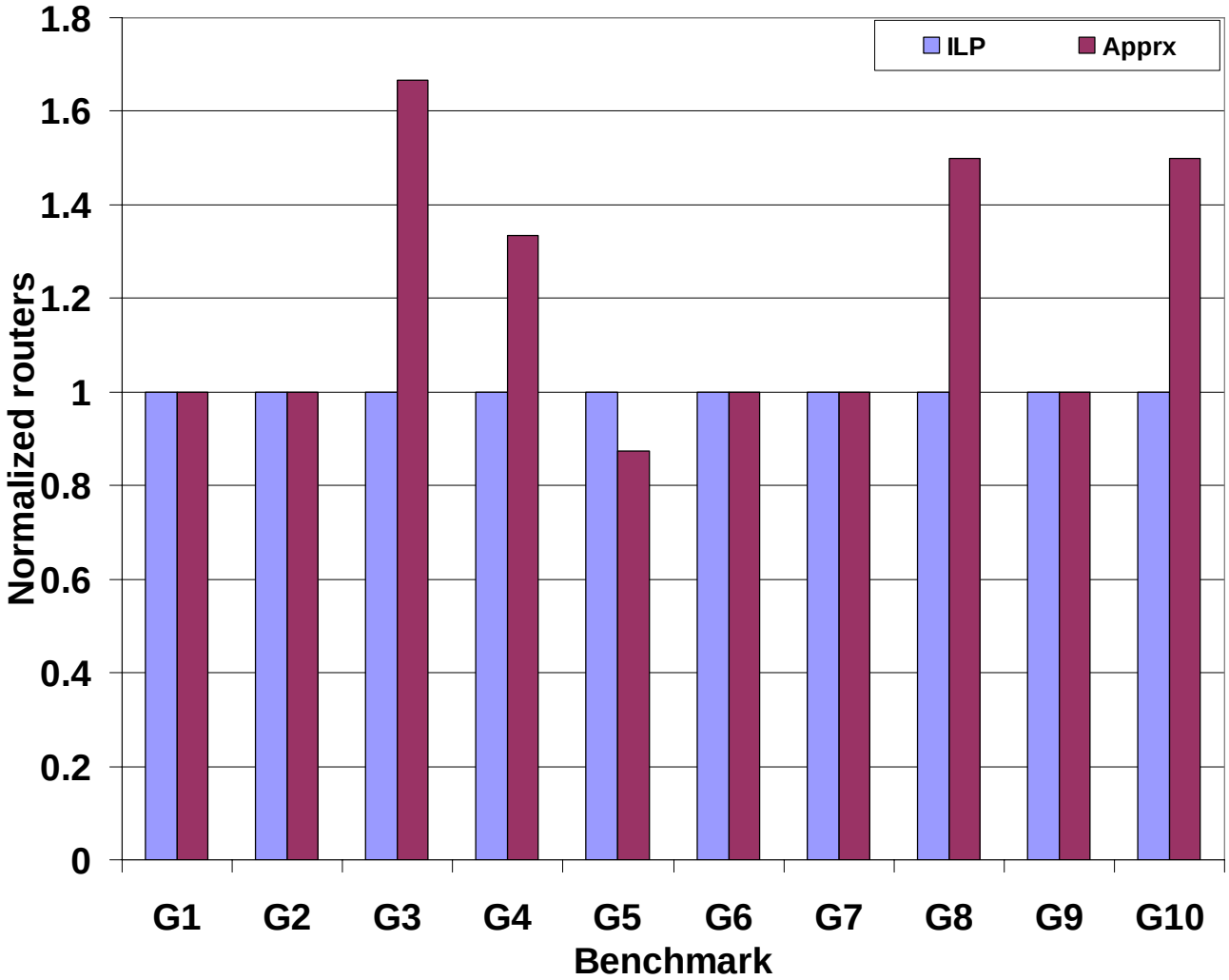
Power comparison with ILP



1.04 times power

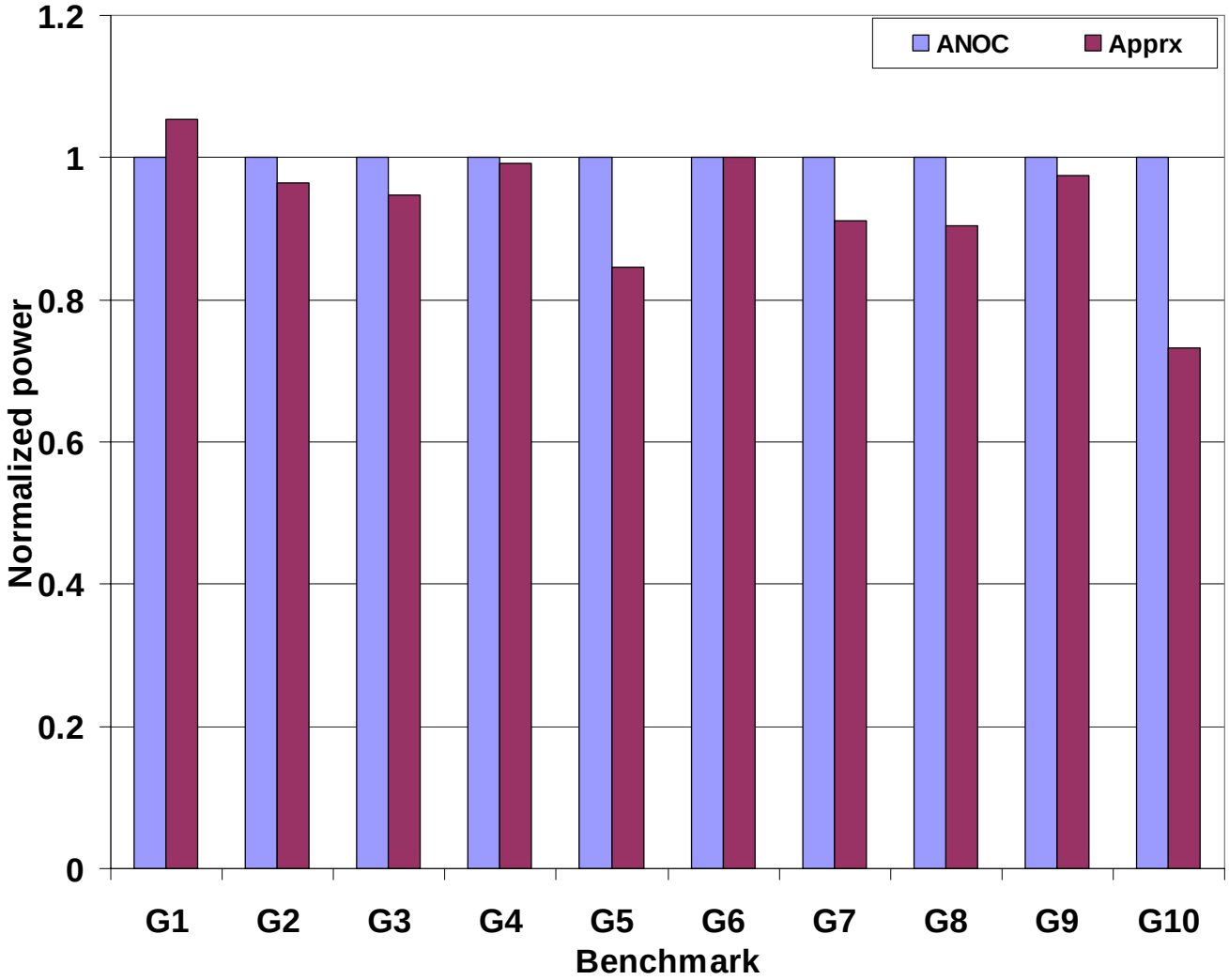
Negligible runtime

Router comparison with ILP



1.1 times the number of routers

Power comparison with ANOC:

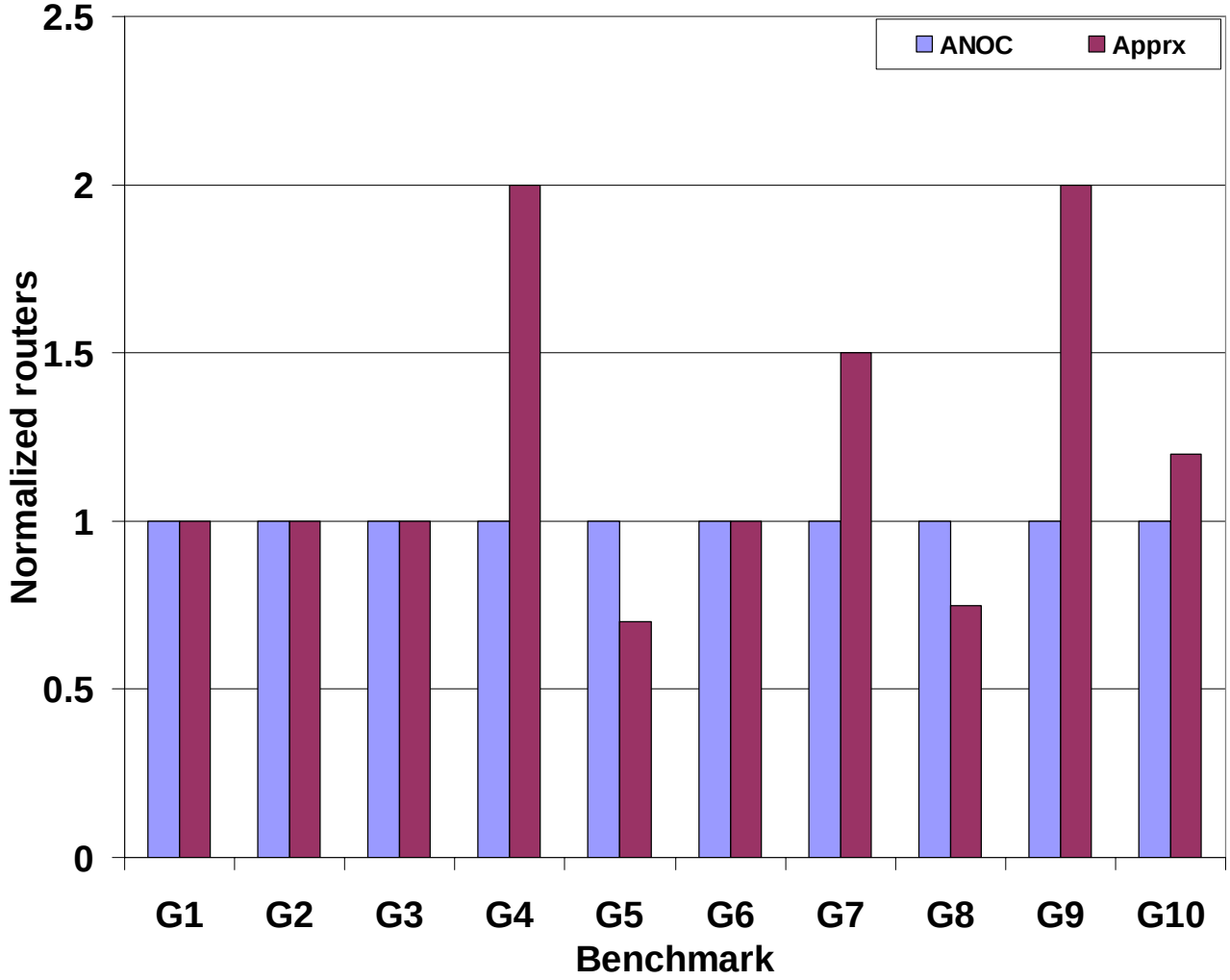


0.9 times power

Lower power for 9 out of 10 benchmarks

Comparable runtime

Router comparison with ANOC:



1.2 times the number of routers

Technique trades-off routers for lower power consumption

Generates router efficient solutions in the absence of low power requirements

Conclusions and Future work

- Conclusions
  - Defined and formulated the application specific NoC design problem
  - Presented an automated technique for application specific NoC design
  - Demonstrated the quality of the technique with comparisons with optimal technique, and existing heuristics

- Future work
  - Exploit advantages of FIFOs, buses and NoC
  - NoC design to minimize thermal hotspots
  - NoC reconfiguration for fault tolerance