DFM reality in Sub-Nanometer IC Design

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Move from ideal-GDSII to Model based Silicon Accurate Design
Outline of DFM reality in Sub-Nanometer IC Design

- 65nm Technology Trends
- Addressing 65nm Challenges during Design
- Summary
Sub-Nanometer Failures Cause Systematic Yield Loss

Systematic Yield is now Dominant

What you design is NOT what you print on Silicon

- DRC is not sufficient anymore
- Risk costly respins or poor utilization of process
- Need to design tools to prevent catastrophic systematic failures

Catastrophic Failures Impact Yield
Sub-Nanometer Failures Cause Parametric Yield Loss

- Increased sensitivity to manufacturing variations on both devices and interconnect
- Current design flows based on ideal GDSII, margins and rules translates in large margins, over-design and long timing closure or undetected parametric failures
Context dependent Variability cannot be Addressed by Rules and Margins

13% delay variation due to context

Top and bottom context impacts transistor CD!

2X leakage variation due to context

Courtesy of a leading foundry, a Clear Shape partner
Traditional ideal-GDSII based design methodology is failing....

Designers need to move from ideal GDSII to contour-based design tools to predict nanometer silicon behavior

- Si-accuracy requires upfront FAB validation
- Must work with traditional design flows
- Library, IP, and Full-chip level
- Runtime in hours for full-chip
- Manufacturing/OPC TOOL independent
- Address both catastrophic and parametric yield issues
Design Infrastructure Evolution to Predict Mfg. Variations and their Impact on the Design

Rule based infrastructure: DRC, LPE, Extraction
Model: SPICE, Silicon Contours Models

Silicon-accurate Timing-Leakage
Model-based Design Manufacturability Checker (DMC)

Silicon Contour Models (+ CMP Model)

Predict and reduce parametric failures due to variations to increase parametric yield
Predict and reduce systematic catastrophic variations to increase functional yield

Design for Variability Platform

Robust designs
Manufacturable layout
Reduced cycle
Reduced Spread
Improved perf.
Increased yield
Disruptive Technology to Improve Yield without Disrupting Design Flows

Rule based infrastructure: DRC, LPE, Extraction
Model: SPICE, **Silicon Contour Models**

<table>
<thead>
<tr>
<th>Custom Layout</th>
<th>Tx. Xtraction</th>
<th>RC Xtraction</th>
<th>SPICE</th>
<th>Timing</th>
<th>SI</th>
<th>Power</th>
<th>Place &amp; Route</th>
<th>Phys Ver. (DRC)</th>
</tr>
</thead>
</table>

Silicon-accurate Timing-Leakage

Model-based Design Manufacturability Checker (DMC)

Silicon Contour Models (+ CMP Model)

Design for Variability Platform

- RET
- OPC
- Mask
- CMP
- Etch
- Silicon
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Contour Prediction Models Enable Physical and Electrical DFM Closure during Design

Designers use Silicon Contour models to:
- Predict catastrophic shapes variations (hotspots)
- Predict timing and power failures due to mfg. variations

Models for Designers

Manufacturing Post-GDSII RET/OPC Flow
- Design Layout
- Retargeted Layout
- Biased Layout
- RETEd Layout
- Mask Layout
- Litho Model
- Silicon Contours across Process window

Design
- Silicon Contour Models
- 193nm Copper

Silicon Contour Models
- e.g. TSMC DDK
- Silicon Contours Across PW
- Hotspots

Parametric variations
Contour-based Extraction Delivers Silicon-Accurate Parametric Analysis

Si-Contour Based Device Extraction

Si-Contour-based Device parameters
- $W_{eq}$, $L_{eq}$
- $\Delta AS$, $\Delta PS$, $\Delta AD$, $\Delta PD$

Si-Contour Based Interconnect Extraction*

Si-Contour-based parasitics
- $\Delta R$, $\Delta C$

*includes CMP thickness variation
Silicon Validation of Contour-based Device Modeling

- Generate Contour for Poly flaring structures
- Compared current predicted with contour-based device model and silicon measurement
- Must take into account electrical behavior of sub-nanometer transistors

Courtesy of a 65nm major semiconductor vendor, Clear Shape partner

Predicted silicon within 2%
Silicon-Proven Device Modeling

Courtesy of a 65nm major semiconductor vendor, Clear Shape partner

Prediction within 2.5% of Silicon
Contour-based Analysis Detects and Reduces Catastrophic Systematic & Parametric Variations

SPICE Netlist with In-Context Variations (AROW) → Fixing ECO constraints set_max_delay → Incremental SDF with in-context Δt → DMC Violations → Fixing Guidelines → Contours → Contour-based Timing → Custom Flow Extract → SPICE Simulator → P&R Extract → STA

25% W variation

Clear Shape Results

Predict & reduce systematic catastrophic variations to increase functional yield

Predict & reduce parametric failures due to variations to increase parametric yield

Silicon Results

Silicon showed a systematic functional failure

26% longer hold time

w/ Variations

Ideal
Outline

◆ 65nm Technology Trends
◆ Addressing 65nm Challenges during Design
◆ Summary
Designers Need Universal Solutions to Address Systematic and Parametric Failures

Contour-based Design Manufacturability Checker
- Need fast and accurate hotspot detection and contour prediction
  - Full-chip, blocks or cells - in hours!
- Easy to use with DRC-like use-model
- Endorsed by foundries and fabs
- OPC-tool independent

Contour-based Variability Analysis
- Predict impact of device and interconnect variations during design
- Silicon-proven device modeling
- Remove margins
- Accelerate timing closure
- Better Yield

Work with an Fab and Fit into any existing design flows
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