A Processor Generation Method from Instruction Behavior Description Based on Specification of Pipeline Stages and Functional Units

Takeshi Shiro, Masaaki Abe, Keishi Sakanushi, Yoshinori Takeuchi, and Masaharu Imai

Graduate School of Information Science and Technology, Osaka University, Japan
Outline

- Background
- Proposed Processor Generation Method
- Experiments
- Conclusion
Background

- **Application-Specific Instruction set Processors (ASIPs)**
  - More flexible than ASICs
  - Higher performance than general purpose processors

- **Design Space Exploration (DSE)**
  - Explore and evaluate various architectures
  - **Requirements**
    - Design and modify various processors within a limited time
    - Compilers, assemblers, and simulators are demanded

---

Processor Design Environment is proposed
Design Flow of Processor Design Environment

1. Architecture parameter Definition
2. Instruction Set Definition
3. Semantics Definition
4. Operation Definition

- SW Development Tools
- HDL of a Processor
- Not Satisfy
- Satisfy?
- Satisfy
- Optimal Processor

Satisfy?
Semantics Definition and Operation Definition

- Semantics Definition
  - For software development tools
  - Defined by behavior description
    - Not specify pipeline stages and functional units
- Operation Definition
  - For HDL description
  - Defined by micro-operation description
    - Specify pipeline stages and functional units

Behavior Description of Instruction ADD

\[
GPR[rd] = GPR[rs0] + GPR[rs1];
\]

Micro-Operation Description of Instruction ADD

Stage1:  
\[
current\_pc = PC.read();
\]
\[
\text{Name} = \text{IMEM.read}(current\_pc);
\]
\[
\text{IR.write}(\text{Name});
\]
\[
PC.inc();
\]
Stage2:  
\[
\text{source0} = GPR.read0(rs0);
\]
\[
\text{source1} = GPR.read1(rs1);
\]
Stage3:  
\[
\text{result} = \text{ALU.add(source0,source1)};
\]
Stage4:  
Stage5:  
\[
GPR.write0(rd,\text{result});
\]
Problems and Solutions

- Problems
  - Describing micro-operation description takes up half of processor design time
    - Code size of micro-operation description is more than that of behavior description
  - Consistency between two descriptions is required
    - Human error may be occur

→ Instructions should be defined by only one description

Generate micro-operation description from behavior description
Outline

- Background
- Proposed Processor Generation Method
- Experiments
- Conclusion
Generation Flow of the Proposed Method

1. Construct Abstract Syntax Trees (ASTs) from the behavior description
2. Generate micro-operation fragments
   - Micro-operation descriptions without specification of pipeline stages and functional units
3. Allocate the micro-operation fragments to the pipeline stages.
4. Define a functional unit for each micro-operation fragment
Assumption

- The behavior description must be complemented with the following information:
  - Allocating micro-operation fragments to pipeline stages
  - Binding functional units to micro-operation fragments
- Give attribute to each pipeline stage
  - execution, memory read, etc.
- Define only one functional unit for a certain function
Construction of Abstract Syntax Trees (ASTs)

- Parse behavior description, and construct AST

Instruction ADD

\[ \text{GPR}[\text{rd}] = \text{GPR}[\text{rs0}] + \text{GPR}[\text{rs1}] \]
Generation of Micro-Operation fragments

- Micro-operation fragments
  - Micro-operation description without specification of pipeline stages and functional units
  - \(\text{result} = \$\text{temp}.\text{add}(\text{source0,source1});\)

- Generate micro-operation fragments by scanning generated ASTs

- Generate micro-operation fragments of operator nodes
  - Functional units are not decided yet
  - Only functions are decided
    - add, addu, mul, etc…
Example of Generating Micro-Operation fragments

Instruction ADD
\[ \text{GPR}[rd] = \text{GPR}[rs0] + \text{GPR}[rs1]; \]

source0 = GPR.read0(rs0);
source1 = GPR.read1(rs1);
source2 = \$temp.add(source0, source1);
GPR.write0(rd, source2);
Allocation to Pipeline Stages

- Allocate each micro-operation fragment to pipeline stage
- Attribute of each stage
  - Given in architecture definition step by a designer
### Attribute of Pipeline Stages

- **Attribute**
  - Instruction fetch, execution, memory read, etc...

<table>
<thead>
<tr>
<th>Stage Name</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stage1</td>
<td>Instruction Fetch</td>
</tr>
<tr>
<td>Stage2</td>
<td>Operand Fetch &amp; Sign-Extension</td>
</tr>
<tr>
<td>Stage3</td>
<td>Execution &amp; Jump</td>
</tr>
<tr>
<td>Stage4</td>
<td>Memory Read &amp; Memory Write</td>
</tr>
<tr>
<td>Stage5</td>
<td>Write Back</td>
</tr>
</tbody>
</table>
Example of Allocating to Pipeline Stages

- Attribute of each pipeline stage
  - Operand Fetch (read0, read1, ..) → stage2
  - Execution (add, sub, ..) → stage3
  - Memory Access (load, store, ..) → stage4
  - Write Back (write0, ..) → stage5

**Instruction ADD**

<table>
<thead>
<tr>
<th>Stage</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stage1</td>
<td>source0 = GPR.read0(rs0);</td>
</tr>
</tbody>
</table>
| Stage2 | source0 = GPR.read0(rs0);  
        | source1 = GPR.read1(rs1);  |
| Stage3 | source2 = $temp.add(source0, source1); |
| Stage4 | |
| Stage5 | GPR.write0(rd, source2); |
Bind Functional Units

- Bind Functional Units to Allocated Micro-operation fragments
  1. List all functions in generated micro-operation fragments
  2. Decide a functional unit for each function
  3. Bind decided functional unit to each micro-operation fragment
Example of Binding Functional Units

<table>
<thead>
<tr>
<th>instruction</th>
<th>operator</th>
<th>function</th>
<th>functional unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD</td>
<td>+</td>
<td>add</td>
<td>ALU</td>
</tr>
<tr>
<td>SUB</td>
<td>-</td>
<td>sub</td>
<td>ALU</td>
</tr>
<tr>
<td>MUL</td>
<td>*</td>
<td>mul</td>
<td>MUL</td>
</tr>
<tr>
<td>LSFT</td>
<td>&lt;&lt;</td>
<td>lsft</td>
<td>SFT</td>
</tr>
</tbody>
</table>

source2 = $\text{temp}.\text{add}(\text{source0},\text{source1});$

$\text{temp} \leftarrow \text{ALU}$

source2 = $\text{ALU}.\text{add}(\text{source0},\text{source1});$
Outline

- Background
- Proposed Processor Generation Method
- Experiments
- Conclusion
Experiments

- Experimental setup
  - Design MIPS R3000 and DLX, and compare design time and design quality between conventional method and proposed method
    - Confirm the reduction of design time without degradation of design quality
  - Modify DLX by changing the pipeline architecture and implementing extra specific instructions, and compare design time and design quality
    - Confirm fast modification
- Conventional method
  - A designer manually describe micro-operation description
- Environment
  - Use ASIP Meister* as a processor design environment

Implemented Processors

- MIPS R3000 subset
  - 5 pipeline stages
  - 42 instructions
    - 13 ALU operation, 4 mult/div, 11 immediate operation, 8 memory access, and 6 jump/branch

- DLX subset with 3 pipeline stages
  - 3 pipeline stages
  - 51 instructions
    - 16 ALU operation, 4 mult/div, 17 immediate operation, 8 memory access, and 6 jump/branch

- Modified DLX subset
  - 5 pipeline stages
  - 8 extra instructions
    - 2 multiply and accumulate (MAC), 4 memory access with post-increment/decrement, ABS(calculation of absolute), and CEX(compare and exchange)
Comparison of Design Time

MIPS R3000 subset

<table>
<thead>
<tr>
<th></th>
<th>conventional</th>
<th>proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture Def.</td>
<td>30</td>
<td>20</td>
</tr>
<tr>
<td>Semantics Def.</td>
<td>100</td>
<td>45</td>
</tr>
<tr>
<td>Operation Def.</td>
<td>45</td>
<td>45</td>
</tr>
<tr>
<td>Others</td>
<td>55</td>
<td>55</td>
</tr>
<tr>
<td>Reduced by 48%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DLX subset

<table>
<thead>
<tr>
<th></th>
<th>conventional</th>
<th>proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture Def.</td>
<td>300</td>
<td>40</td>
</tr>
<tr>
<td>Semantics Def.</td>
<td>125</td>
<td>60</td>
</tr>
<tr>
<td>Operation Def.</td>
<td>60</td>
<td>75</td>
</tr>
<tr>
<td>Others</td>
<td>75</td>
<td>20</td>
</tr>
<tr>
<td>Reduced by 48%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Comparison of Design Quality

Area

<table>
<thead>
<tr>
<th></th>
<th>Conventional</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIPS R3000</td>
<td>36.8</td>
<td>36.1</td>
</tr>
<tr>
<td>DLX</td>
<td>39.1</td>
<td>36.1</td>
</tr>
</tbody>
</table>

Delay

library: 0.18 μm CMOS

<table>
<thead>
<tr>
<th></th>
<th>Conventional</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIPS R3000</td>
<td>8.85</td>
<td>9.72</td>
</tr>
<tr>
<td>DLX</td>
<td>8.97</td>
<td>9.83</td>
</tr>
</tbody>
</table>
Modification of DLX processor

**Design Time**
- Conventional: 50 minutes
- Proposed: 20 minutes

**Area**
- Conventional: 52.2 Kgates
- Proposed: 52.8 Kgates

**Delay Time**
- Conventional: 8.41 ns
- Proposed: 8.52 ns
Outline

- Background
- Proposed Processor Generation Method
- Experiments
- Conclusion
Conclusion

- A method of generating micro-operation description from behavior description
  - Generate micro-operation fragments from abstract syntax trees
  - Automatically allocate fragments, base on attribute of each stage
- Quick design becomes possible
  - Reduce code by about 65 %
  - Reduce design time by about 50%
  - Hardly degrade
- Future Work
  - Optimizing combination of functional units
  - Generate micro-operation description of interrupts