Modeling the Overshooting Effect for CMOS Inverter in Nanometer Technologies

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Outline

- Background
- Analytical expressions for overshooting effect
- Considering process variation
- Simulation results
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The differential equation for the CMOS inverter is:

\[ C_L \frac{dV_{out}}{dt} = I_p - I_n + C_M \frac{d(V_{in} - V_{out})}{dt}, \]

where:

- \( C_L \) is the load capacitance,
- \( I_p \) and \( I_n \) are the currents through the p- and n-channel transistors, respectively,
- \( C_M \) is the Miller capacitance,
- \( V_{in} \) and \( V_{out} \) are the input and output voltages, respectively.

The input voltage for the falling input ramp is expressed as:

\[ V_{in} = \begin{cases} 
V_{DD} & : t \leq 0 \\
(1 - \frac{t}{t_{in}})V_{DD} & : 0 \leq t \leq t_{in} \\
0 & : t > t_{in} 
\end{cases} \]

“\( C_M \) is known as the Miller effect, but is seldom of importance in digital circuits. It is, however, of major importance in analog circuits.”
I. Background

For traditional process technologies, the effect of overshooting is very small and can be neglected.

\[ t_D = t_{50} - \frac{1}{2} t_{in} \]

\[ t_D = t_{ov} + t_r - \frac{1}{2} t_{in} \]
I. Background

The influence of overshooting time on timing analysis

- $t_{ov}$ decreases much faster than $t_r$ and $t_d$ with the increasing of gate sizes. And $t_{ov}$ is equal to or larger than $t_r$.

- With the scaling of technology process, $t_{ov}$ becomes much important for delay time.
I. Background

The influence of overshooting time on power analysis

Short-circuit power consumption

The overshooting time is one important parameter for power consumption estimation.

\[ P = V_{DD} \int_{t_{ov}}^{t_{off}} I_n \, dt \]
I. Background

Conventional models for overshooting time

The overshooting time is neglected

\[ t_{ov} = 0. \]

The overshooting time is assumed as simple value

\[ t_{ov} = \left( \frac{V_t}{V_{dd}} \right) t_{in} \]

J. L. Rossell, …“Charge-based analytical model for the evaluation of power consumption …”, TCAD 2002.
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- **Simulation results**
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II. Proposed Model

\[ V_{out}(t) = \frac{C_M}{\beta_n \left( V_{GS} - V_{THN} \right)} \frac{dV_{in}}{dt} \left[ 1 - e^{-\frac{\beta_n (V_{GS} - V_{THN})}{C_L + C_M}} \right] \]
II. Proposed Model

\[ t_{vmin} = t_T + \kappa(t_{in} - t_T), \]

\[ \kappa = \frac{C_M V_{DD} e^{-\frac{\rho(V_{DD} - V_T)}{C_L + C_M}} t_T}{t_{in} I_{D0}}. \]

\[ t_{ov} = t_{vmin} - \frac{1}{2} \left[ t_{vmin} - t_{Teff} - C_M \frac{V_{DD} t_{in} - t_{Teff}}{I_{D0}} \right] \]

\[ + \sqrt{\frac{2 Q_1}{I_{D0}} \left( t_{in} - t_{Teff} \right)} + \frac{1}{4} \left[ t_{vmin} - t_{Teff} - C_M \frac{V_{DD} t_{in} - t_{Teff}}{I_{D0}} \right]^2, \]
II. Proposed Model

Minimum overshooting time

\[ \lim_{t_{in}\to 0} t_{ov} = t_{ov}^{min} = \frac{C_M}{I_{D0}} (V_{DD} - V_{Teff}). \]

\[ t_D = t_{ov} + t_r - \frac{1}{2} t_{in} \]

The overshooting time has minimum values.

Minimum delay > Minimum overshooting time
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III. Considering Process Variation

In recent technologies, the variability of circuit performance due to the process variation has become a significant concern. As process geometries continue to shrink, the evaluation for critical device parameters is becoming more and more difficult due to the significant variations.

The sensitivities of the overshooting time with respect to the variation sources.

\[ t_{ov} = t_{ov}^0 + \frac{\partial t_{ov}}{\partial V_T} \Delta V_T + \frac{\partial t_{ov}}{\partial T_{ox}} \Delta T_{ox} + \frac{\partial t_{ov}}{\partial L} \Delta L, \]

With respect to the variation of length.

\[ \frac{\partial t_{ov}}{\partial L} = \lambda_L \approx 0, \]

With respect to the variation of threshold voltage.

\[ \frac{\partial t_{ov}}{\partial V_T} = \lambda_{VT} \approx \frac{t_{in}}{V_{DD}} \left[ 1 - \kappa - \xi (1 - C_M \frac{V_{DD}}{t_{in} I_{D0}}) \right], \]
III. Considering Process Variation

Variation of $L$ has no influence on the overshooting time.

Variation of $L$ has the influence only on the rising time.

\[ t_D = t_{ov} + t_r - \frac{1}{2} t_{in} \]

\[ \frac{\partial t_{ov}}{\partial L} = \lambda_L \approx 0, \]

D. Sinha, “Gate Sizing Using Incremental Parameterized Statistical Timing Analysis” ICCAD-2005
III. Considering Process Variation

1. With input time decreases, the influence due to the Tox decreases greatly.

2. The influence due to L is 0.

3. With the scaling of process technologies, the variation of Vt increases, the influence due to Vt will increase greatly.

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</table>

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IV. Simulation Results

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V. Conclusions

- The input-to-output coupling capacitance has been proved to have significant influence on CMOS gates: timing analysis and power analysis.

- The overshooting time has become one of main parts of gate delay.

- The analytical model for overshooting time is derived.
  1. The overshooting time has minimum value
  2. Gate delay cannot be smaller than this minimum value.

- Considering process variation:
  1. The variation due to L has the influence only on output rising time, but has almost no influence on overshooting time.
  2. The variation due to Vt has the most significant influence on overshooting time with the scaling of technologies.
Thank you for your attentions