Development of Low Power ISDB-T One-Segment Decoder by Mobile Multi-Media Engine SoC (S1G)

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Toshiba Corp.
Semiconductor Company
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Outline

- System Overview
- Chip Specification
- Power Comparison
- Low Power Analysis
  - Multi-Vth Technique
  - Clock Gating Techniques
  - Software Architecture
- Summary
S1G in Mobile Phone System

- Digital TV Tuner
  - OFDM
- TV in
- TV out
- Camera module
  - Camera I/F
- Dynastron
- LCD module
  - LCDD
- Back Light
- LCD
- Hard Disk
- SD, mini SD
- Memory Card-I/F
  - Security
- Memory Module (NAND)
- NAND, MCP
- H.264
- MPEG4
- AAC
- MP3
- WMA
- AMR
- Audio DAC
- Audio
- Video/JPEG
- 2D/3D Graphic
- ARM
- BB LSI
  - MODEM
  - 3G/GPRS/
- MCP
- PS regulator
- RF
- BT
- High speed serial bus
- TV in
- TV out
- High speed serial bus
- OFDM
ISDB-T 1-seg Data Flow

① TS Packet Receiving & Buffering
② De-multiplexing of TS packet
③ H.264 & Audio decoding
④ Scaling for display
⑤ Output of Video data
⑥ Output of Audio data

Audio DA/AD
Sub LCD
Main LCD
NTSC Encoder
LVDS Panel
System Clock Input

Audio I/F
SIF
IO Bus
Indirect Bus
Memory Bus

MPG-MeP @DSP VA
DRAM Controller
LPLL
LVDSC I/F
LVDSL I/F
LVDS Panel

LPLL
2D SD
JPEG Cont.
Scaler

Camera I/F
Scaler
JPEG Cont.

H.264 & Audio decoding
De-multiplexing of TS packet
Output of Video data
Output of Audio data

① TS Packet Receiving & Buffering
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Memory
Psedo Sync.
27MHz

LVDS Camera
DTV Tuner

ASP-DAC 2007 YOKOHAMA
Jan. 25, 2007

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S1G Floor plan and Chip specification

- Technology
  - Toshiba 90nm CMOS
  - 5 layer metal
  - Multi-Vth
  - Embedded DRAM

- Package
  - 289pin TFBGA

- Logic Gate
  - 2.7MGate

- Memory
  - SRAM 1.3Mbit
  - eDRAM 20Mbit

- Supply Voltage
  - 1.2V Core
  - 2.5V eDRAM
  - 1.8V/3.0V IO

- Operation Frequency
  - 162MHz
Evaluation Environment

Power is measured by this environment. Not simulation

S1G PCI Board

ISDB-T Receiving picture

Host CPU (PC)

UHF input

TS IF

42mW ISDB-T 1-seg

Control of ISDB-T Tuner Module by PC application

ISDB-T Tuner Module

Evaluation Environment

Power is measured by this environment. Not simulation

S1G PCI Board

Host CPU (PC)

UHF input

TS IF

42mW ISDB-T 1-seg

Control of ISDB-T Tuner Module by PC application

ISDB-T Tuner Module
Power Comparison

MPEG4 Decode operation
(Condition: QVGA, 15fps, 384kbps)

<table>
<thead>
<tr>
<th></th>
<th>Hardware Solution</th>
<th>Software Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product A</td>
<td>160 mW</td>
<td>80 mW</td>
</tr>
<tr>
<td>(130nm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Product B</td>
<td>100 mW</td>
<td></td>
</tr>
<tr>
<td>(90nm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S1G</td>
<td>40 mW</td>
<td></td>
</tr>
<tr>
<td>(90nm)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Breakdown of Power Consumption

Total Power

Data Path

IDLE Power

Clock Tree

Leak

Applied techniques for Low Power in S1G

90nm technology

Low operation frequency

Module level clock gating

Clock gating by S/W control

H/W Clock gating by Tool

Multi-Vth Technique
Multi-Vth Technique for Low Leak Design

First achievement

HS ratio becomes low but timing violation occurs

LP cells in violation paths replaced to HS cells again

<table>
<thead>
<tr>
<th></th>
<th>LP Replacement</th>
<th>LP ratio [%]</th>
<th>25°C</th>
<th>85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leak Power [mW]</td>
<td>Leak Power [mW]</td>
<td>Leak [mW]</td>
<td>Leak [mW]</td>
<td></td>
</tr>
<tr>
<td>Before</td>
<td>51.0</td>
<td>1.99</td>
<td>0.59</td>
<td>13.44</td>
</tr>
<tr>
<td>After</td>
<td>75.3</td>
<td>1.39</td>
<td>4.79</td>
<td>8.65</td>
</tr>
</tbody>
</table>
Clock Hierarchy in S1G

PLL
sysclk

Clock Generator

Module level
clock gating

MPG–MeP Module

MeP

Sleep/Halt
Instruction

GMM–MeP Module

MeP

Sleep/Halt
Instruction

Other Modules

S/W control
clock gating for
MPG, GMM

H/W automatic
clock gating
Relation between Gate counts and IDLE power

IDLE Power vs Module gate counts

- IDLE (offset) power is proportional to module gate counts
- Clock gating by Power Compiler
- Additional Clock gating makes further low power

Gate Counts [KGate]

0 100 200 300 400 500 600 700 800

IDLE Power [mW]

0 5 10 15 20 25 30

0.036 mW/KGate

0.024 mW/KGate
Software architecture

Host CPU

TS I/F
TS Demux
GMM MeP

AAC Decoder
H264 Decoder
Compositor
Scaler

Speaker
LCD

Pre-processing
Non routine task
Syntax analysis etc
Routine task
Signal processing
Composition by H/W

Demux
Sleep
Audio

Video
Sleep

Demux
Sleep

GMM MeP
TS Demux, Control

1msec

MPG MeP
Video Audio Video Audio Video Audio

20msec

@DSP
Video Audio Video Audio Video Audio

Scaler
Composition

Composition

Video Audio Video Audio Video Audio
H.264 Decoder in MPG module

 Pipeline

 Shared Data Memory makes effective pipeline operation
 between MPG–MeP and @DSP

 Bit Stream

 MPG–MeP
 Syntax Analysis

 MeP Local Data Memory

 @DSP
 Signal Processing

 Frame Memory

 Picture

 10% MIPS Reduction by MeP
 User Custom Instructions

 Peak MIPS

 Load balance

 Simultaneous Operation

 10% MIPS Reduction

 Peak MIPS

 Low operation frequency
 by good load balance

 MPG–MeP

 @DSP
MeP User Custom Instruction

User can define and implement UCI to reduce operation MIPS of target application

From profiling result of H.264 decoder, 1)Table search, 2)Bit manipulation etc… 10 kinds of UCIs are implemented

10% MIPS Reduction
## Summary of Application Power

<table>
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<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>ISDB-T 1-Seg.</td>
<td>H.264</td>
<td>320x180</td>
<td>15</td>
<td>214</td>
<td>AAC+SBR Stereo</td>
<td>48</td>
<td>32</td>
<td>42</td>
</tr>
<tr>
<td>H.264 Decode</td>
<td>H.264</td>
<td>320x240</td>
<td>15</td>
<td>384</td>
<td>AAC Stereo</td>
<td>44.1</td>
<td>32</td>
<td>49</td>
</tr>
<tr>
<td>MPEG4 Encode</td>
<td>MPEG4</td>
<td>320x240</td>
<td>15</td>
<td>384</td>
<td>AMR-NB</td>
<td>8</td>
<td>12.2</td>
<td>63</td>
</tr>
<tr>
<td>MPEG4 Decode</td>
<td>MPEG4</td>
<td>320x240</td>
<td>15</td>
<td>384</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>45</td>
</tr>
<tr>
<td>AAC Decode</td>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>AAC Stereo</td>
<td>48</td>
<td>128</td>
<td>13</td>
</tr>
</tbody>
</table>
Relation between MIPS and Power

\[ P = \text{DataPath} + \text{IDLE} \]

- \textbf{P}: Total Core Power
- \textbf{DataPath}: Actual operation power (Frequency x Slope)
- \textbf{IDLE}: IDLE Power (Sysclk is provided)

**Core Power vs Operation MIPS**

- **Product A**: Audio + Video
- **S1G**: Audio + Video, Video, MPEG4 Enc, Operated at 162MHz, ISDB-T 1-seg.
- **37mW**: Sleep State
- **10mW**: AAC Dec

**Graph Details**
- **Core Power [mW]**
  - 0 to 130
- **Operation MIPS**
  - 0 to 180

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Summary

- Multi-Vth technique is effective for low leak design
- Additional clock gating by sleep instruction of MeP processor realizes lower IDLE power
- RUN and IDLE control in fine grain by S/W is effective for low power operation
- Good load balance between processors leads low operation frequency

We have accomplished low power ISDB-T One-segment in 42mW.