Simultaneous Control of Subthreshold and Gate Leakage Current in Nanometer-Scale CMOS Circuits

Youngsoo Shin¹, Sewan Heo¹, Hyung-Ock Kim¹, Jung Yun Choi²

¹Dept. of Electrical Engineering, KAIST, KOREA
²Samsung Electronics, KOREA
Outline

• Introduction: leakage current, power gating
• Supply switching with ground collapse (SSGC)
• Implementation of SSGC
• Experimental results
• Summary
Leakage Current

- Leakage current in nanometer regime
  - Exponential growth of leakage
    - Subthreshold leakage due to reduced $V_{th}$
    - Gate leakage due to reduced $T_{ox}$

Leakage Current

- **Gate leakage current**
  - Grow faster than subthreshold leakage
  - May dictate the total leakage in future technology
Power Gating

- Power gating
  - Widely used to suppress subthreshold leakage
  - Active mode: footer turned-on
  - Standby mode: footer cuts off power rail

Balloon circuit [Schigematsu-JSSC-1997]
Power Gating

- Power gating in nanometer regime
  - State-retention and output-holding circuit leak gate leakage
  - Leakage saving from power gating greatly reduced

ISCAS benchmark s1269 w/ power gating
Supply Switching with Ground Collapse

- **SSGC:** supply control + power gating

**Active**
- Supply switching circuits: $V_{dd}$
- Footer: on

**Standby**
- Supply switching circuits: $V_{sv} (< V_{dd})$
- Footer: off

![Supply switching with Ground Collapse Diagram](attachment:image.png)
Supply Switching with Ground Collapse

- SSGC circuit
  - Reduce leakage of combinational logic through power gating (ground collapse)
  - Reduce leakage of FF through lowered voltage (supply switching) and power gating
  - No need to use state-retention FF
Supply Switching with Ground Collapse

- Implementation of SSGC
  - Design of supply switching circuits
  - Physical design
    - Power networks
    - SSGC flip-flop
    - Footer
    - Output-holding circuit
Supply Switching Circuits

- **M1 switch**
  - Supplying active \( V_{dd} \)
  - High \( V_{th} \) PMOS
  - Sizing affects circuit performance

- **M2 switch**
  - Supplying standby-mode \( V_{sv} \)
  - Low \( V_{th} \) NMOS
Supply Switching Circuits

- $V_{ddv}$ in standby
  - Bounded by the potential to retain states in FFs + noise margin
  - Factors: temperature, process variation, states (0 or 1), FF types

\[
\begin{align*}
\text{Temperature } [\degree \text{C}] & \quad 90\text{nm, 1.0V} \\
0 & \quad 260\text{mV for state retention}
\end{align*}
\]
Supply Switching Circuits

- Design of M2 switch
  - Selection of M2 size and $V_{sv}$ for
    - Efficient leakage saving
    - Lowest $V_{ddv}$ (e.g. 260mV)
  - Voltage drop across M2 dictates $V_{sv}$

\[ V_{sv} = V_{ddv} + I_{leakage} \times R_{M2} \]

\[ R_{M2} = \frac{R_{min}}{\text{M2 size}} \]
Supply Switching Circuits

- Design of M2 switch
  - M2 size vs. $V_{sv}$
    - Trade-off between area overhead and leakage power

\[ V_{sv} = V_{ddv} + I_{leakage} \times \frac{R_{min}}{M2 \text{ size}} \]

- Graphs showing $V_{sv}$ and leakage current vs. M2 size for different temperatures:
  - $V_{sv}$ at Temp=125°C
  - Leakage current at Temp=25°C

- M2 size = 20um
Physical Design of SSGC

- Power networks for SSGC
  - Conventional $V_{dd}$ and $V_{ss}$ rails as $V_{dDV}$ and $V_{SSV}$ rails

$V_{dd}$: vertical rails
$V_{ss}$: horizontal rails

$V_{dDV}$ and $V_{SSV}$ rails for combinational logic cells
Physical Design of SSGC

- SSGC flip-flop
  - State maintained in slave latch with low $V_{sv}$
    - No need of state-retention element
    - Low gate and subthreshold leakage current
      - Other parts are power gated for further reduction
• Footer layout
  - Isolated body (body bias to $V_{ss}$) preferred for leakage current $\rightarrow$ area overhead due to well isolation
  - Building block-based approach: flexible placement, control of area overhead
Physical Design of SSGC

- Output-holding circuit
  - Output-holding circuits are needed due to $V_{sv}(<V_{dd})$ in standby
  - Utilize high $V_{th}$ to reduce subthreshold leakage
SSGC Design Flow

1. Gate-level netlist
2. Footer sizing
3. M1 sizing
4. M2 and $V_{sv}$ design
5. Replacing Flip-flops
6. Inserting output-holding circuits
7. Inserting footer, M1, M2
8. Power network
9. Footer, M1, M2 placement
10. Auto P & R
11. SSGC layout

Footer and supply switching circuits design
Modifying SSGC netlist
SSGC physical design
Experimental Results

- Test circuits
  - ISCAS and ITC benchmark circuits
  - 65- and 45-nm predictive models
Case Study: ETM

- **Embedded Trace Macrocell (ETM)**
  - Debugging and tracing core for ARM
  - 90nm, 1.0V commercial process

<table>
<thead>
<tr>
<th>I / Os</th>
<th>SEs</th>
<th>Gates</th>
<th>Leakage</th>
</tr>
</thead>
<tbody>
<tr>
<td>320 / 124</td>
<td>5,501</td>
<td>90,068</td>
<td>410uA</td>
</tr>
</tbody>
</table>

- **Footer, M1, and M2 sizing**
  - M1 and footer sizing for 10% delay increase
  - M2 sizing to optimize leakage at room temperature
Case Study: ETM

- SSGC implementation result
  - Total leakage saving: 32× at 25°C
  - Area increase: 3%
  - Wirelength increase: 6%

Leakage current breakdown

- Output-holding circuits: 0.3µA
- Footer: 0.1µA
- SEs: 12.8µA
- Power rings: 0.71 mm
Summary

- **Power gating**
  - Widely used to suppress subthreshold leakage
  - NOT efficient in nanometer technology due to gate leakage of storage elements and output-holding circuits

- **Supply switching with ground collapse**
  - Overcomes the limitation of power gating
  - Demonstrates cell-based semicustom design flow based on SSGC