ARM11 MPCore™

The streamlined and scalable ARM11 processor core

Kazuyuki HIRATA
Senior Manager – Business Development
ARM K.K.

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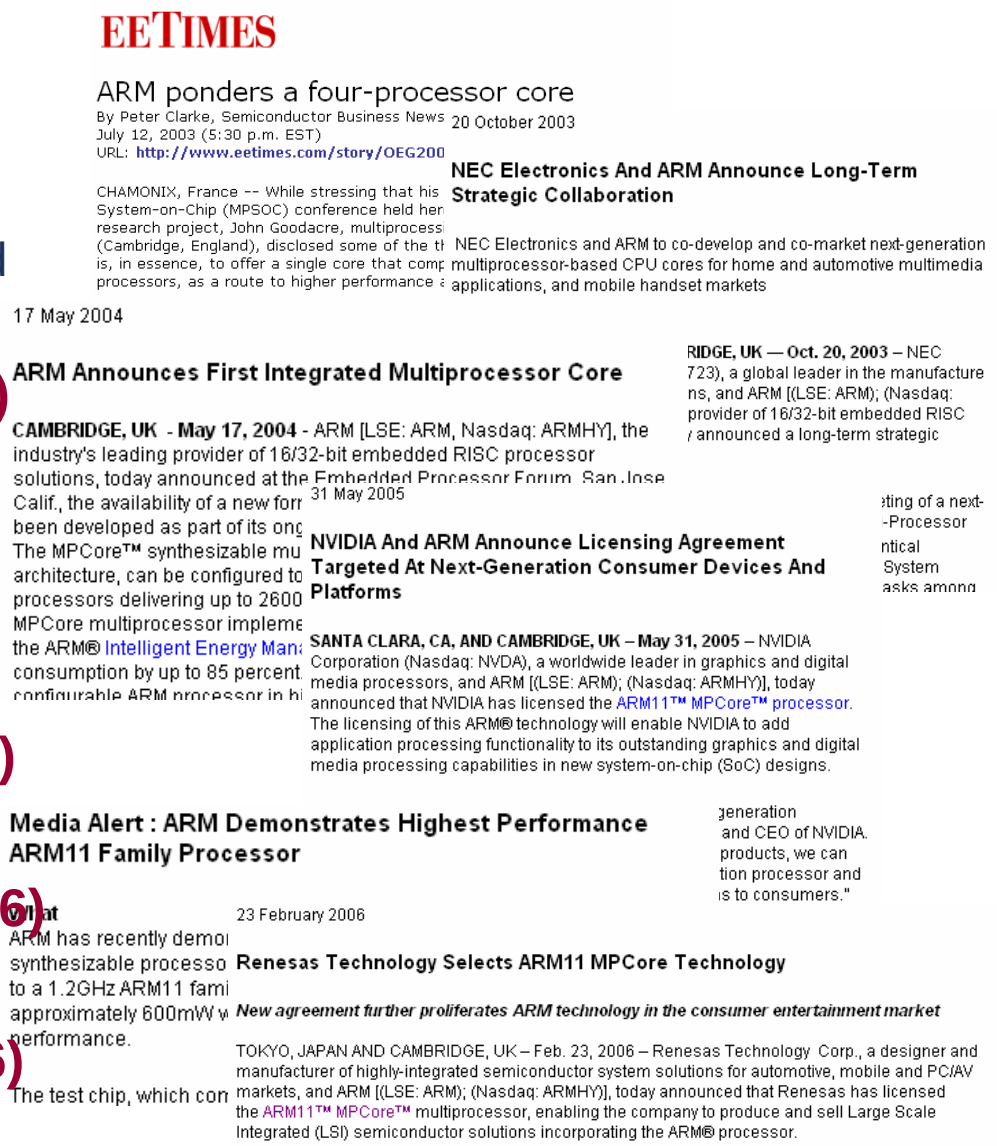
Quick History of ARM11 MPCore

- **First public disclosure (July'03)**
  - "4 CPU's look interesting"
- **MPCore announced (May'04)**
  - "Desktop performance at handheld power levels"
- **NECEL in Collaboration (Oct'04)**
  - Bring Multi Core capable cores to market
- **Working First Silicon (July'05)**
  - "Highest performance ARM"
- **NVIDIA selects MPCore (May'05)**
  - "To add applications processing"
- **Renesas selects MPCore (Feb'06)**
  - "Consumer entertainment
- **Sarnoff licence MPCore (July'06)**
  - "Mobile Vision SoC"



EETIMES

ARM ponders a four-processor core

By Peter Clarke, Semiconductor Business News
July 12, 2003 (5:30 p.m. EST)
URL: http://www.eetimes.com/story/OEG200

CHAMONIX, France -- While stressing that his
System-on-Chip (MPSOC) conference held her
research project, John Goodacre, multiprocess
(Cambridge, England), disclosed some of the tl
is, in essence, to offer a single core that comp
processors, as a route to higher performance

20 October 2003

NEC Electronics And ARM Announce Long-Term Strategic Collaboration

NEC Electronics and ARM to co-develop and co-market next-generation multiprocessor-based CPU cores for home and automotive multimedia applications, and mobile handset markets

17 May 2004

ARM Announces First Integrated Multiprocessor Core

CAMBRIDGE, UK - May 17, 2004 - ARM [LSE: ARM, Nasdaq: ARMHY], the industry's leading provider of 16/32-bit embedded RISC processor solutions, today announced at the Embedded Processor Forum, San Jose Calif., the availability of a new forr
been developed as part of its ong
The MPCore™ synthesizable mu
architecture, can be configured to
processors delivering up to 2600
MPCore multiprocessor impleme
the ARM® Intelligent Energy Mana
consumption by up to 85 percent
configurable ARM processor in hi

RIDGE, UK — Oct. 20, 2003 – NEC
723), a global leader in the manufacture
ns, and ARM [(LSE: ARM); (Nasdaq:
provider of 16/32-bit embedded RISC
announced a long-term strategic

31 May 2005

NVIDIA And ARM Announce Licensing Agreement Targeted At Next-Generation Consumer Devices And Platforms

SANTA CLARA, CA, AND CAMBRIDGE, UK – May 31, 2005 – NVIDIA Corporation (Nasdaq: NVDA), a worldwide leader in graphics and digital media processors, and ARM [(LSE: ARM); (Nasdaq: ARMHY)], today announced that NVIDIA has licensed the ARM11™ MPCore™ processor. The licensing of this ARM® technology will enable NVIDIA to add application processing functionality to its outstanding graphics and digital media processing capabilities in new system-on-chip (SoC) designs.

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Media Alert : ARM Demonstrates Highest Performance ARM11 Family Processor

generation
and CEO of NVIDIA.
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s to consumers."

23 February 2006

Renesas Technology Selects ARM11 MPCore Technology

New agreement further proliferates ARM technology in the consumer entertainment market

TOKYO, JAPAN AND CAMBRIDGE, UK – Feb. 23, 2006 – Renesas Technology Corp., a designer and manufacturer of highly-integrated semiconductor system solutions for automotive, mobile and PC/AV markets, and ARM [(LSE: ARM); (Nasdaq: ARMHY)], today announced that Renesas has licensed the ARM11™ MPCore™ multiprocessor, enabling the company to produce and sell Large Scale Integrated (LSI) semiconductor solutions incorporating the ARM® processor.

ARM11 MPCore: Key Benefits

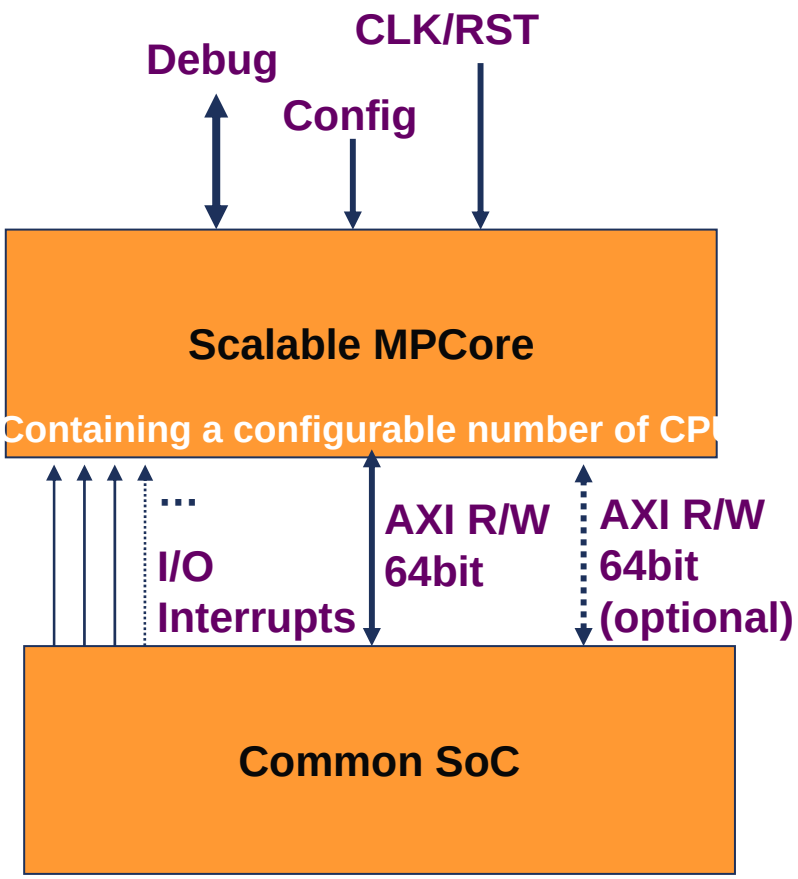
- **ARM v6 Architectural Compatibility**
  - Full ARMv6K ISA with ARM, Thumb, SIMD, and Jazelle and optional FP
  - Offering a rich software and support ecosystem to de-risk and simplify product development
- **Flexible and Easy system design**
  - Mixed system configuration of SMP and AMP
  - Uni-Interface independent from the number of cores
  - L1 cache coherency
- **Performance scalability and low power consumption for application processing**
  - Offering a scalable solution over a broad cost/performance envelope
  - With advanced power management technology to reduce power consumption by up to 85%
- **Rich and high efficiency processing**
  - Highly efficient memory system permitting higher performance from slower and cheaper memory systems

Target Applications

- Next generation consumer devices
  - From rich single-cpu handheld devices through to embedded general purpose computing platforms
- Rich multi-function networking/enterprise appliances
  - High throughput embedded devices
  - Computer graphics
  - Imaging
- Auto-infotainment and navigation
  - Routing, Recognition, Media-Player, etc
- Wireless handsets
  - Open multi-media platforms

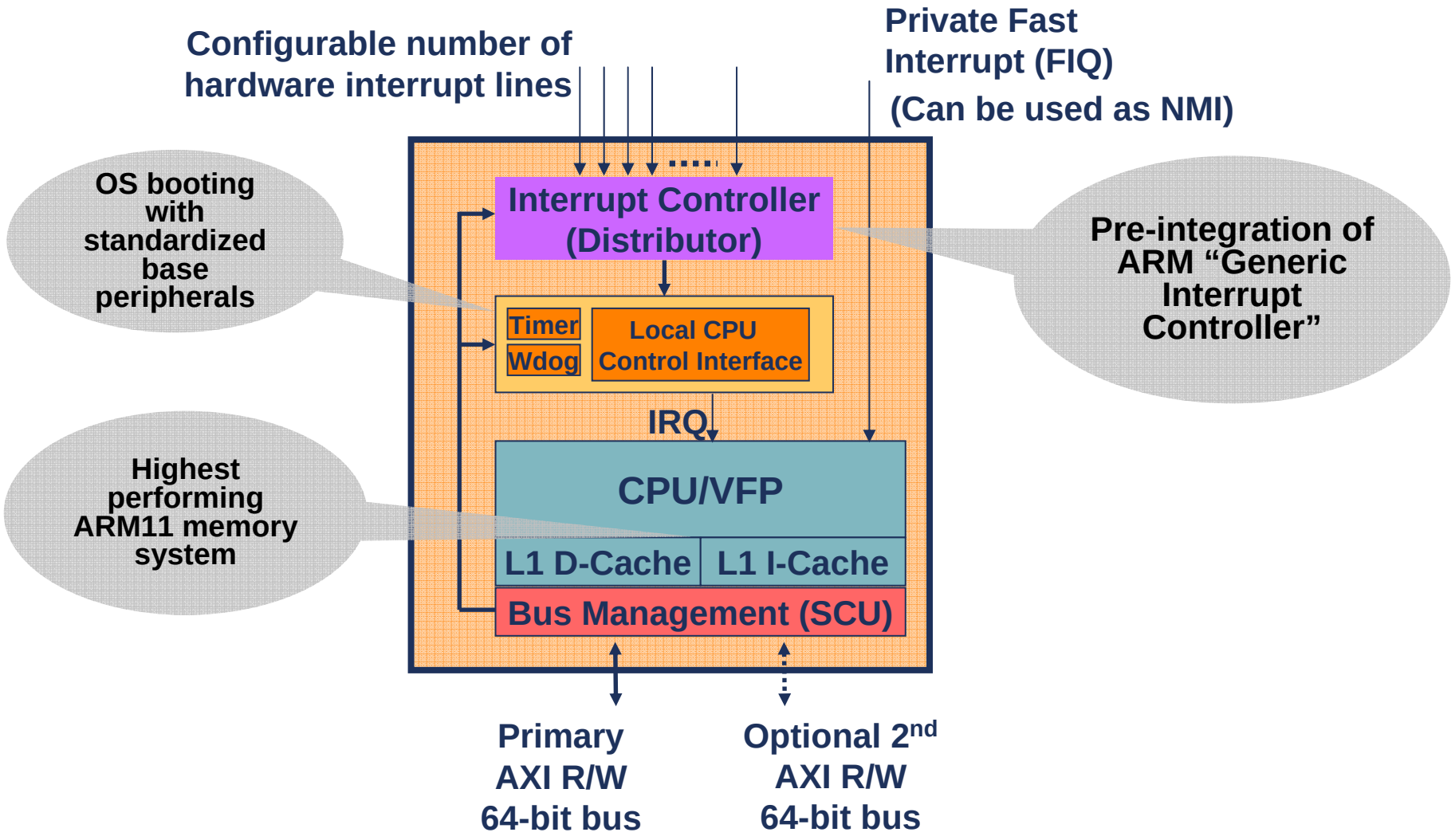
Current devices using ARM (non-MPCore)

MPCore Simplifies Multiprocessor SoC



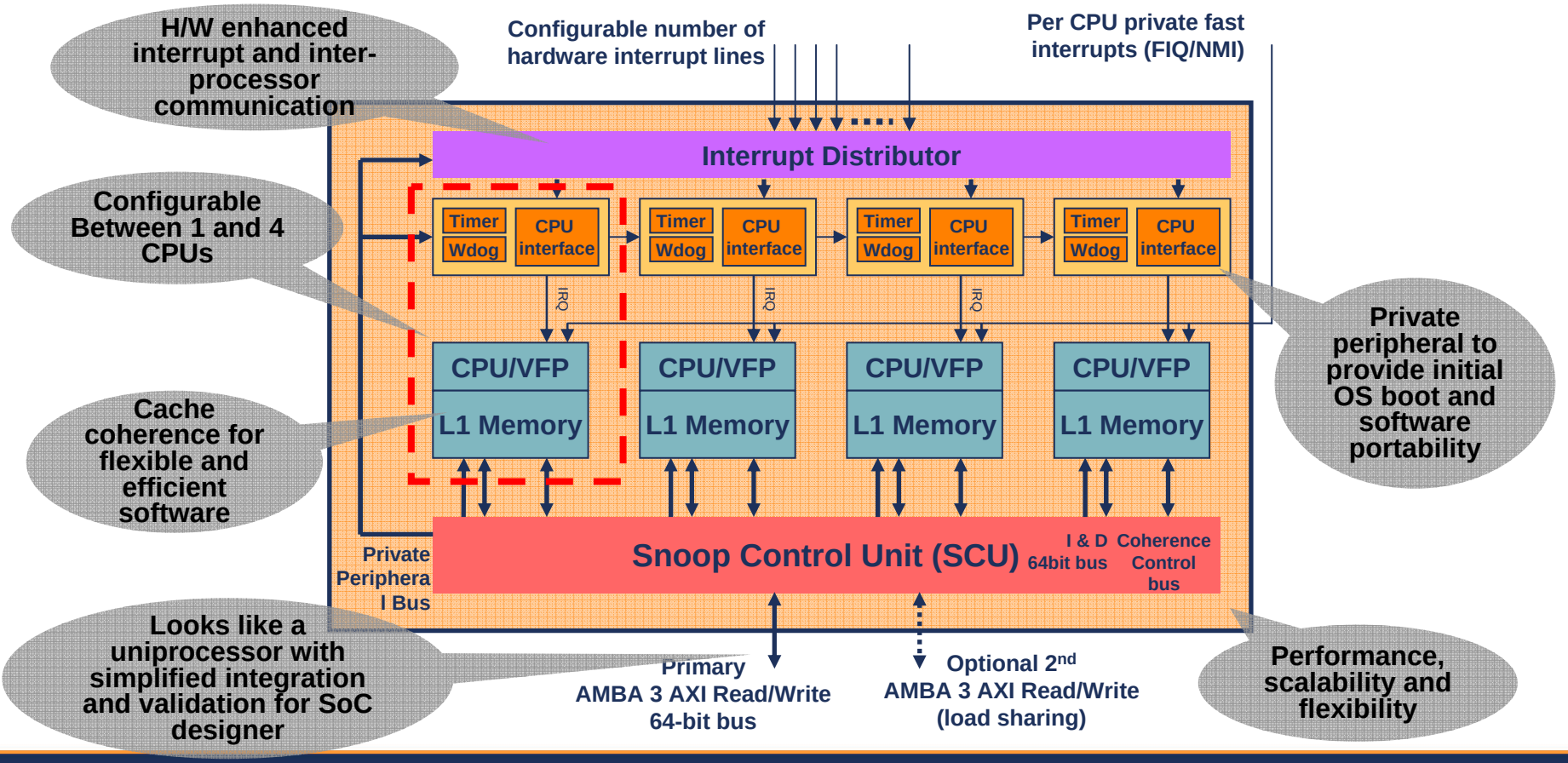
- **'Looks' like a uniprocessor**
  - Simplified SoC integration
  - Common solution for a range of devices
  - Standardized software platform
- Synthesis configurability
  - Number of processors
  - Number of interrupts
  - Number of system bus
  - Size of data and inst. caches
  - Vector Floating Point coprocessor per CPU
  - Support for DVFS (level shifters/latches)
  - Synchronous or Asynchronous bus interface

ARM11 MPCore (Single CPU)

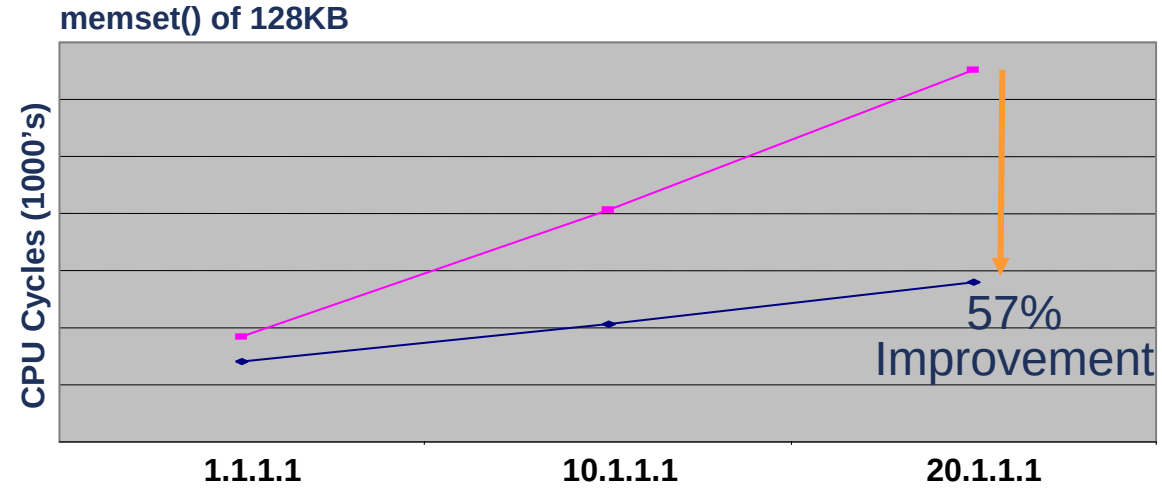


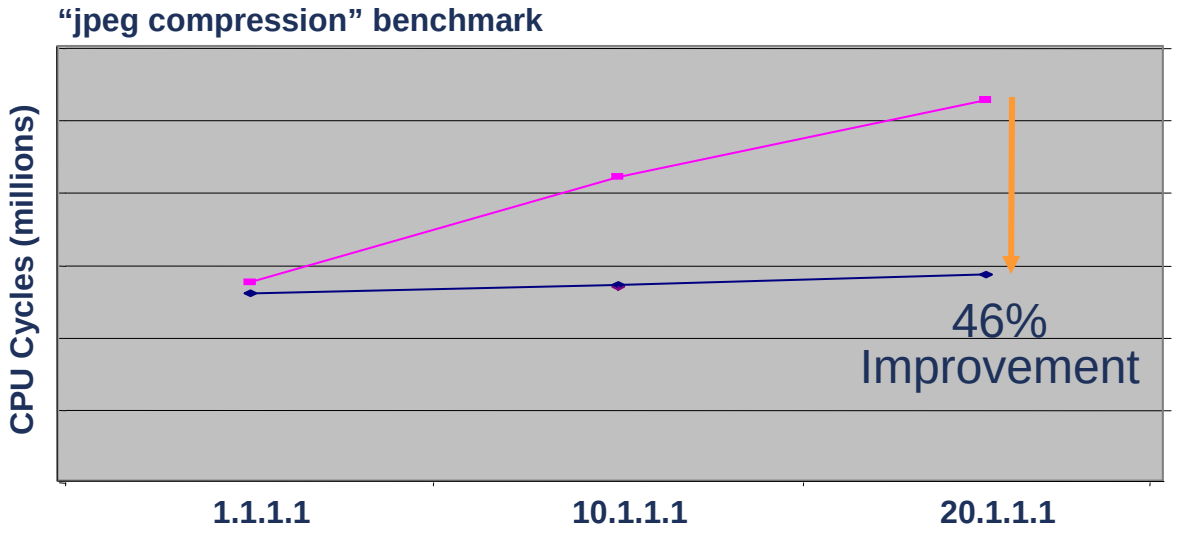
Scalable Multiprocessing

- **RTL synthesis configurations to define scalability between 1 and 4 CPUs**
  - With the design addressing the scalability and bottlenecks of traditional MP design
  - Interrupt distributor for low latency inter-processor communications
  - Snoop control unit for high performance and power efficient cache coherency



Benefits from MPCore's Enhanced L1

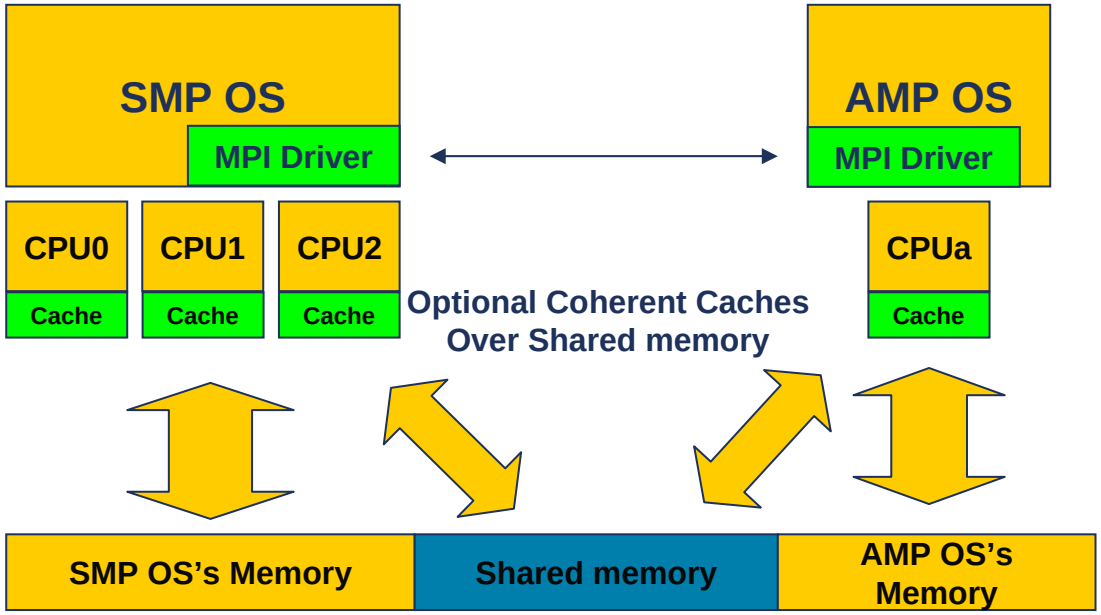




- Memory throughput improvement due to MPCore's L1 memory system
  - Providing better memory bursting
  - Providing higher performance from higher latency memory
  - Reducing power consumption by less memory activity

Without enhancement
With enhancements

SMP / AMP Hybrid System



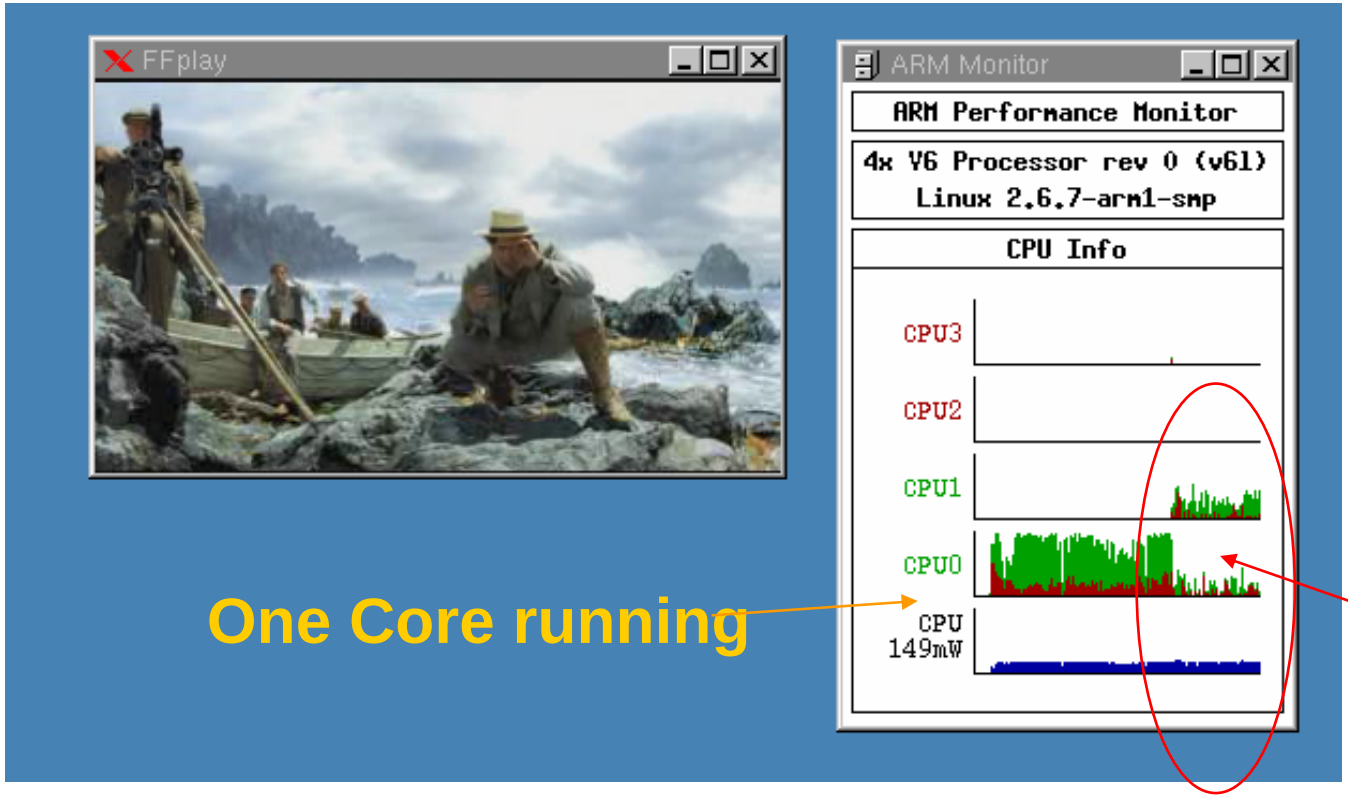
- **MPI (Message Passing Interrupt) Driver**
  - 'send a message' via MPCore's IPI 'doorbell' mechanism
  - Handling doorbell notification into OS applications. Eg 'receive a message'
  - Ensuring ownership and usage of shared memory

CPU Power Management

- Adaptive power management for workload variation
- Four low power mode per core

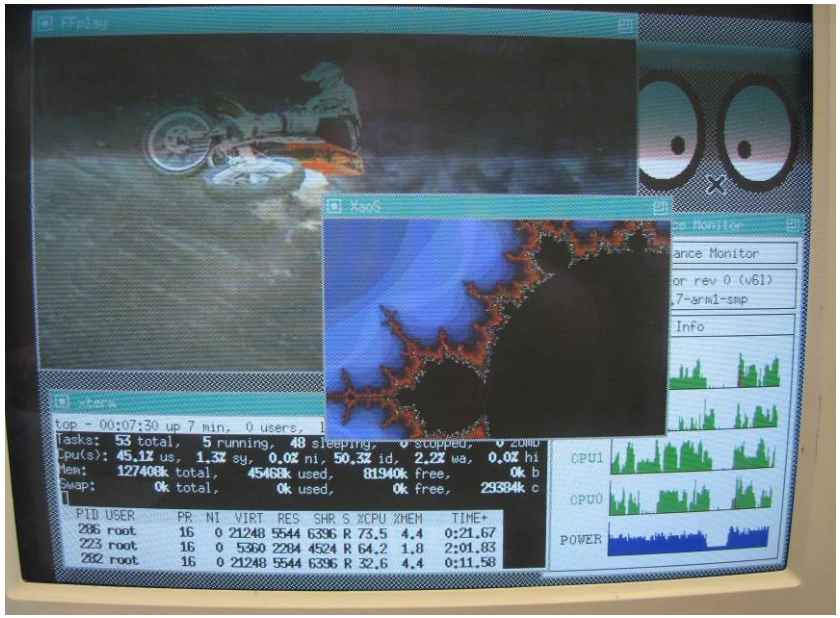
	CPU Logic	RAM Arrays (L1 Memory)	*Wake-up Mechanism*
Running	Powered up Everything clocked	Powered	*N/A*
Standby	Powered up Only wake-up logic clocked	Powered	*Wake up on interrupts (external I/O or Timer / WatchDog) or Event*
Dormant	Power off	Retention state voltage only	*Via external wake-up event from power controller*
Power Off	Power off	Power off	*Via external wake up event from power controller*

Demonstration of power save with MP



- Reduced MHz allow for lower supply voltage which enables more than 50% energy save
- Lower power in dual-CPU than single-CPU at same MHz
  - Reduction in context switching
  - Increase in cache effectiveness

ARM11 MPCore – Test Chip - first time



CT11-MPCore Coretile

ARM Integrator/CP Baseboard

Linux 2.6 SMP with standard X11 applications

- First test silicon of the 4 way multiprocessor available now
- Delivering the equivalent of 1.2GHz ARM11 at around 300MHz

  (600mW @130nm process)
- Demonstrating openly available applications dynamically sharing the CPUs and delivering stunning media performance

OS support for ARM11MPCore

- **AMP OS**
  (Communicating kernel Images)
  - Linux
  - uITRON
  - eT-Kernel
  - ThreadX
  - QNX
  - TOPPERS FDMP
  - VxWorks
  - WinCE
  - Nucleus
  - RTXC™
  - etc …..

- **SMP OS**
  (Single kernel image)
  - Linux
  - eT-Kernel
  - ThreadX
  - QNX
  - etc …

Summary

The ARM11 MPCore for general application processor designs featuring:

- **Shorten Time To Market by easing design**
  Easy design of Multi Core by unique CPU interface with Automatic extension of memory & Interrupt system
- **A streamlined and highly efficient implementation of the ARM11 microarchitecture**
  Providing market leading performance for cost sensitive designs with the ability to scale seamlessly into higher performance designs
- **Supporting the latest AMBA 3.0 AXI infrastructure**
  For simplify system interconnect, providing higher data bandwidth, Easier timing closure and reduced design complexity
- **Flexible power management schemes**
  Reducing Energy Consumption, Extend Battery Life and maintaining fan-less operations of designs
- **Software support**
  OS support, Software development tool support for both AMP and SMP configuration

Thank you !