भारतीय प्रौद्योगिकी संस्थान दिल्ली
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REWIRED: Register Write Inhibition by Resource Dedication

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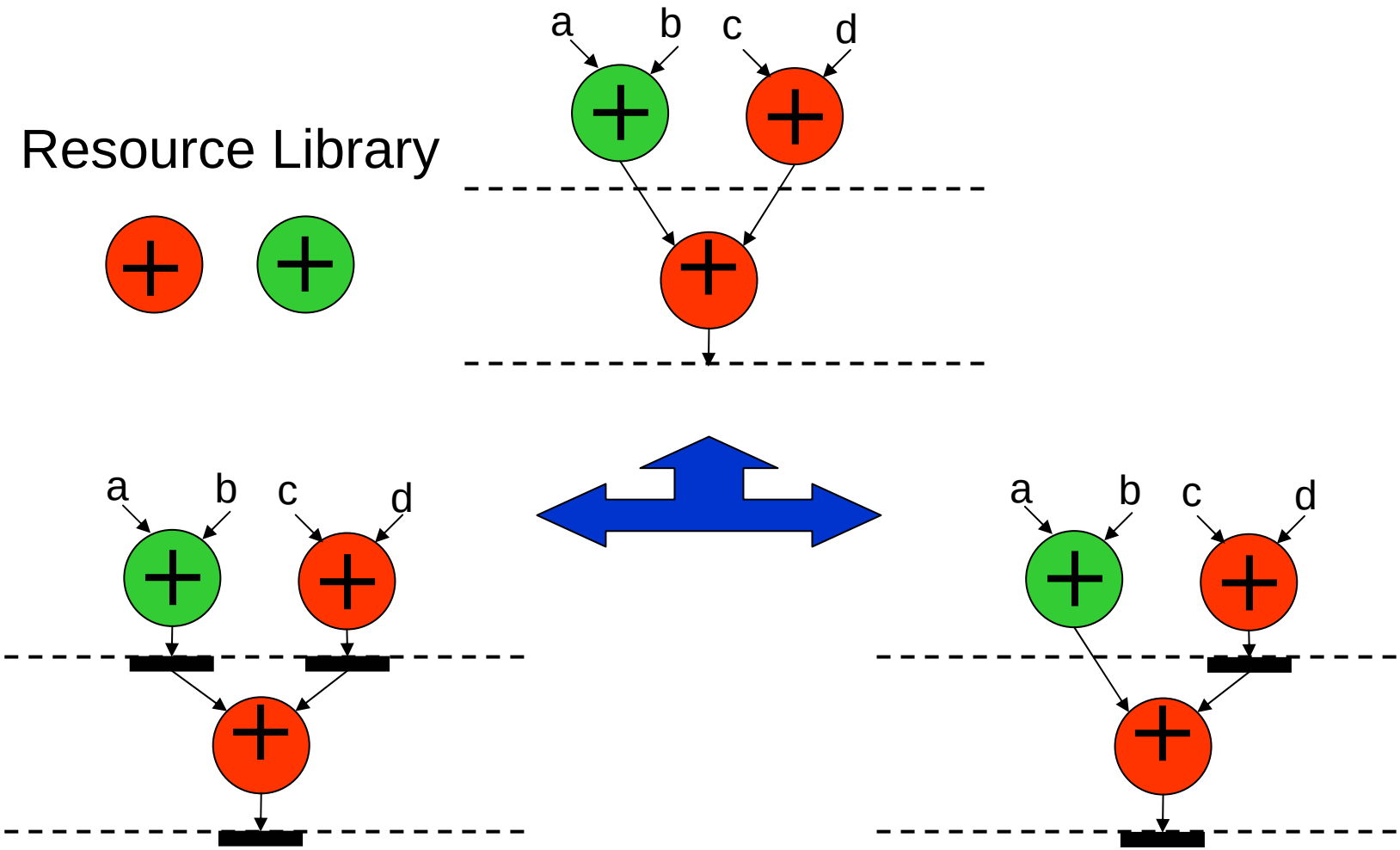
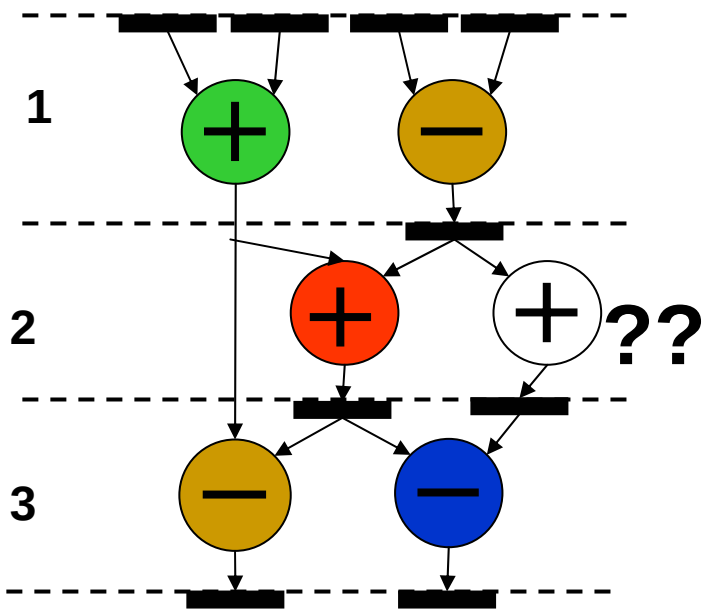
REWIRED: Register Write Inhibition by Resource Dedication

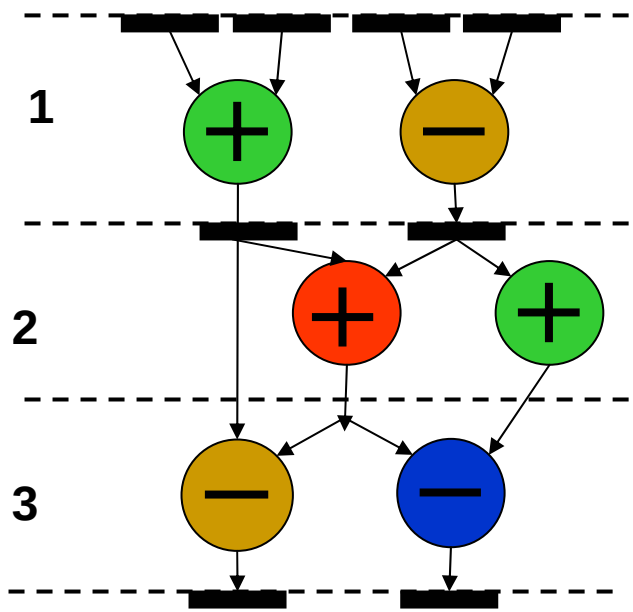
- Low power optimization technique
- Input: Scheduled DFG and a resource library
- Combines Resource and Register allocation
- Lesser register save operations, reduces switching power
- No change in circuit latency or the schedule

Basic Idea



Resource Contention





Optimization Problem: Decide which values need to be stored in registers to avoid resource contention

Problem Formalization

- Remove the maximum number of register write operations and still avoid resource contention
- Good News: Large resource libraries imply high scope for resource dedication
- Bad News: Problem of finding the optimal (largest) set is NP-Complete

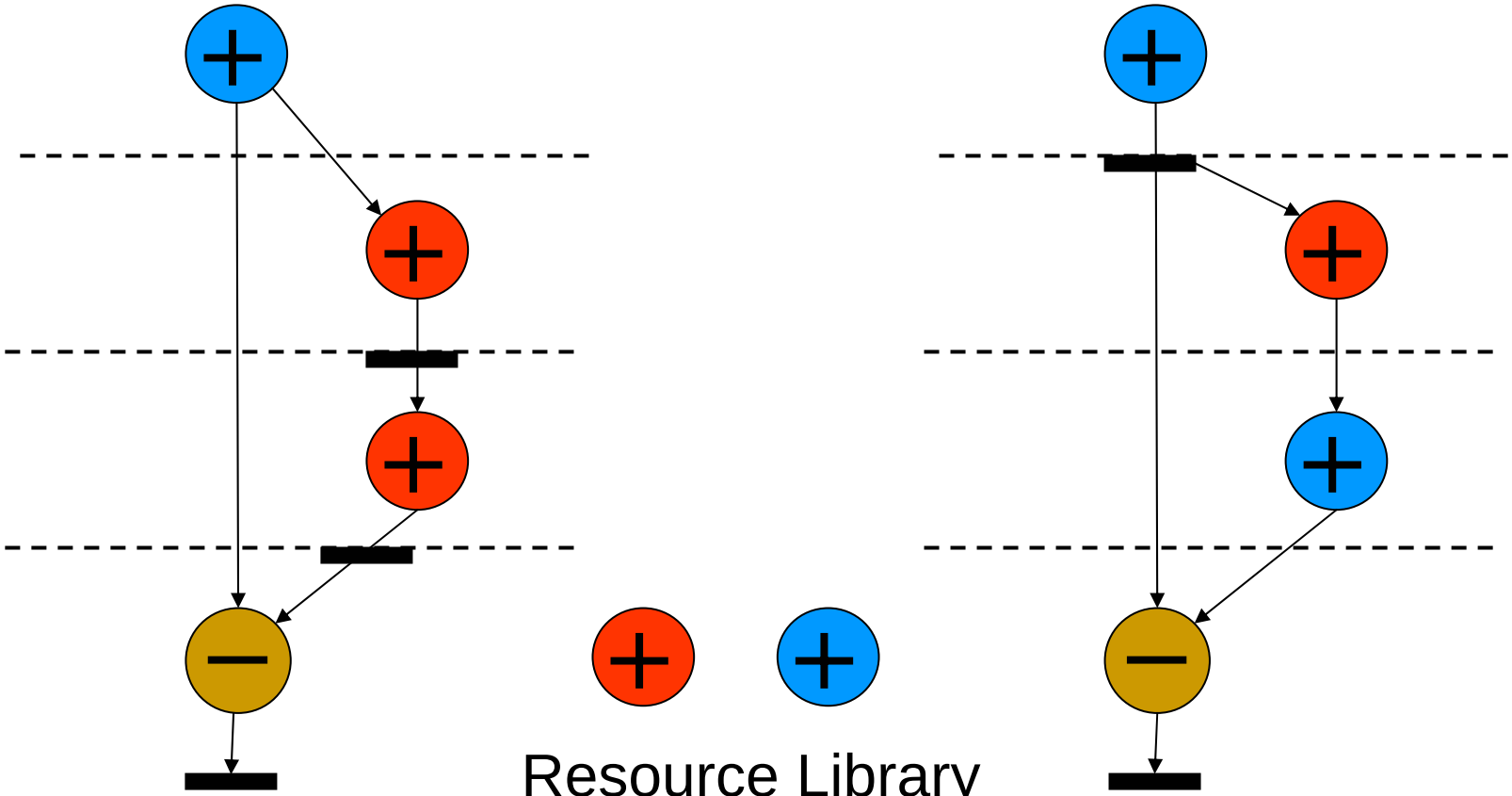
Solution 1: Genetic Algorithm

- Encoding scheme for every valid configuration
- Define the fitness ~ power saving potential of the circuit
- Define cross-over (reproduction) between states and mutation of states
- Wait for the system to stabilize

Solution 2: Fast Heuristic

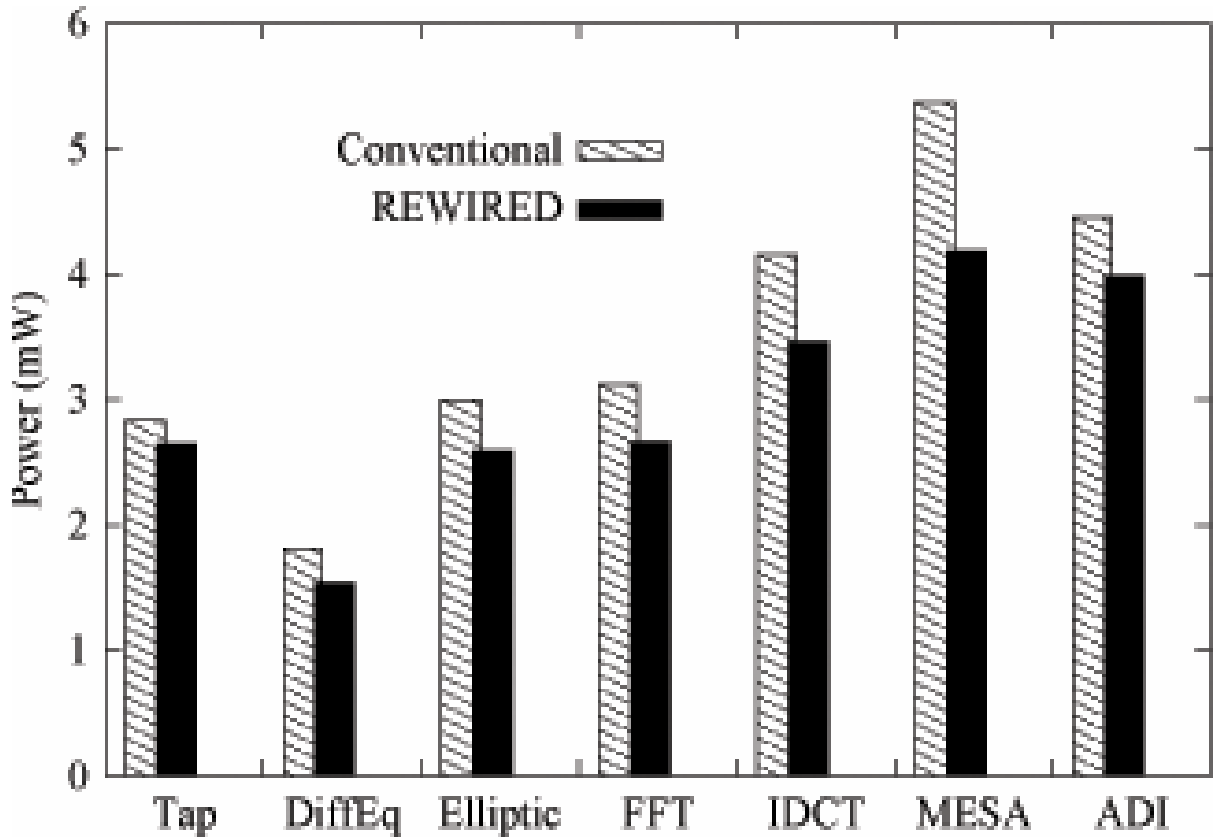
- Greedy heuristic
- Higher priority to operations whose results have small life times.
- Less pressure on resources
- Fewer conflicts
- Avoid resource contention

Fast Heuristic : Example



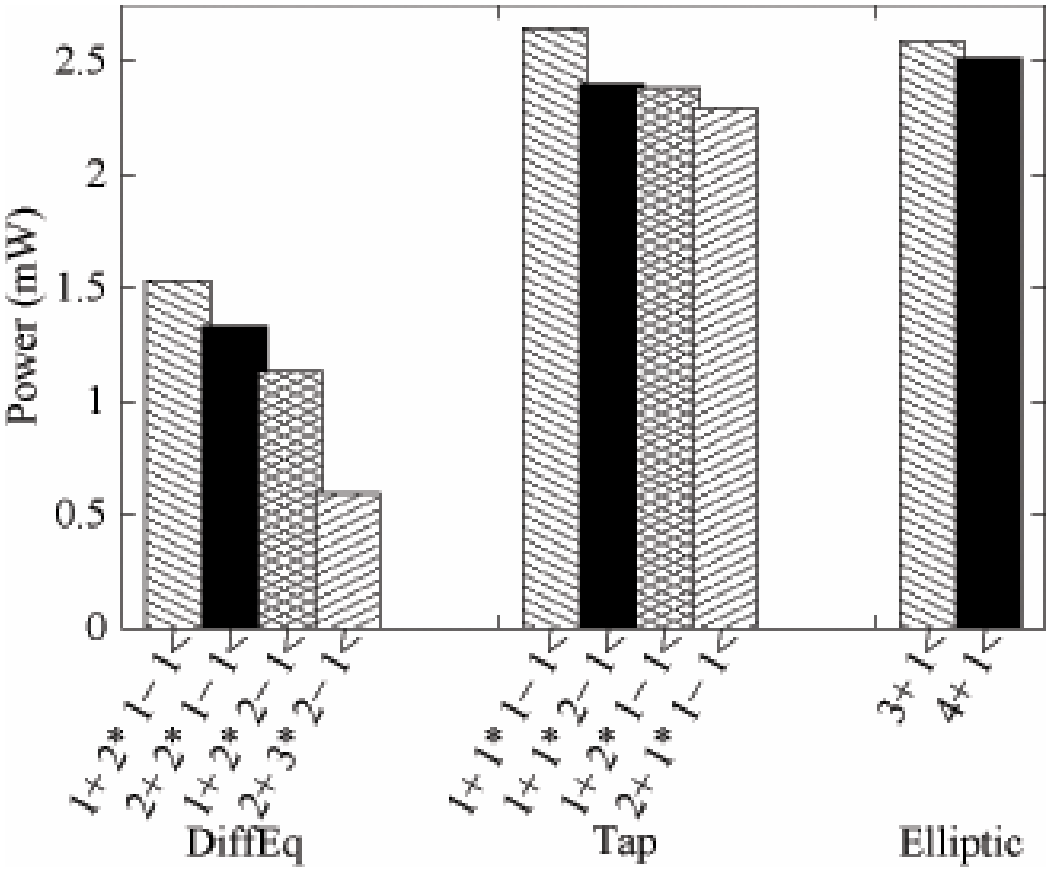
Choosing resources with smaller life times is advantageous

Results(1): REWIRED vs Conventional



- Power reduction of 15 % on an average
- 2 % Area reduction due to simpler control circuits.

Results(2): REWIRED with large resource libraries



- Higher savings with larger resource library

Results(3): Genetic Algorithm vs Heuristic

Application Name	Number of Generations	GA running time (secs)	Heuristic running time
DiffEqn	3000	0:05:39	0.094
TAP	5000	0:07:11	0.136
Elliptic	13000	0:10:42	0.320
FFT	82000	0:44:01	1.323
IDCT	103000	1:05:52	1.125
MESA	77000	0:32:37	1.025
ADI	114000	1:23:18	1.147

Conclusions and Future Work

- REWIRED: Power optimization in HLS by combining register and resource allocation
- 15% power savings
- Future Work
  - Span across basic blocks
  - Revisit scheduling decisions for power aware synthesis
  - Permit schedule latency
  - Leakage Power optimizations

Thank you