A 1.2GHz Delayed Clock Generator for High-speed Microprocessor

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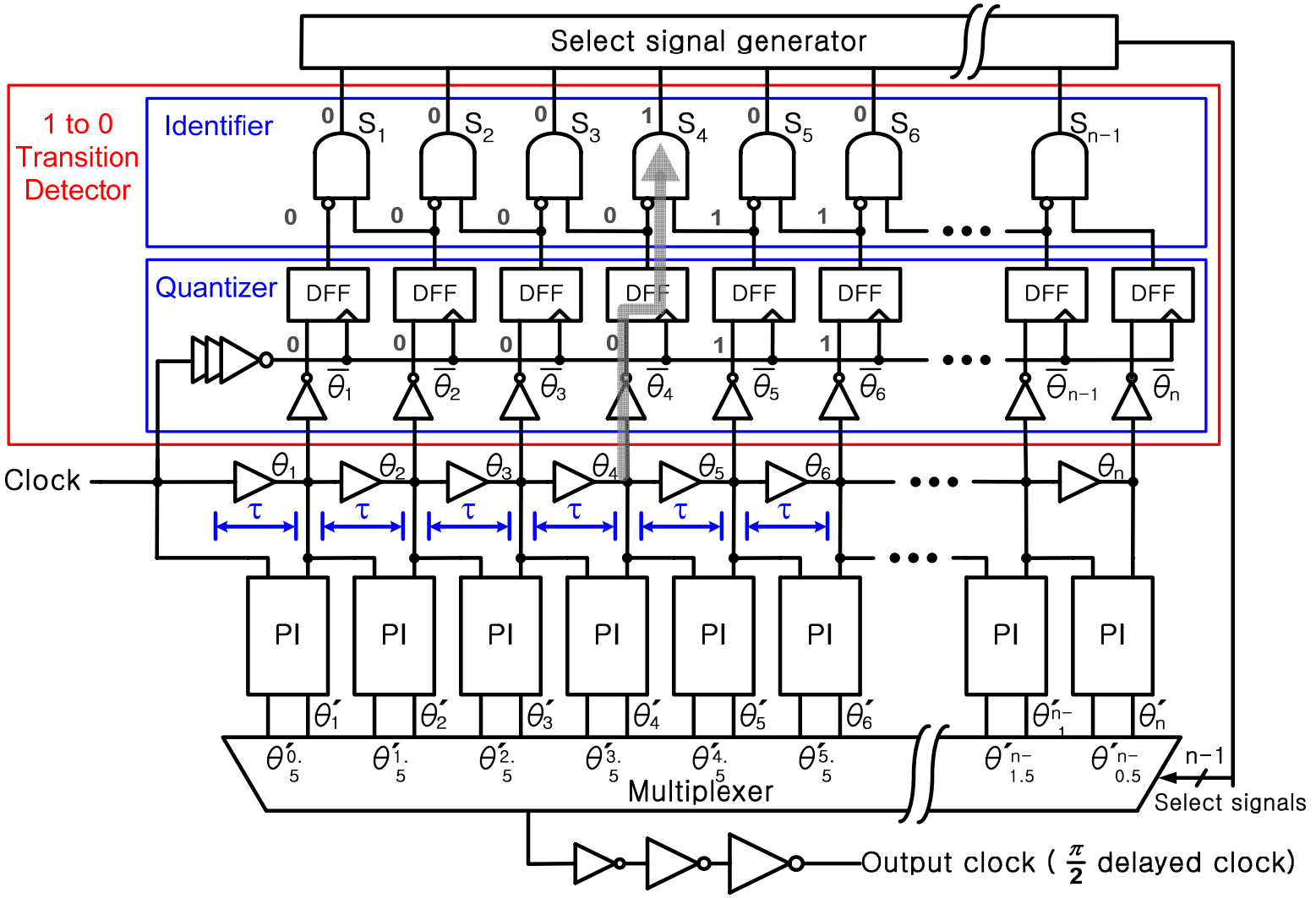
Outline

- **Overall Concept**
- **Building Blocks**
  - Multiphase Clock Generator
  - 1 to 0 Transition Detector
  - Phase Interpolator
  - Select Signal Generator
- **Simulation Results**
- **Measurement Results**
- **Conclusions**

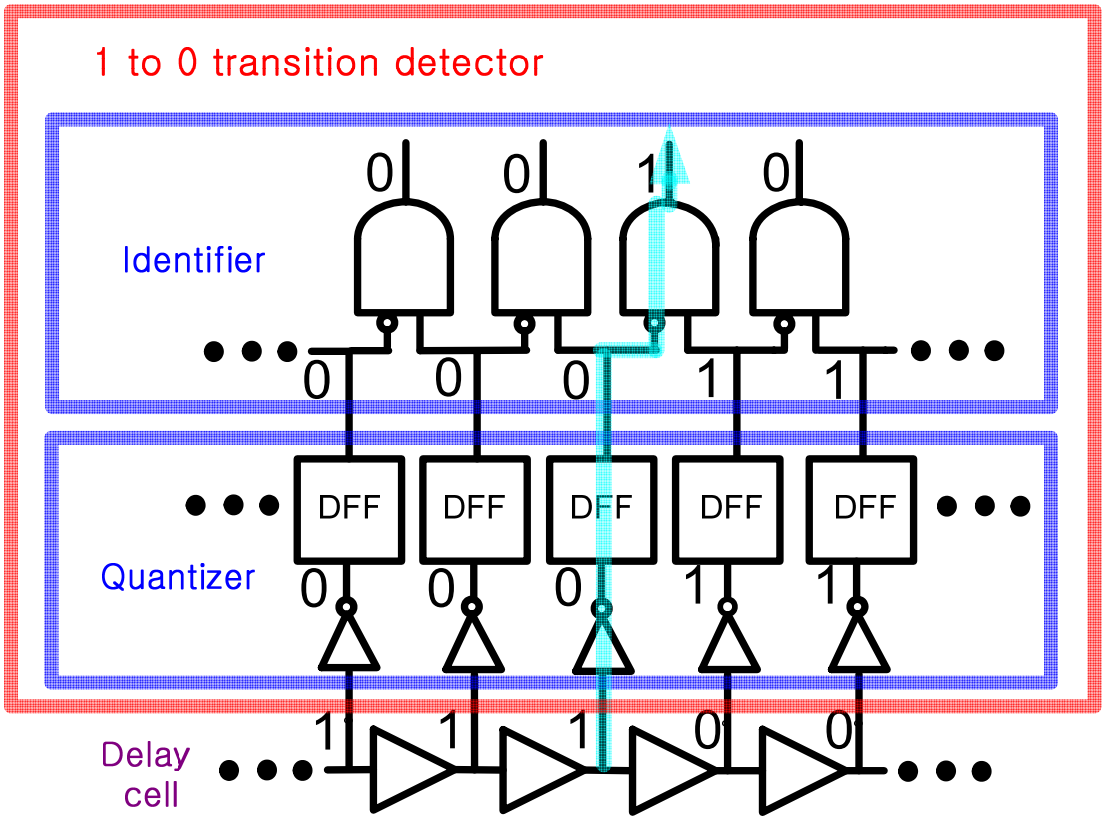
Motivation

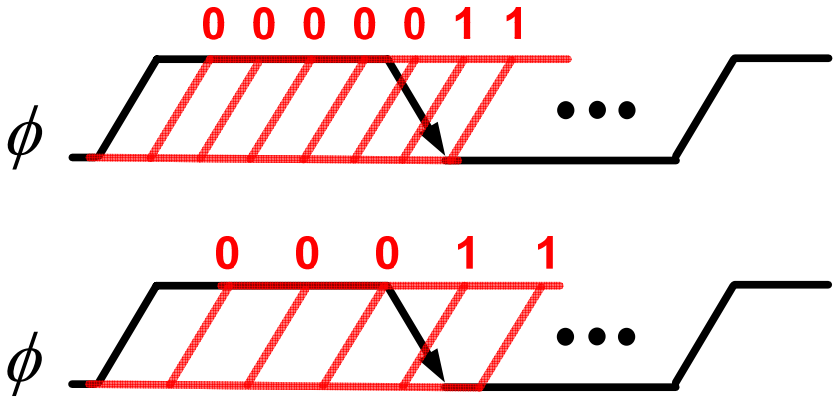
- **1.2 GHz RISC processor**
  - has a main clock generator using PLL
  - Also needs multiphase local delayed clock generator to reduce system-level power consumption
- **A local clock generator requires**
  - single-cycle lock time for clock-on-demand
  - small area to be used in 14 places
  - low power consumption
- **Conventional PLL/DLL and digital clock generators cannot meet all the requirements**

Overall Block Diagram



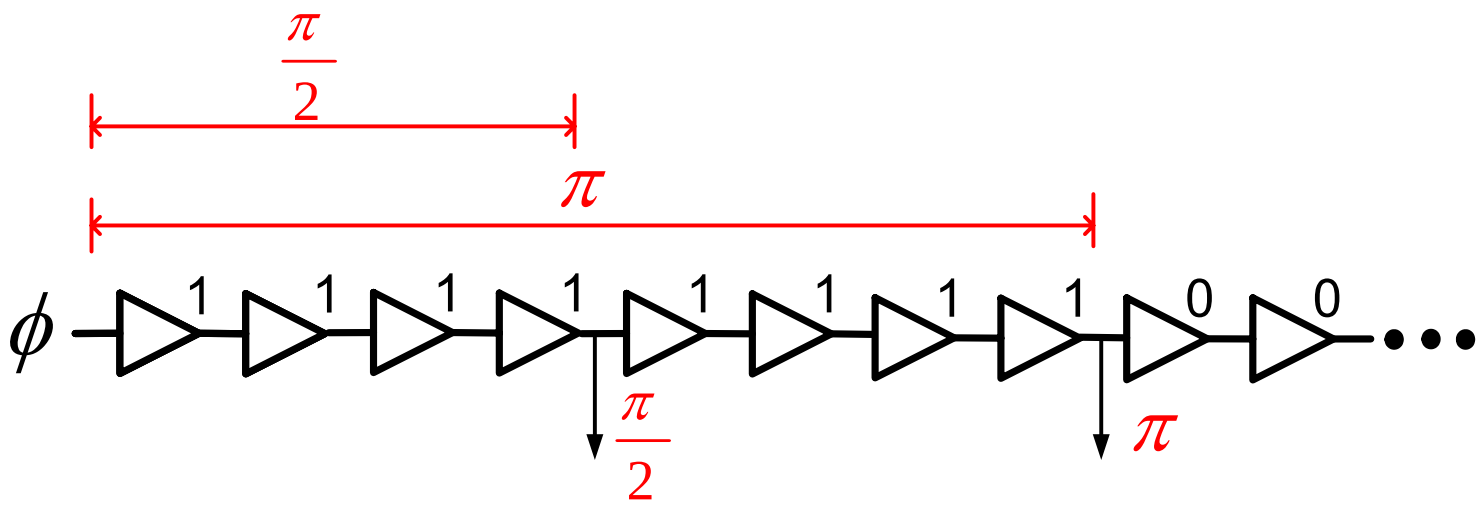
1 to 0 Transition Detector





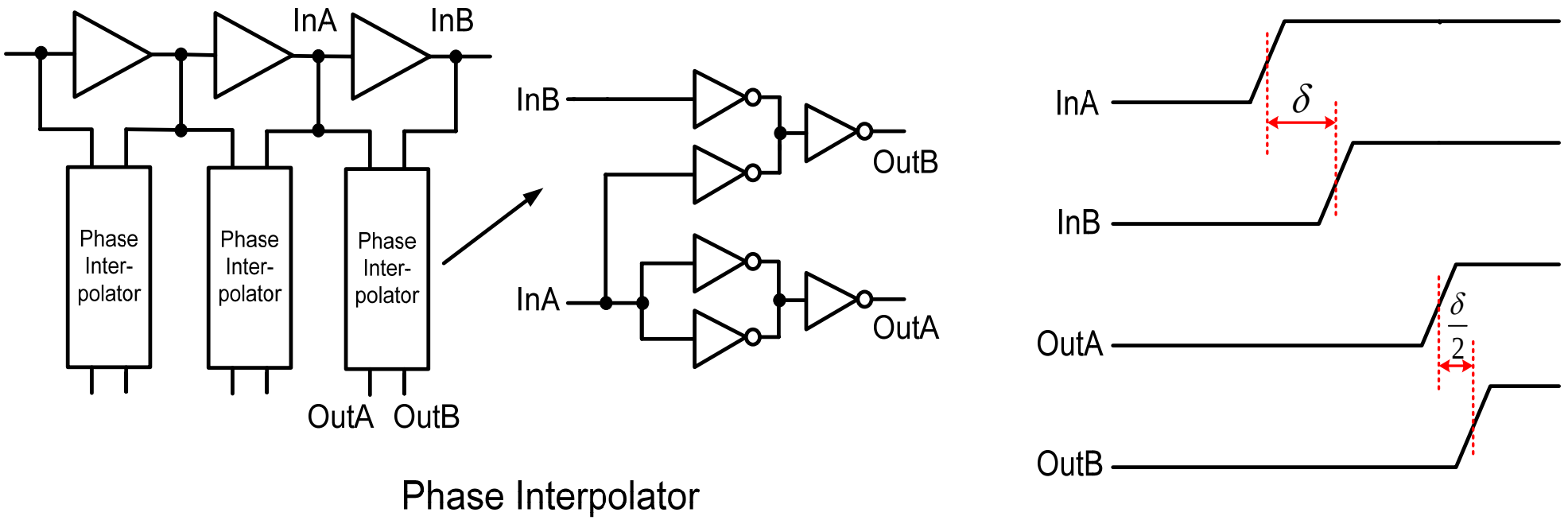
- Consists of quantizer and idetifier.
- Finds a position where data changes from 1 to 0.

Fundamental Idea of Select Signal



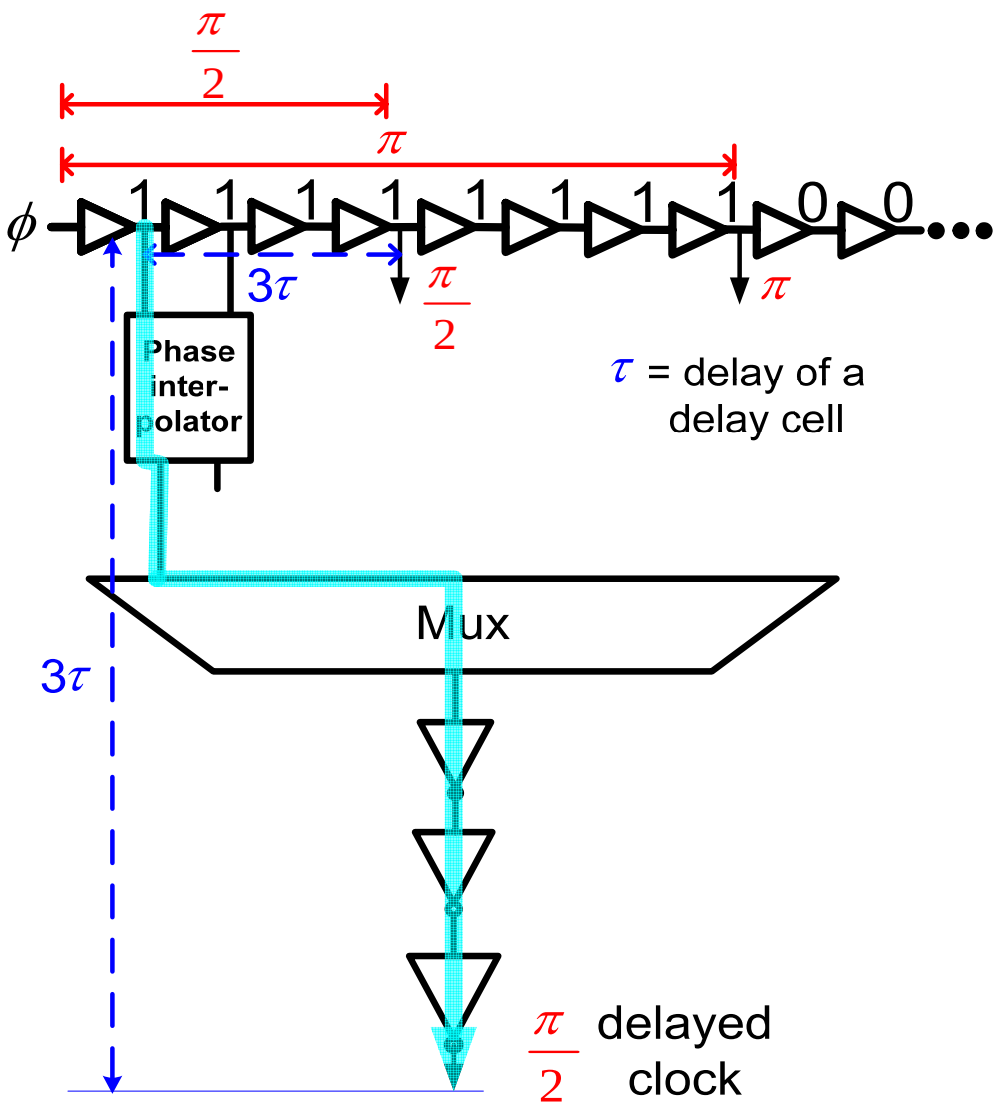
- If 1 to 0 transition detector finds a position of π phase, a position of π/2 phase can be easily determined.
- Half the number of delay cells in π phase points the position of π/2 phase.
- If the number of delay cells within a π phase is odd, interpolated phase is needed.

Phase Interpolator



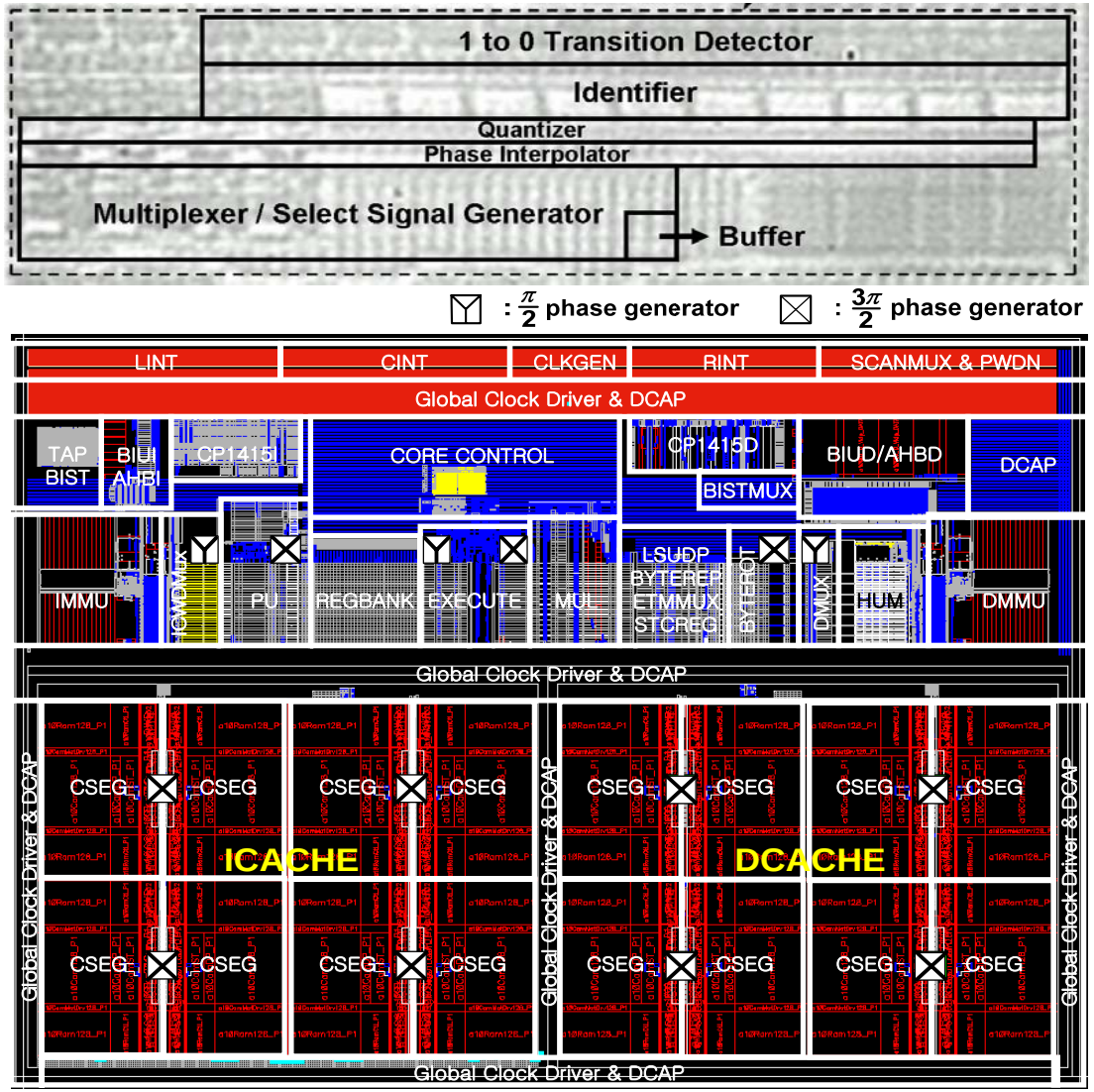
- By proper sizing of inverters, interpolated phase can be achieved.

Shift of Select Signal



- Need to shift select signal to compensate the delay of phase interpolator and mux stages

Die Photo and Layouts of Tile1

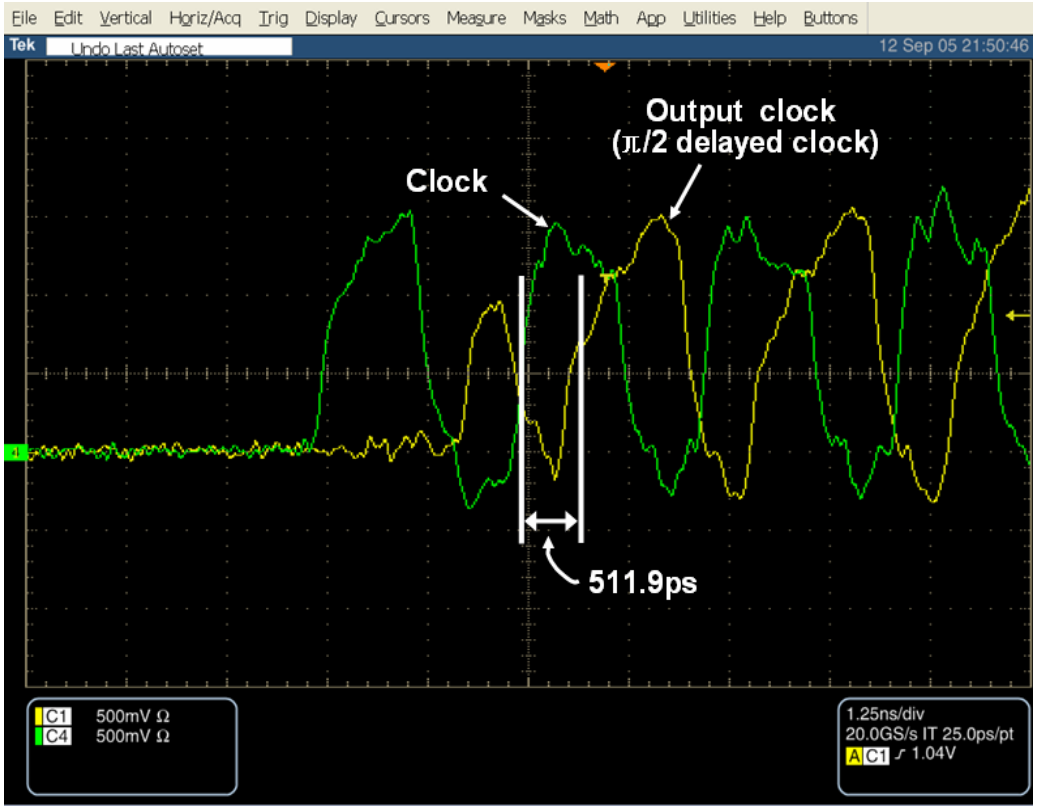


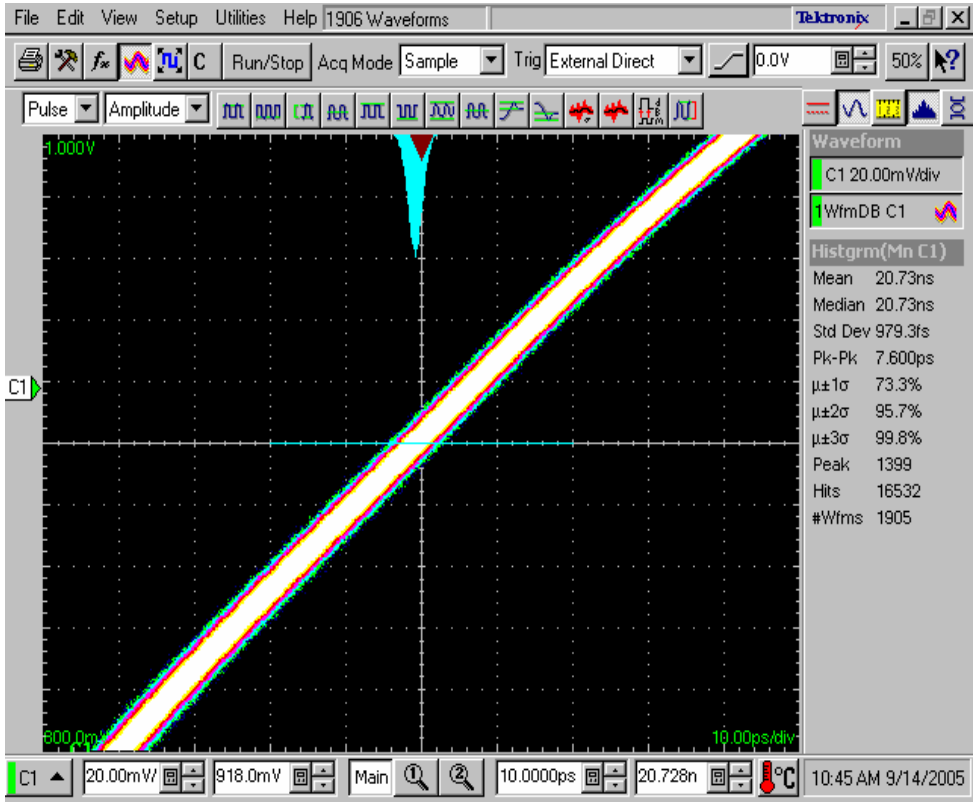
- Die photo of Tile1
  108.5μm x 36.67μm

- Layout of 1.2GHz RISC processor

  Fourteen $\pi/2$ and $3\pi/2$ tiles are used

Measurement Results of Tile2





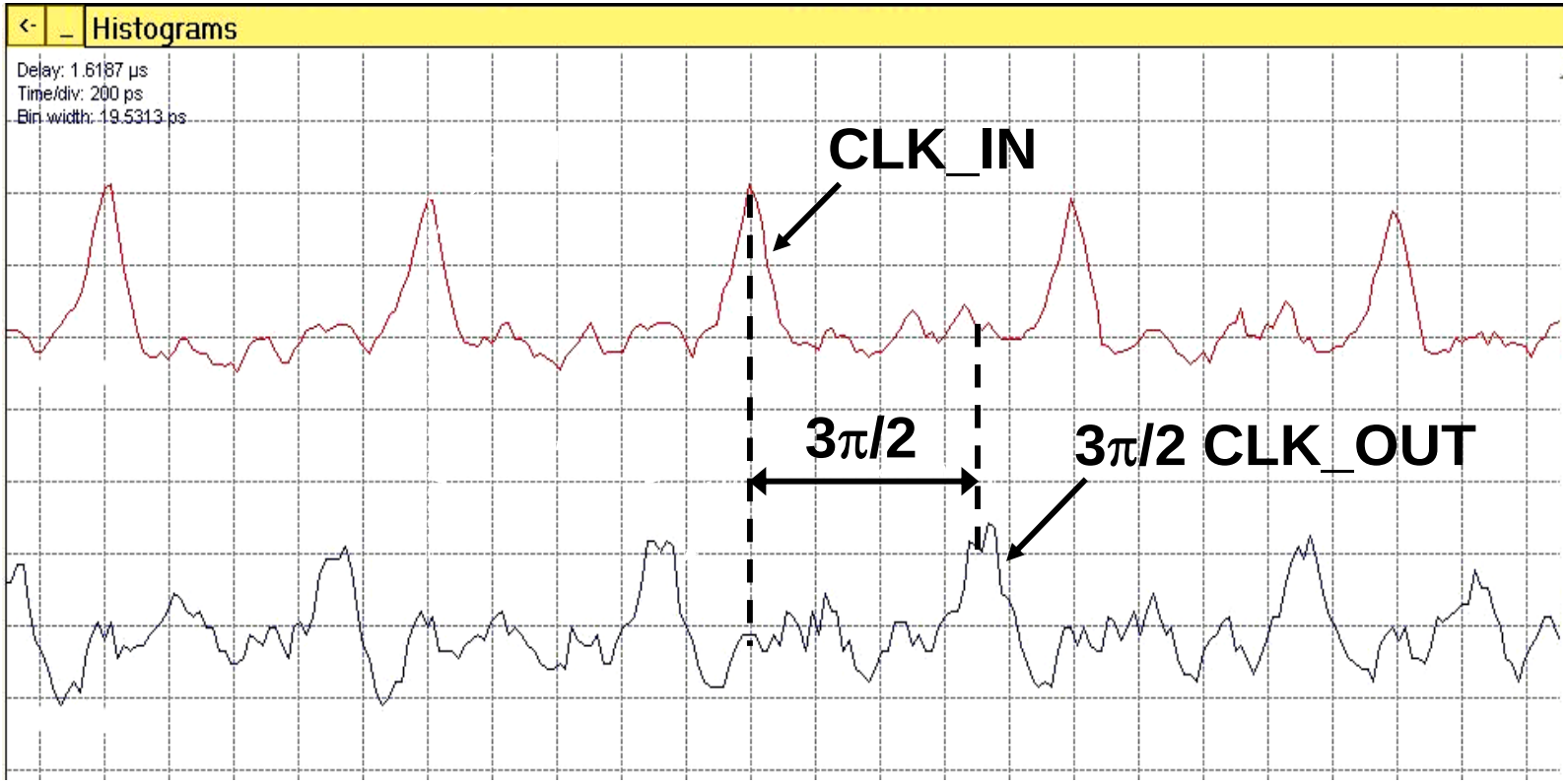
One cycle lock time measurement

Jitter measurement

Peak to peak jitter :

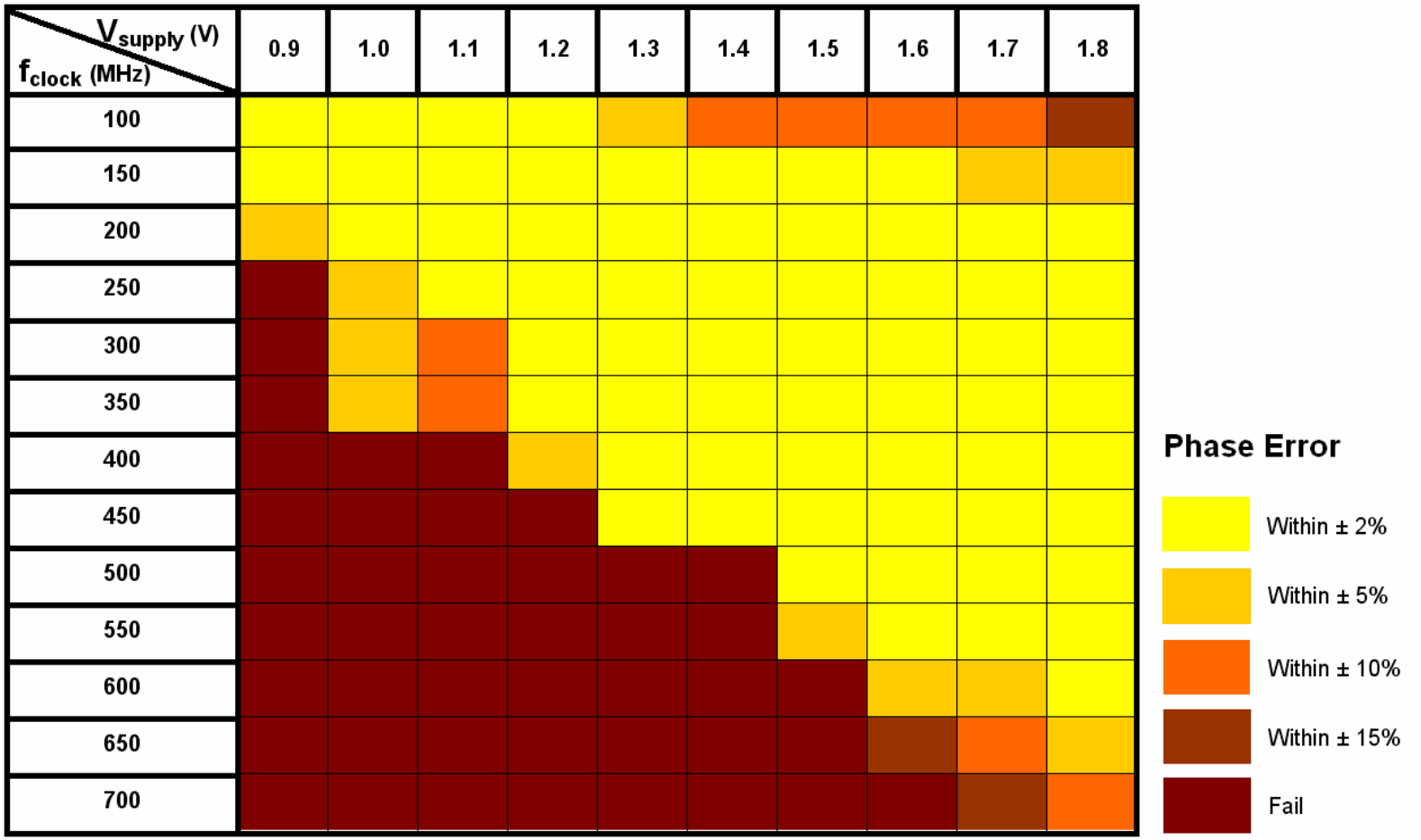
7.60ps @ 500MHz

Measurement Results of Tile1



- Measured by EMI scope
  - Peaks indicate rising edges of the clock signal
- Measurement results at 1GHz

Shmoo Plot of Tile2



- **Operating frequency at 1.8V supply voltage is from 200MHz to 600MHz**

Comparisons

* open loop, † closed loop

Company	Speed (GHz)	Process (um)	Area (mm^2)	Power (mW)	Supply (V)	Jitter (ps)	Phase error
NEC [2]	1.5 ~ 2.8	0.13	0.009	30	1.5	21* 46.8†	±5°
Intel [3]	2.1 ~ 3.5	0.15	0.136	32* 70†	1.6		< 4%* < 8%†
NEC [4]	~ 1.2	0.25	0.140	15@ 2.5V	0.9-2.5	400@ 311MHz	0.29ns
Tile 1	0.625 ~ 1.2	0.13	0.004	3	1.2		< 2%
Tile 2	0.2 ~ 0.6	0.18	0.010	7.48	1.8	7.6@ 500MHz	< 2%
	0.05 ~ 0.15	0.18	0.010	0.518	0.9	30.8@ 150MHz	<2%

Note: [2] and [4] are clock and data recovery applications, and [3] and tiles are for microprocessor applications.

Conclusions

- **Non-PLL/DLL Q-phase clock generator**
  - **Clock on demand (Fast lock time: 1 cycle)**
  - **Smaller area**
  - **Lower power consumption**
  - **No jitter accumulation (Open loop)**

- **All digital gates**
  - **Low voltage operation**
    (achieved via few logic depth)
  - **Portable IP**
  - **Good for time-to-market**
  - **Fewer masks needed**