

Parameterized Embedded In-Circuit Emulator and Its Retargetable Debugging Software for Microprocessor/Microcontroller/DSP Processor

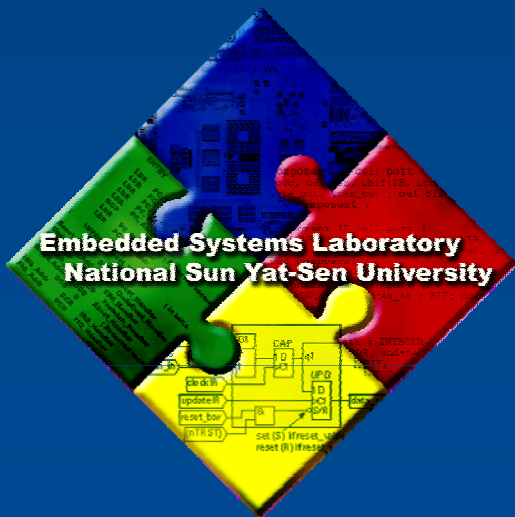
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Introduction to Embedded ICE

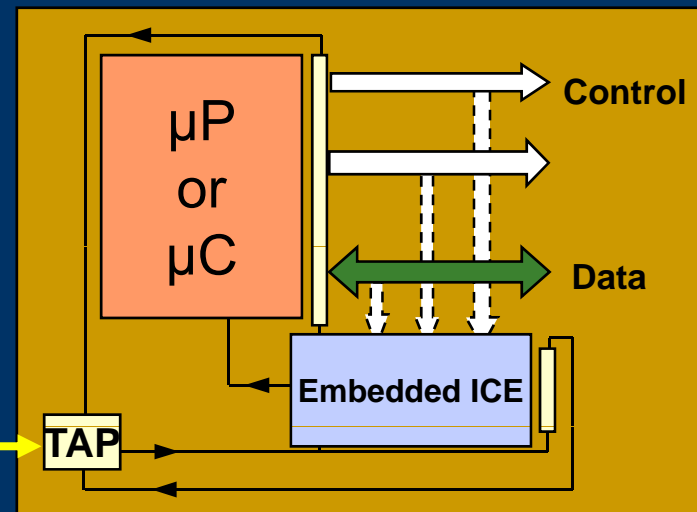
- Preserve the original behavior of a microprocessor
- Embedded ICE contains hardware breakpoint
- Allows instruction breakpoints and data watchpoints to be set
- Programmable through JTAG
- Comparators monitor:
 - Address bus
 - Data bus
 - Control signals
- When there is a match:
 - the processor halts execution
 - the debugger allows the user to view the state of the registers and memory through the JTAG port

Debugger
running on
the host



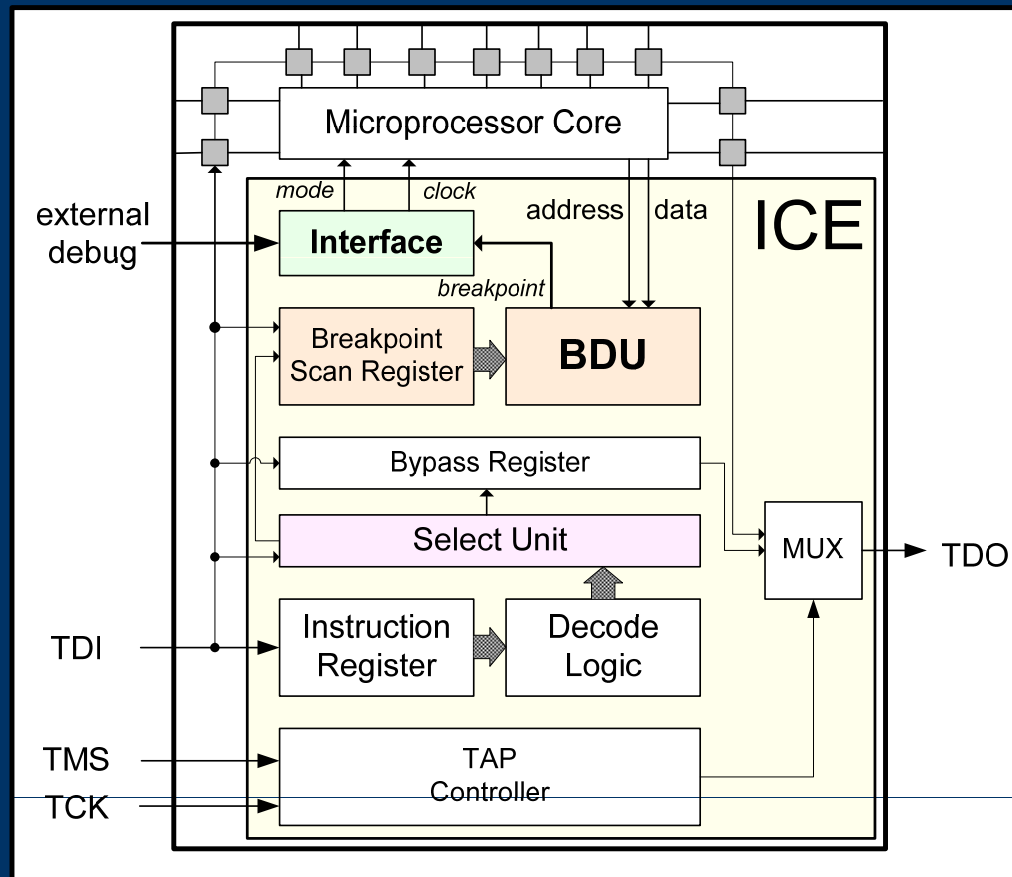
Protocol
Converter

5 wire
JTAG



Block Diagram for the Embedded ICE

- Our EICE is based on IEEE 1149.1 with some extensions



JTAG Extensions to Support the EICE Functionality

- Component Modification

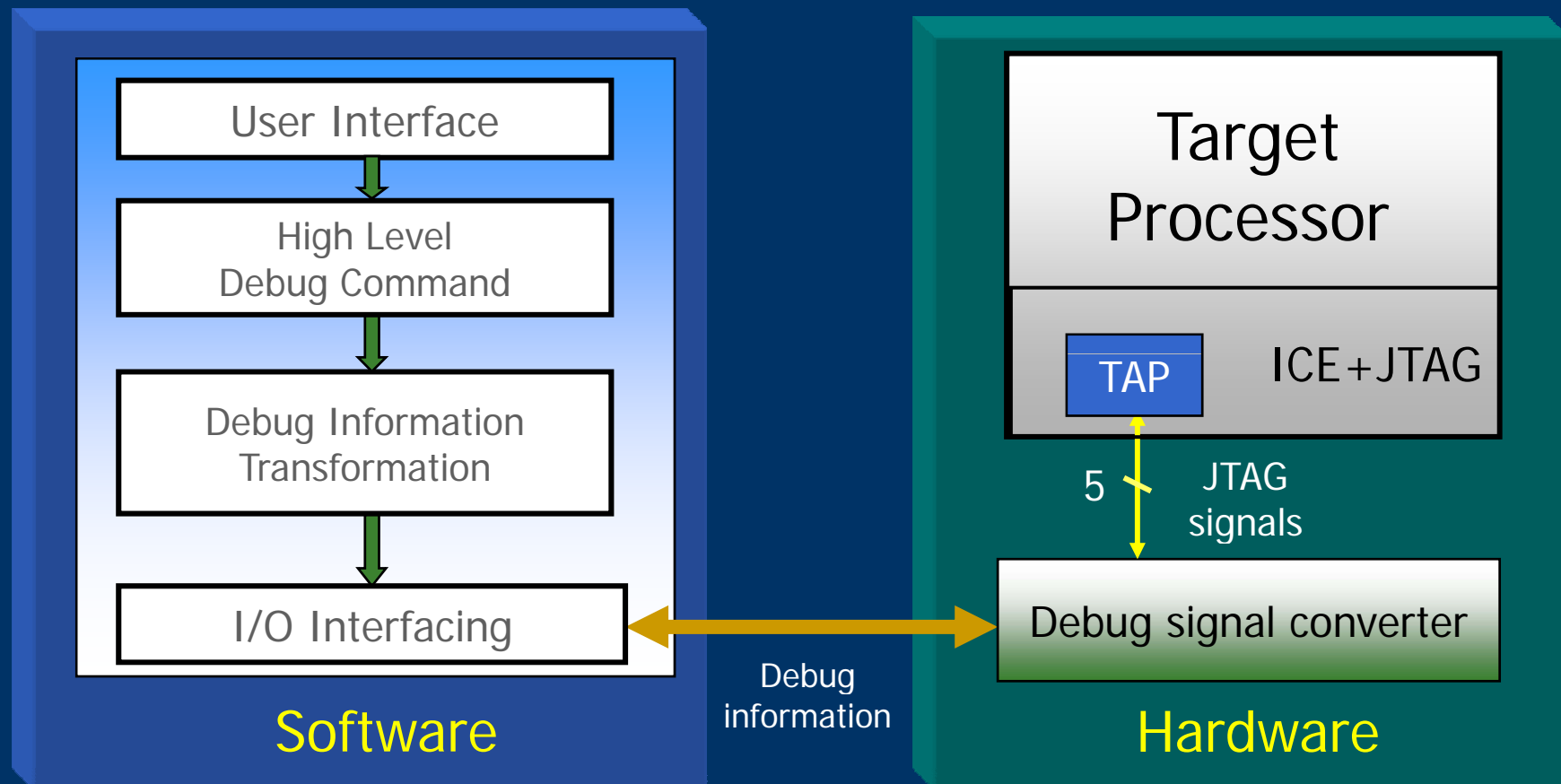
Classification	Components
Original 1149.1 JTAG components	TAP controller, Boundary Scan Registers, Bypass Register
Modified 1149.1 JTAG components	Instruction Register, Instruction Decode Logic, Data Register Selector
New Components	Core Data Register, Breakpoint Scan Register, Scan-Chain Select Register, Breakpoint Detection Unit

Feature

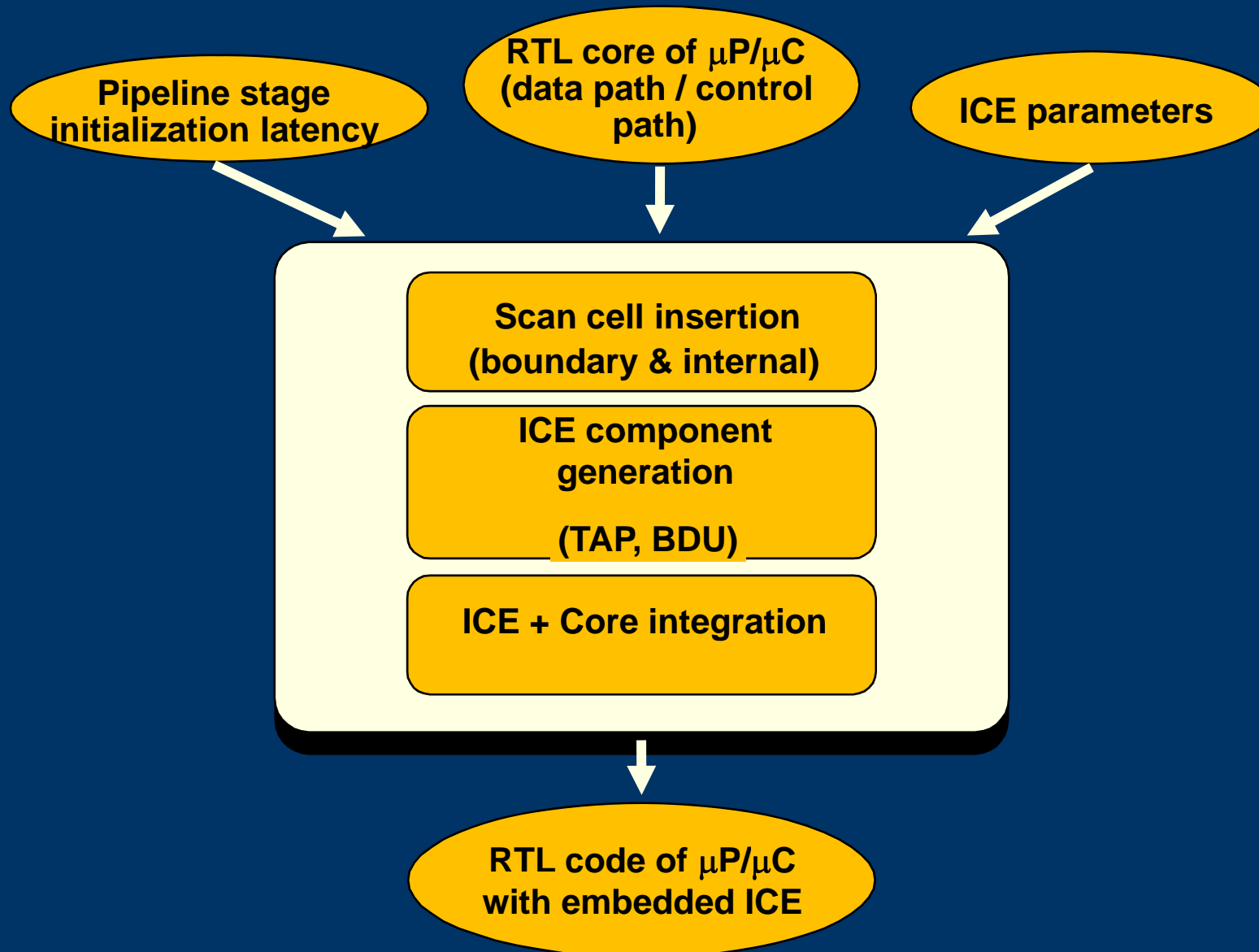
- Reusable ability to Reduce HW/SW Development Cost
 - In general, EICEs are designed for specific targets.
 - Our design can be applied different processors
- Easy to Integrate Embedded ICE IP into Processor

Proposed approach

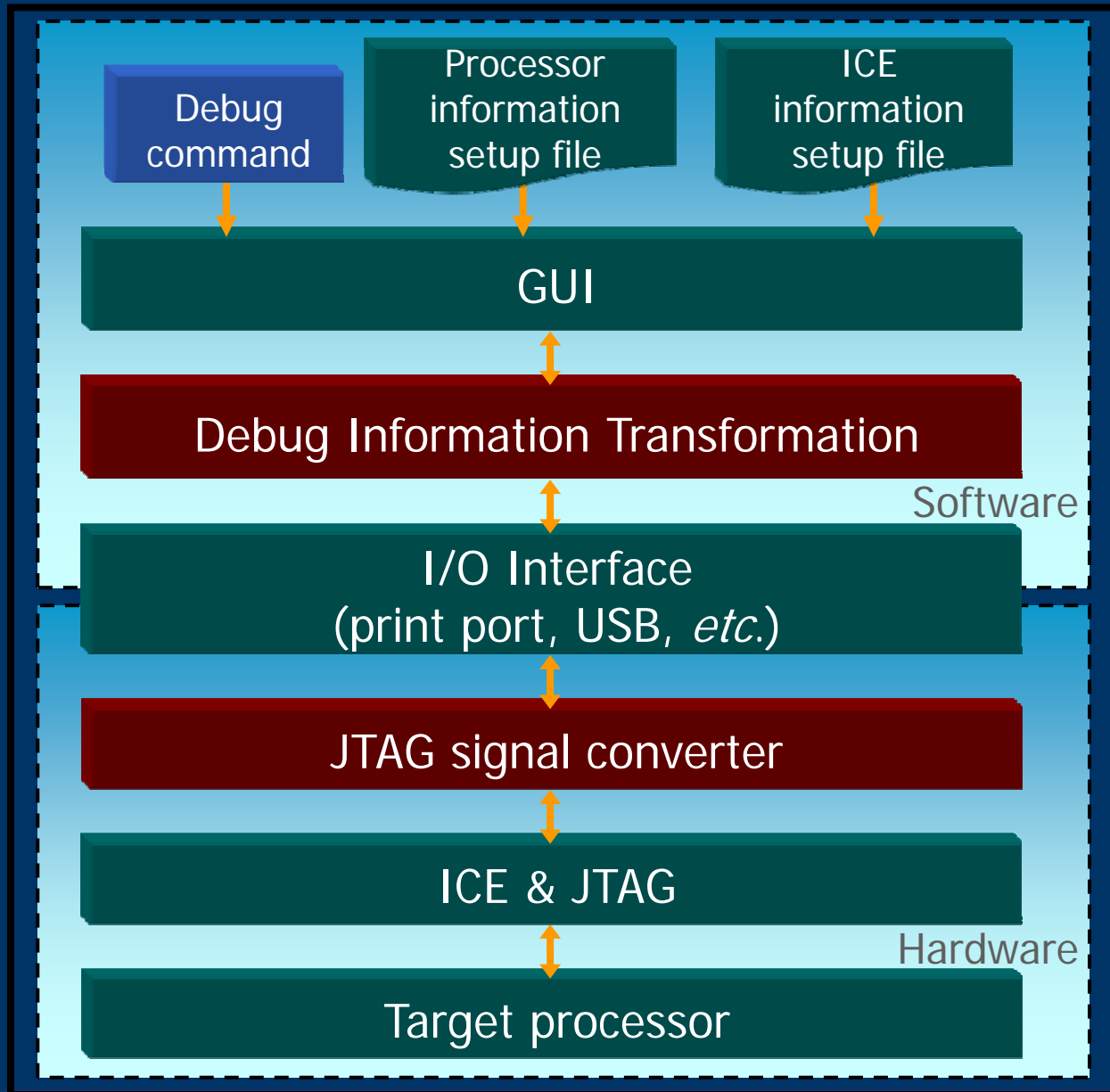
- HW/SW co-generate the debugging information



μ P/ μ C + ICE Integration Flow



Retargetable EICE debugging software



Integration Consideration

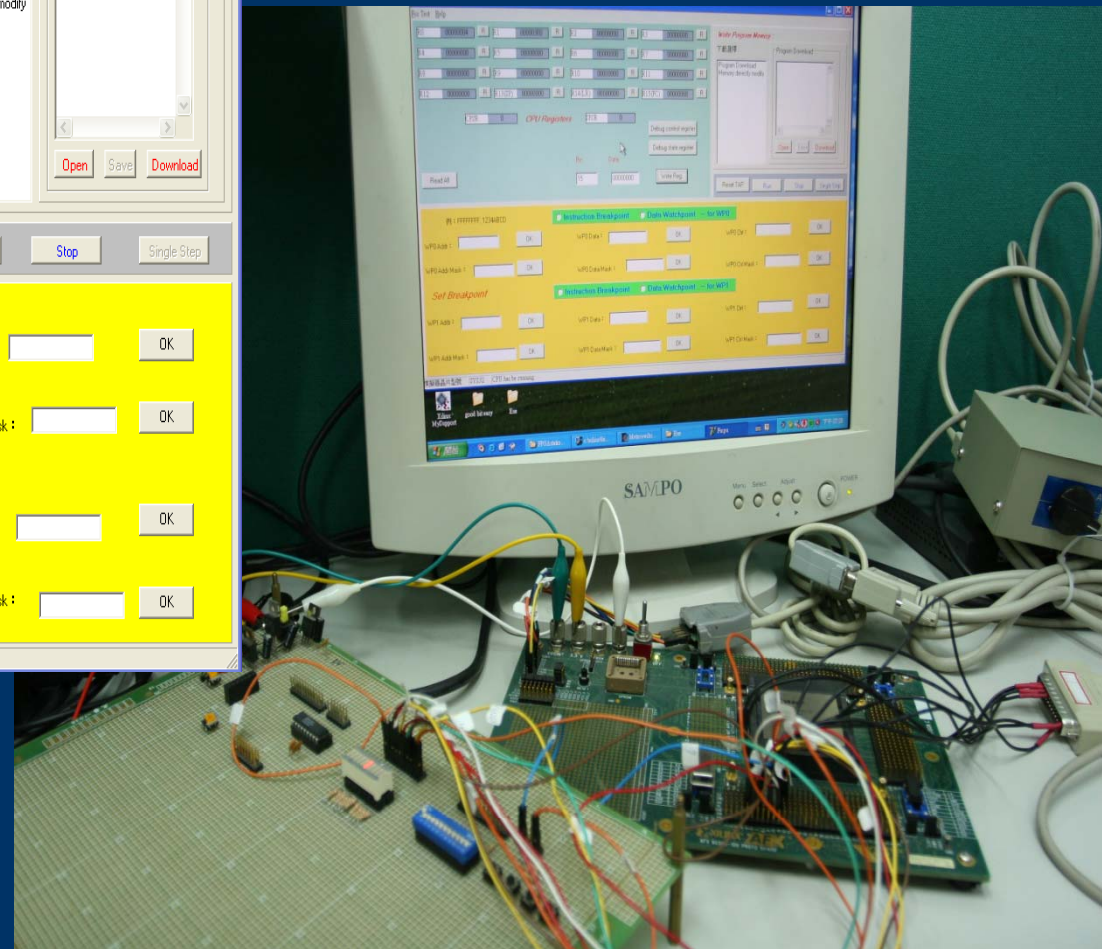
- Interface between microprocessor and ICE
- Insertion of internal scan cells
- Define test data registers
- Breakpoint scan register
- Breakpoint detection unit
- Test data register selection method
- JTAG instructions extension
- Instruction decoder modification

Applications of the Retargetable ICE

- with 8-bit μ C:
 - HT48100 (FPGA, chip) ...**Holtek**
- with 32-bit μ P:
 - Academic ARM7-like CPU core (SYS32TM Series) (FPGA, chip) ...**NSYSU**
 - SPARC-like core (RTL) ...**ACard**
 - K310 CPU (in progress) ...**Himax**
- With DSPs:
 - PAC DSP (FPGA, chip) ...**ITRI-STC**,
 - “Q” DSP (in progress) ...**Himax**

Prototyping for Our Designed Environment

The screenshot shows the STS32 ICE software interface. At the top, there's a menu bar with 'For Test' and 'Help'. Below it, a grid of CPU registers (R0 to R15) is displayed, each with a value of 0. The CPU Registers section includes CPSR and SPSR fields, both set to 0. A 'Write Program Memory' dialog box is open, showing a 'Program Download' list and buttons for 'Open', 'Save', and 'Download'. Below the registers, there are 'Read All', 'Write Reg.', 'Run', 'Stop', and 'Single Step' buttons. At the bottom, there are sections for setting breakpoints and watchpoints, with 'Instruction Breakpoint' and 'Data Watchpoint' selected. The example address is 'FFFFFFF, 1234ABCD'. The status bar at the bottom shows '模擬器晶片型號 STS32'.



Prototyping for ARM Development Environment

The screenshot shows an ARM development environment with the following assembly code in the main window:

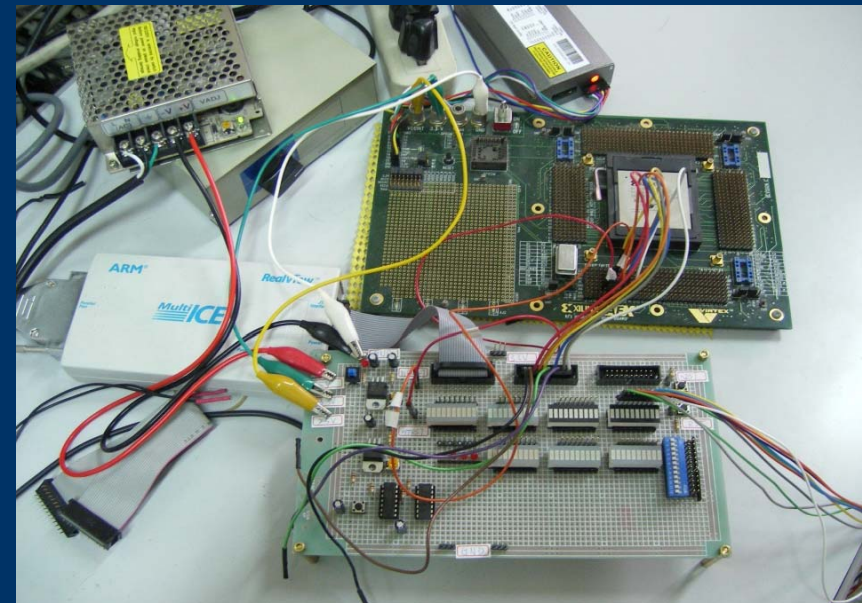
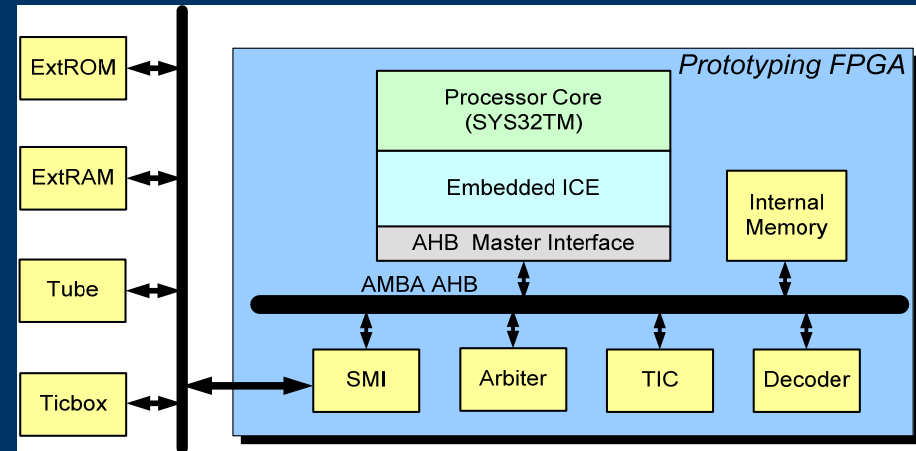
```
0000042C E3A0B01B MOV r11,#0x1b
00000430 E3A0C01C MOV r12,#0x1c
00000434 E3A0D01D MOV r13,#0x1d
00000438 E1A00000 NOP
0000043C E3A00011 MOV r0,#0x11
00000440 E3A01012 MOV r1,#0x12
00000444 E3A02013 MOV r2,#0x13
00000448 E3A03014 MOV r3,#0x14
0000044C E3A04015 MOV r4,#0x15
00000450 E3A05016 MOV r5,#0x16
00000454 E3A06017 MOV r6,#0x17
00000458 E3A07018 MOV r7,#0x18
0000045C E3A08019 MOV r8,#0x19
00000460 E3A0901A MOV r9,#0x1a
00000464 E3A0A01B MOV r10,#0x1b
00000468 E3A0B01C MOV r11,#0x1c
0000046C E3A0C01D MOV r12,#0x1d
00000470 E3A0D01E MOV r13,#0x1e
00000474 E1A00000 NOP
00000478 E3A00012 MOV r0,#0x12
0000047C E3A01013 MOV r1,#0x13
00000480 E3A02014 MOV r2,#0x14
```

The registers window shows the following state:

R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	SP	LR	PC	CPSR
00000011	00000012	00000013	00000014	00000015	00000015	00000016	00000017	00000018	00000019	0000001A	0000001B	0000001C	0000001D	00000454	0000044C	00000010

The status window shows:

Type	Value
ARM7TDMI_r1	PC=0x0000044C
Image	<None>



Conclusion

- We propose a parameterized embedded in-circuit emulator and its retargetable debugging software in order to reduce the debugging design procedure time for different target systems.
- The goal is to integrate the EICE component into the microcontroller/microprocessor/DSP processor, and to execute debugging functions via proposed retargetable GUI debugger tool.
- As a result of it, the duration of debugging procedure and time-to-market is reduced.