LVDS-type On-Chip Transmission Line Interconnect with Passive Equalizers in 90 nm CMOS Process

Akiko Mineyama[1], Hiroyuki Ito[2], Takahiro Ishii[1], Kenichi Okada[1], and Kazuya Masu[1]

[1]Integrated Research Institute, Tokyo Institute of Technology

[2]Precision and Intelligence Laboratory, Tokyo Institute of Technology

Masu Group
Tokyo Tech

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Backgrounds

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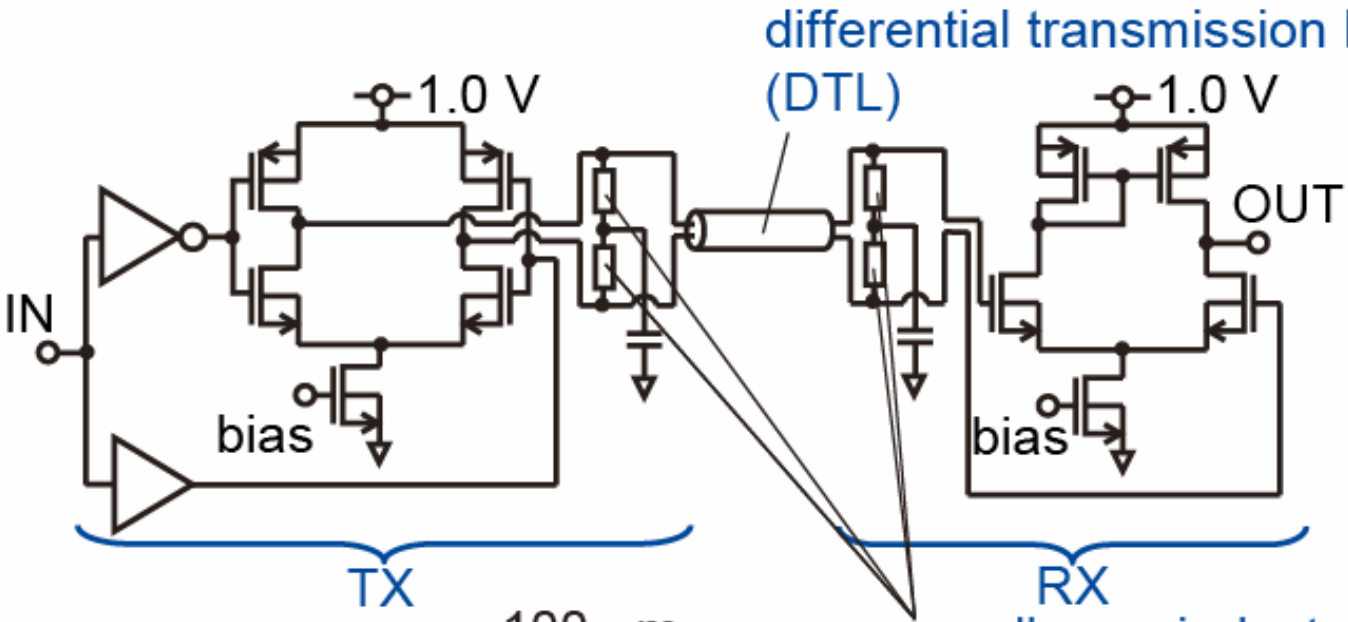
- Miniaturization of Si CMOS
  - Increase in global interconnect delays
    - Complicates timing designs
    - Limits LSI performances
- Transmission line interconnects[1]
    - Much smaller delay than conventional lines
    - High power-efficiencies at high-speed signaling

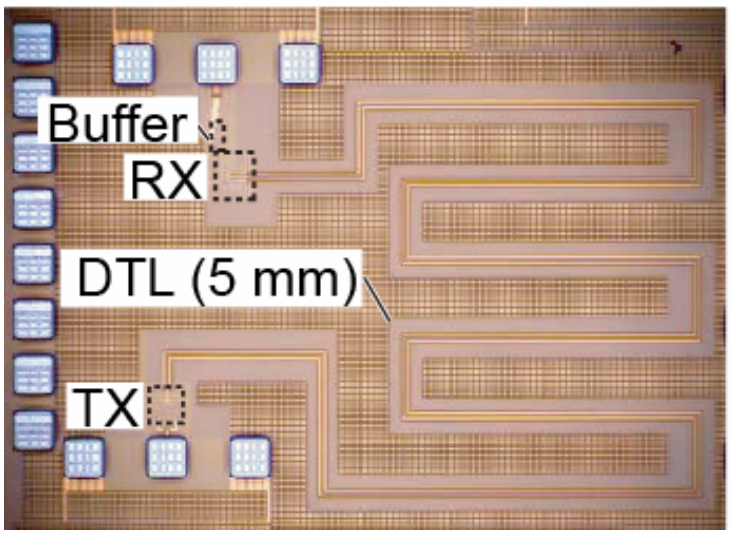
Purpose

To propose a low-voltage-differential-signaling (LVDS) type transmission line interconnect for achieving higher speed and higher power-efficiency

[1]R. T. Chang, *et al*., IEEE JSSC, vol. 38, no. 5, pp. 834-838, May 2003.

The proposed DTL interconnect





90 nm CMOS process

Total area of TX and RX is11,100 μm^2

Measurement results

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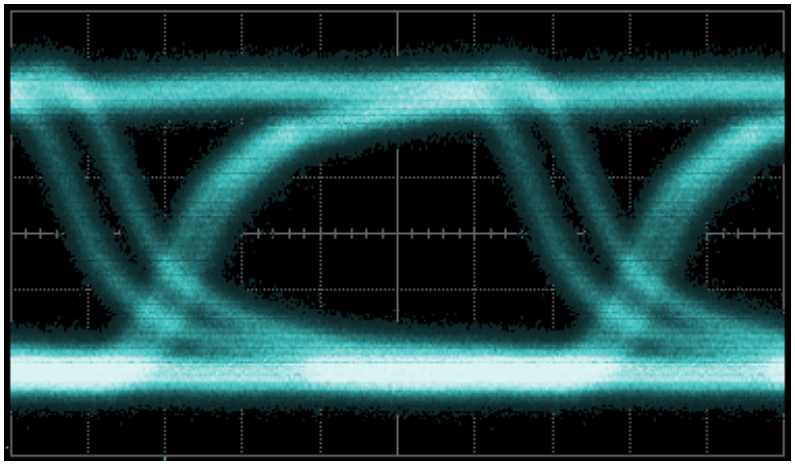
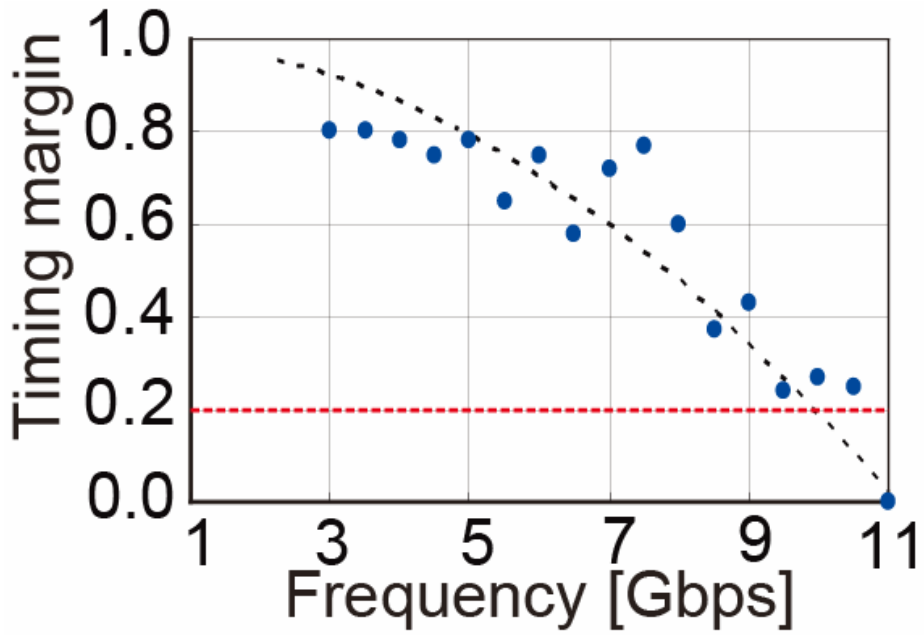


10.5 Gbps

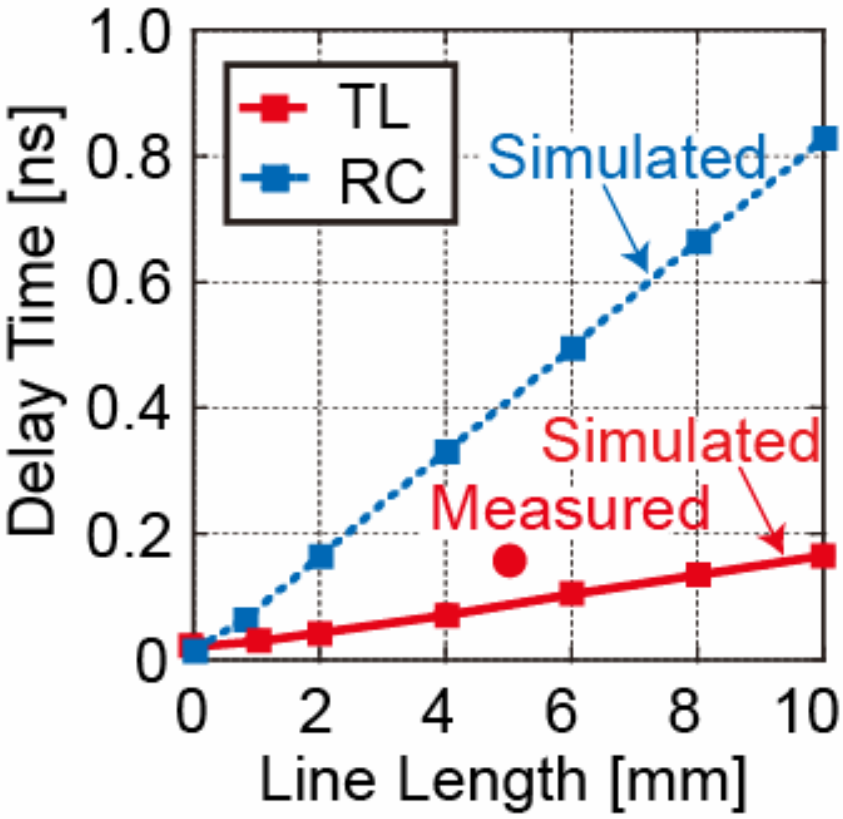
15.9 mV / div
15.9 ps / div

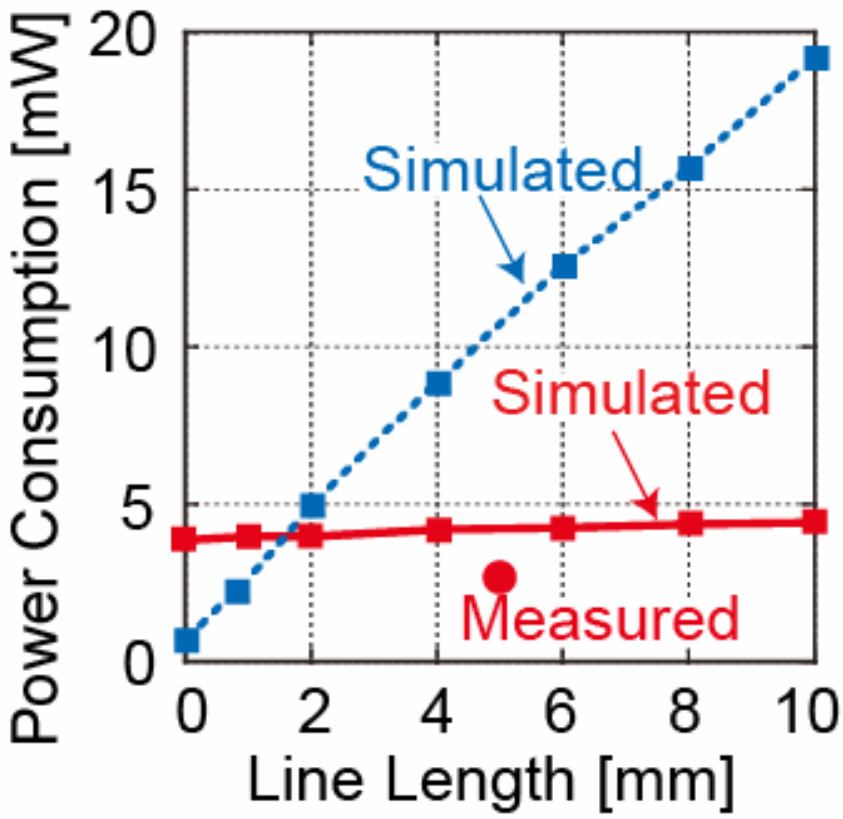


Process	90 nm standerd Si CMOS
The maximum frequency	10.5 Gbps
Average delay of 23 chips	173 ps / 5 mm
Power consumption (V_{DD}=1V, 10Gbps)	TX : 1.9 mW, RX : 0.8 mW Total : 2.7 mW
Energy per Bit	0.25 pJ / bit

* Eye-width margin is assumed to be over 20% of period at BER of 10^{-12}.

Comparison of delay and power



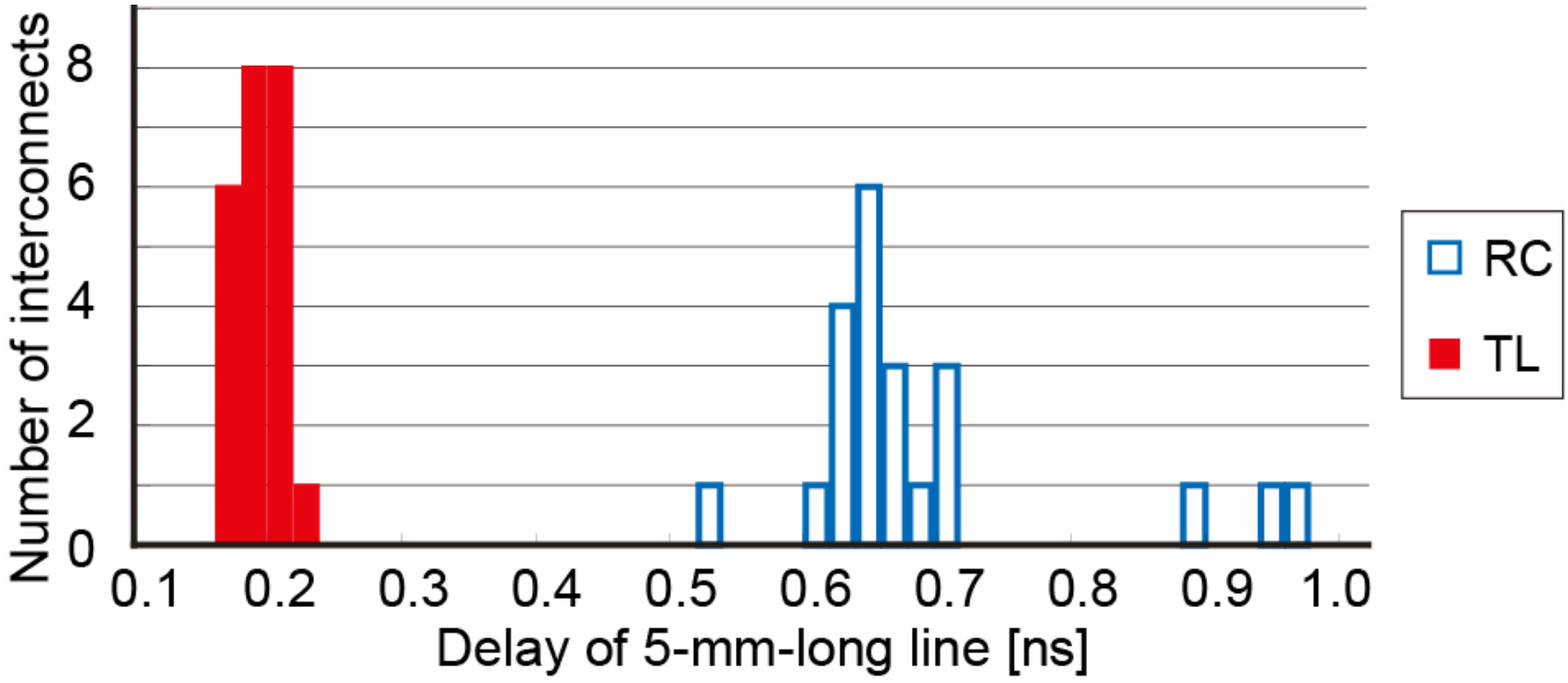


- The transmission line interconnect

  Shorter delay and smaller power consumption than the so-called RC line as the line length increases

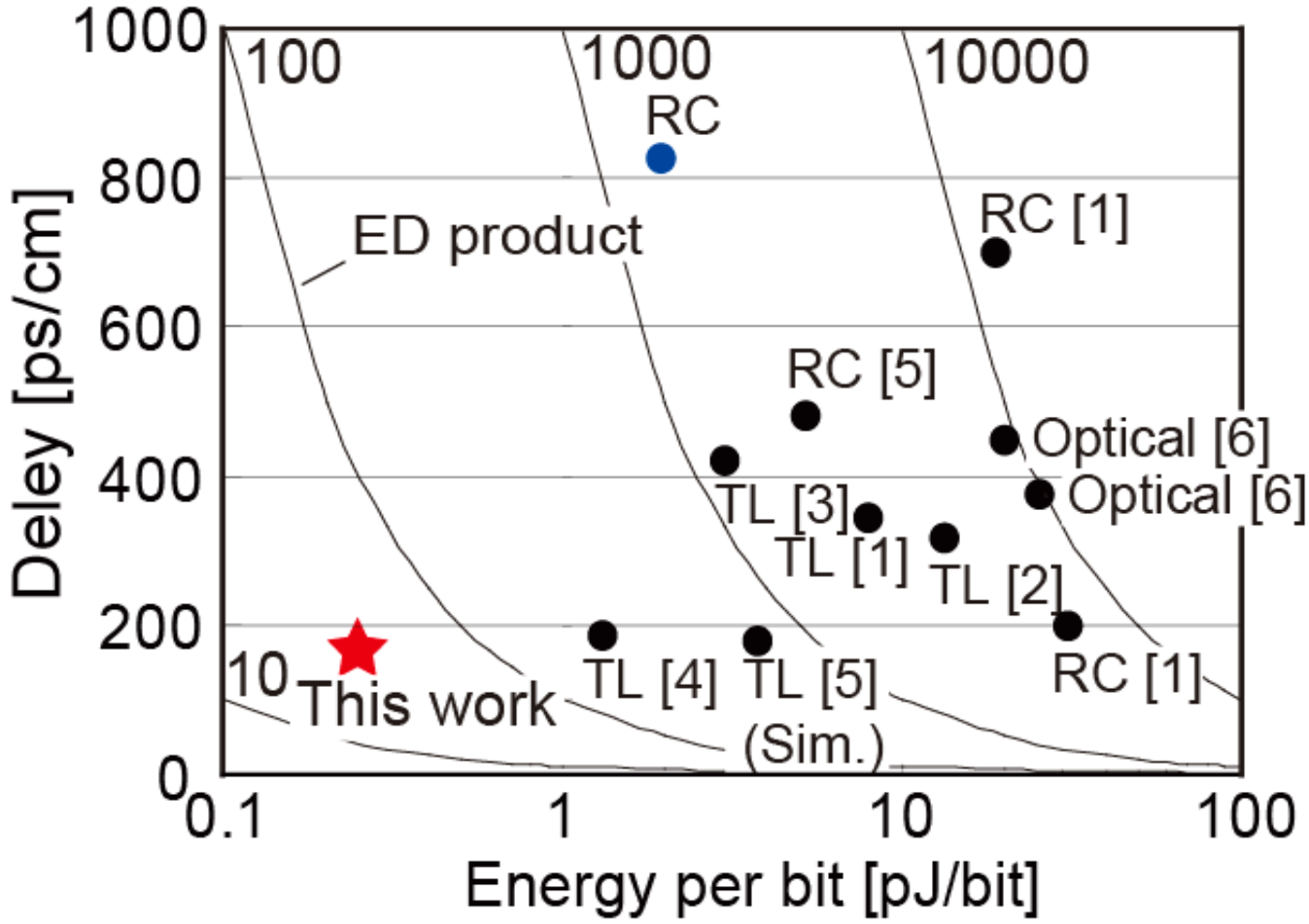
RC line: Minimum line widths and optimal repeater spacing (0.4mm)

Delay variation



	TL Interconnect	RC Line
Average delay (23 chip)	173ps	697ps
Delay variation (3σ)	55ps	310ps

Performance comparison



[1] R. T. Chang, *et al.*, IEEE JSSC, vol. 38, no. 5, pp. 834-838, May 2003.
[2] H. Ito, *et al.*, IEEE A-SSCC, pp. 417-420, 2005.
[3] H. Ito, *et al.*, Circuit Exhibition of ESSCIRC, Poster 26, 2005.
[4] T. Ishii, *et al.*, IEEE A-SSCC, pp. 131-134,. 2006.
[5] S. Gomi, *et al.*, IEEE CICC, pp. 325-328, 2004.
[6] E. D. Kyriakis-Bitzaros, *et al.*, JLT,vol. 19, no. 10, pp. 1532-1542, 2001.

Summary and conclusion

- The LVDS-type on-chip transmission line (TL) interconnect was proposed.
- Delay of the proposed TL interconnect is among the shortest, and energy per bit is the best in reported on-chip long interconnects.