A Slew-Rate-Controlled Output Driver With One-Cycle Tuning Time

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Motivation

- With increasing data rate and signal frequency, ringing by improper termination, crosstalk of transmission lines, and timing problems have emerged.

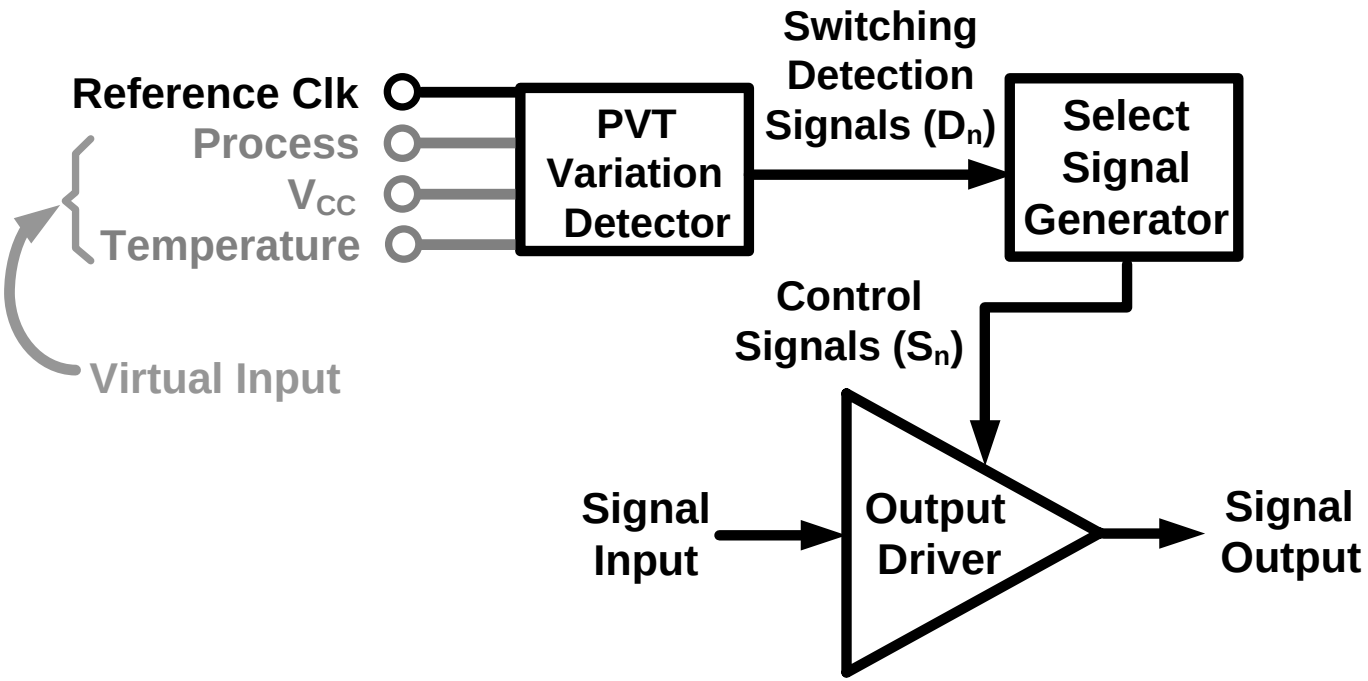
- To obtain a high-speed interface faster than 1Gb/s/pin in low-voltage operation, the output slew rate must be controlled.

- The controlled slew rate technique not only minimizes the power noise but maintains the speed performance of the driver.

Conventional Works

- The PLL based slew-rate controlled output driver (S.-K. Shin, et al., JSSC 2003)
  - The analog PLL occupies large area and consumes large power.
  - Lock time of hundreds of cycles
- The slew rate is controlled by supplemental drivers (T. Matano, et al., JSSC 2003)
  - Easily used in a power down mode
  - Lock time of tens of cycles
- Output driver using a speed-locked loop (SLL) (M. Baze, et al., ISSCC 2004)
  - Digital circuit function and simple interface to output buffers
  - Eight cycles for correct locking

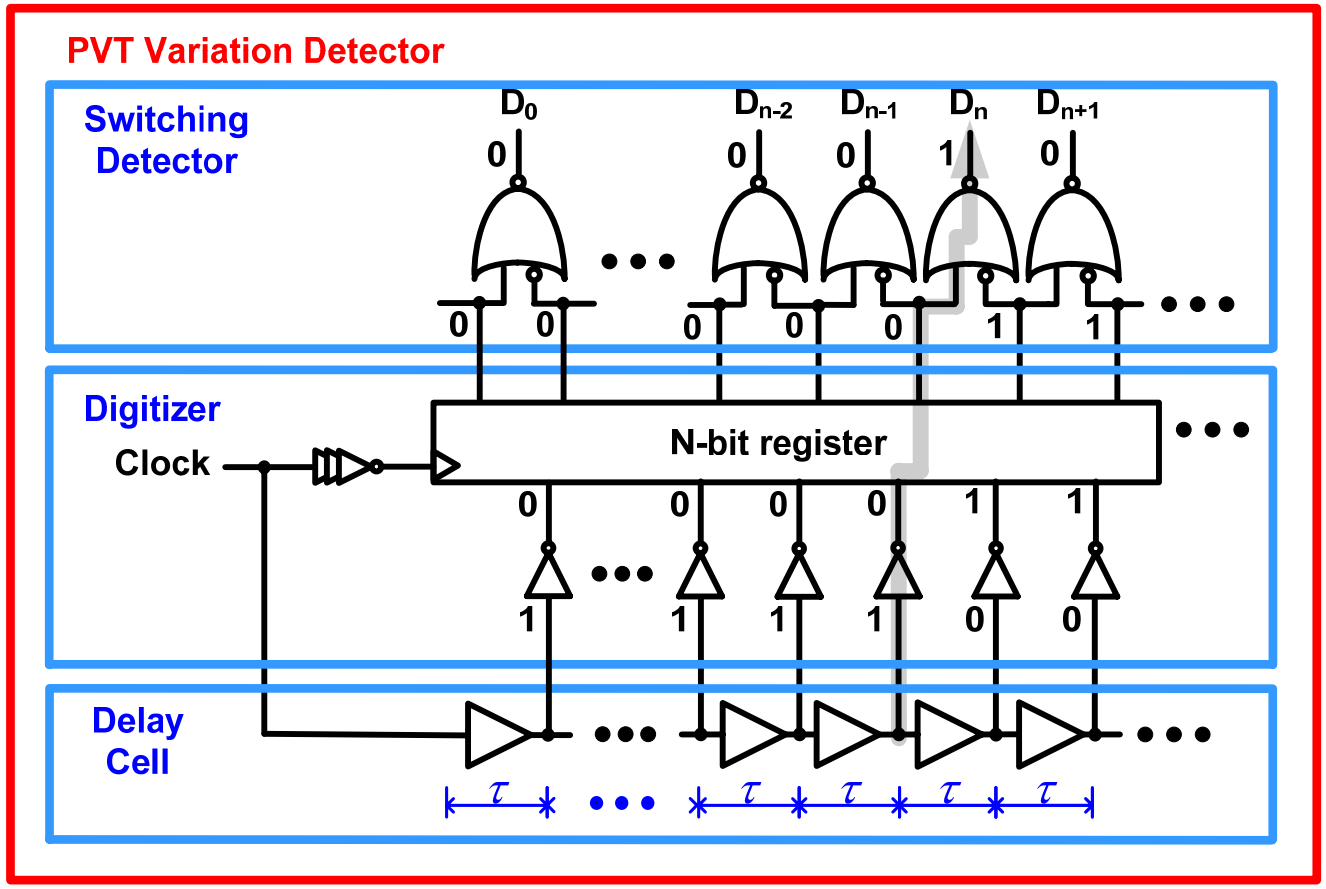
Proposed Architecture

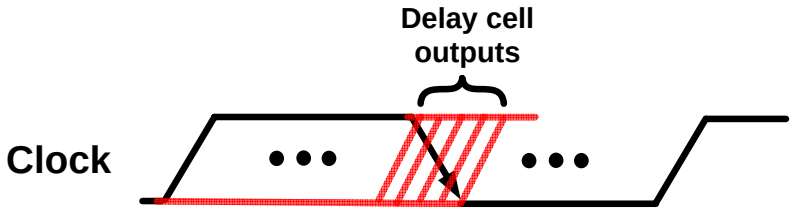


• PVT variation detector detects the process, voltage, and temperature variations by counting the numbers of ‘HI’ stages.

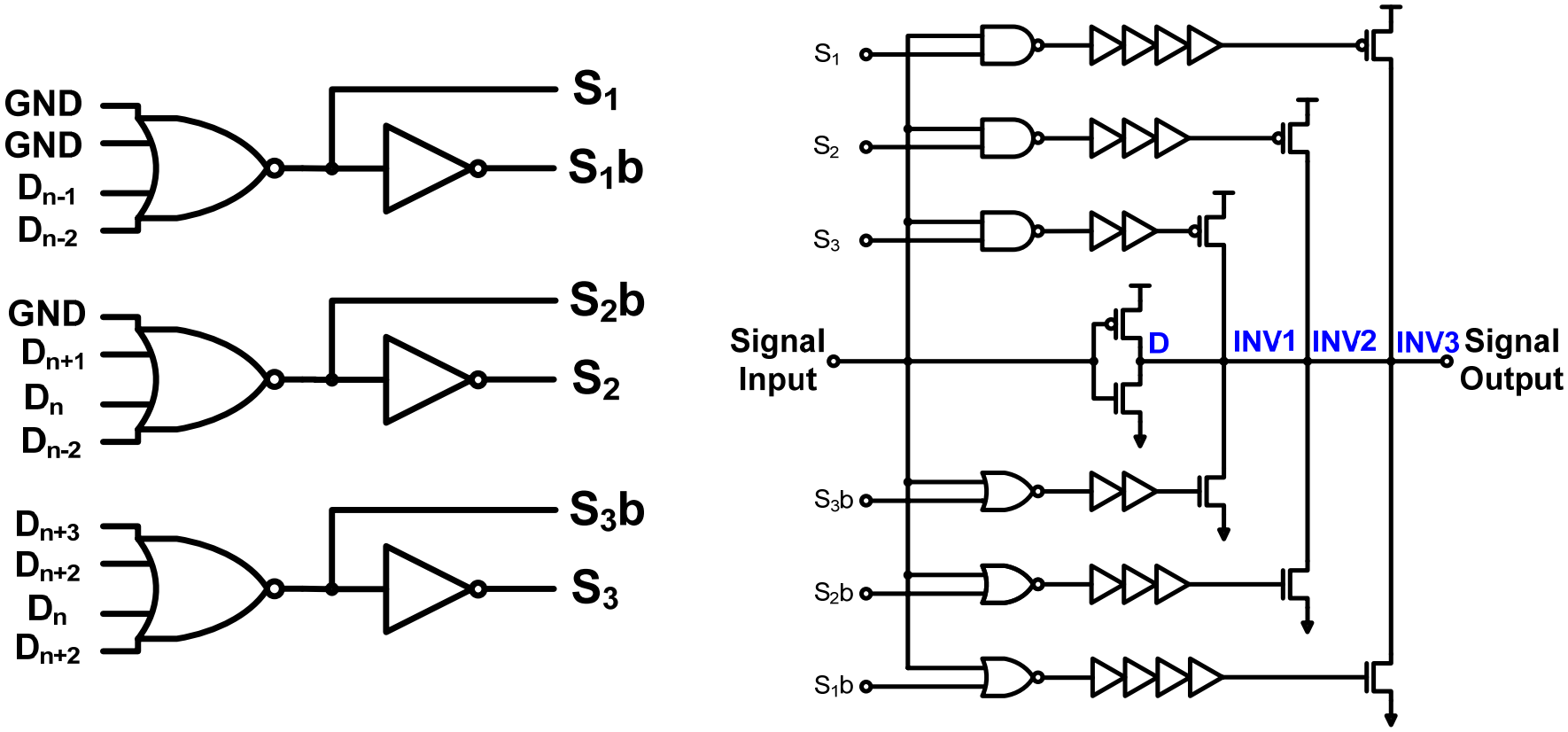
• Select signal generator chooses an optimal output driver configuration.

PVT Variation Detector





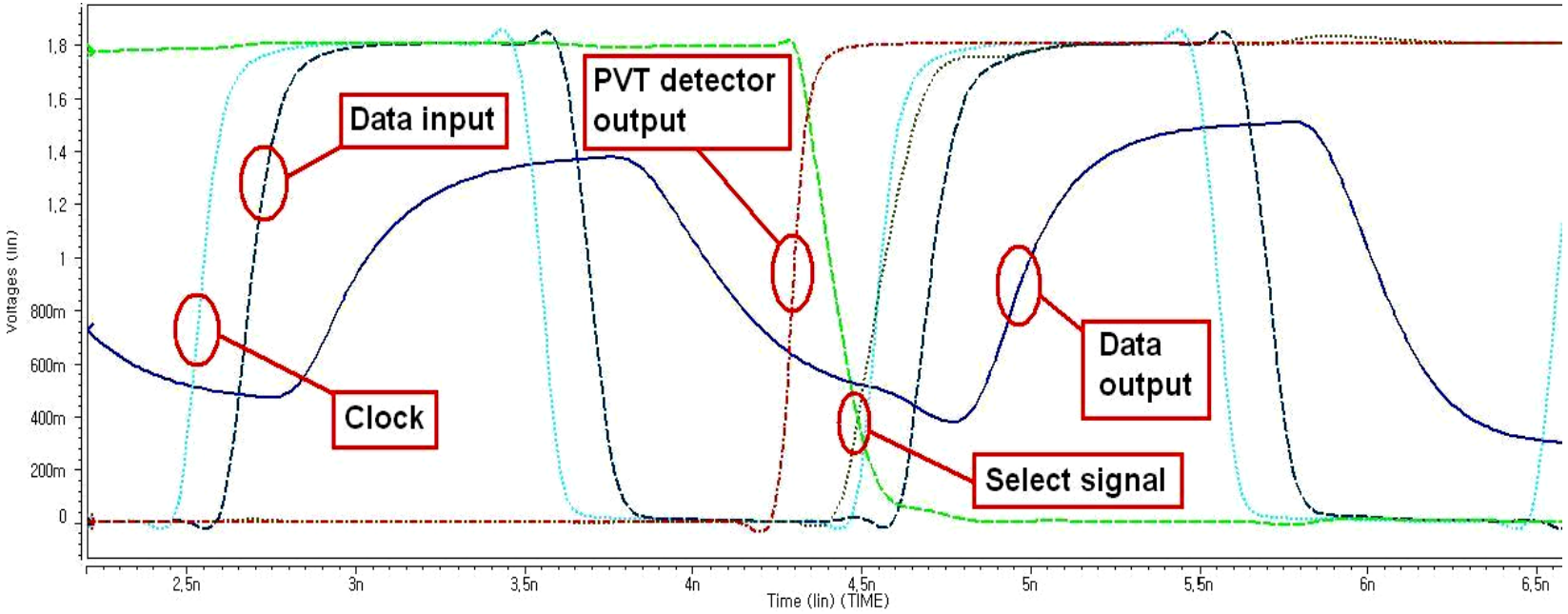
Select Signal Generator / Segmented Output Driver



- Distributed and weighted output driver is used in this scheme.

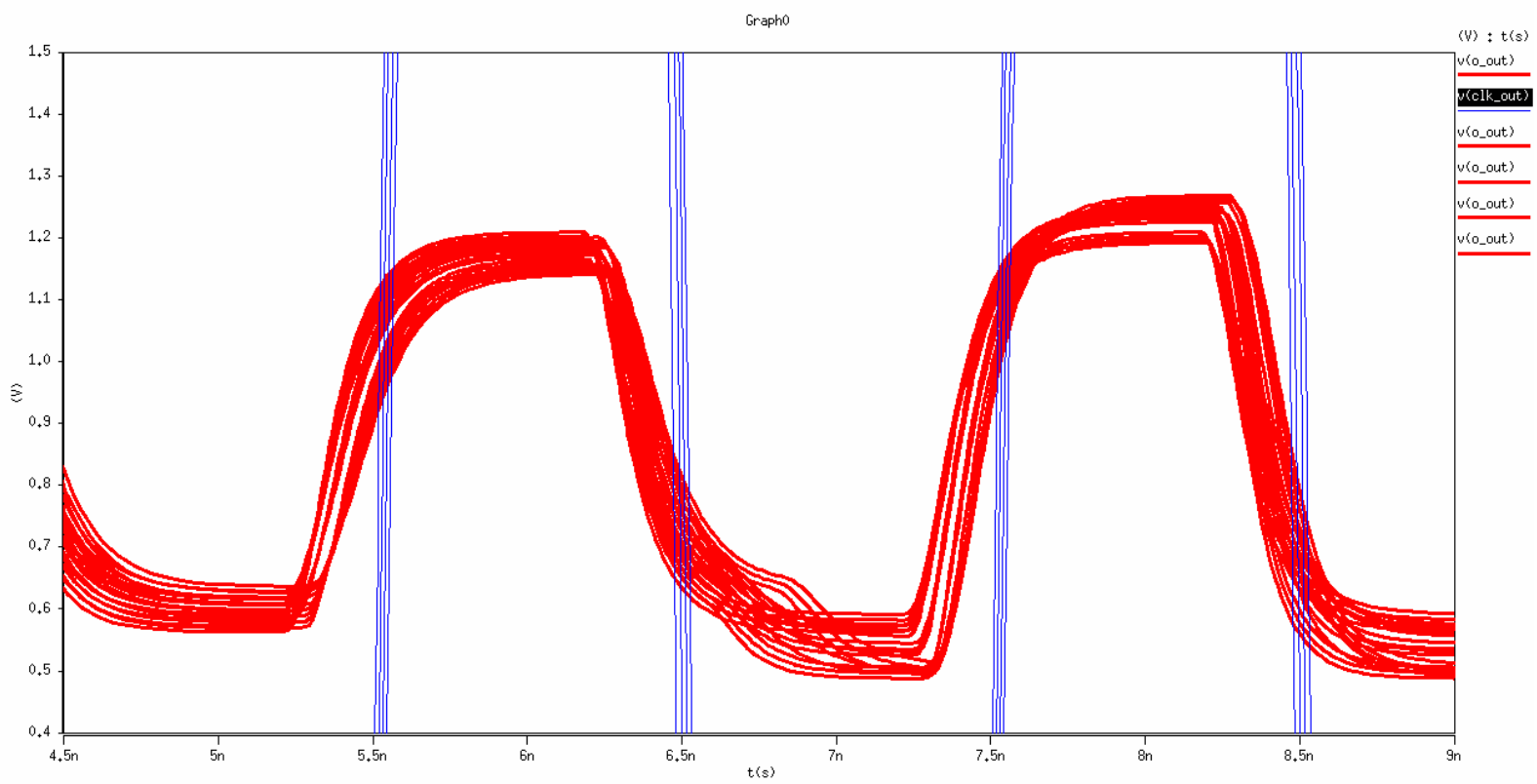
[T.J. Gabara, JSSC 1992]

Simulation Result: Lock time



- The slew rate of the output driver is changed from 1.2V/ns to 2.4V/ns after one-cycle clock.

Simulation Result: Const. Slew-rate



- Simulation conditions: combination of (NN,FF,SS,SF,FS), and (25°C to 95°C) at 1.8V supply voltage @1Gbps
- Output slew rate: from 2.1V/ns to 3.6V/ns

Measurement Result

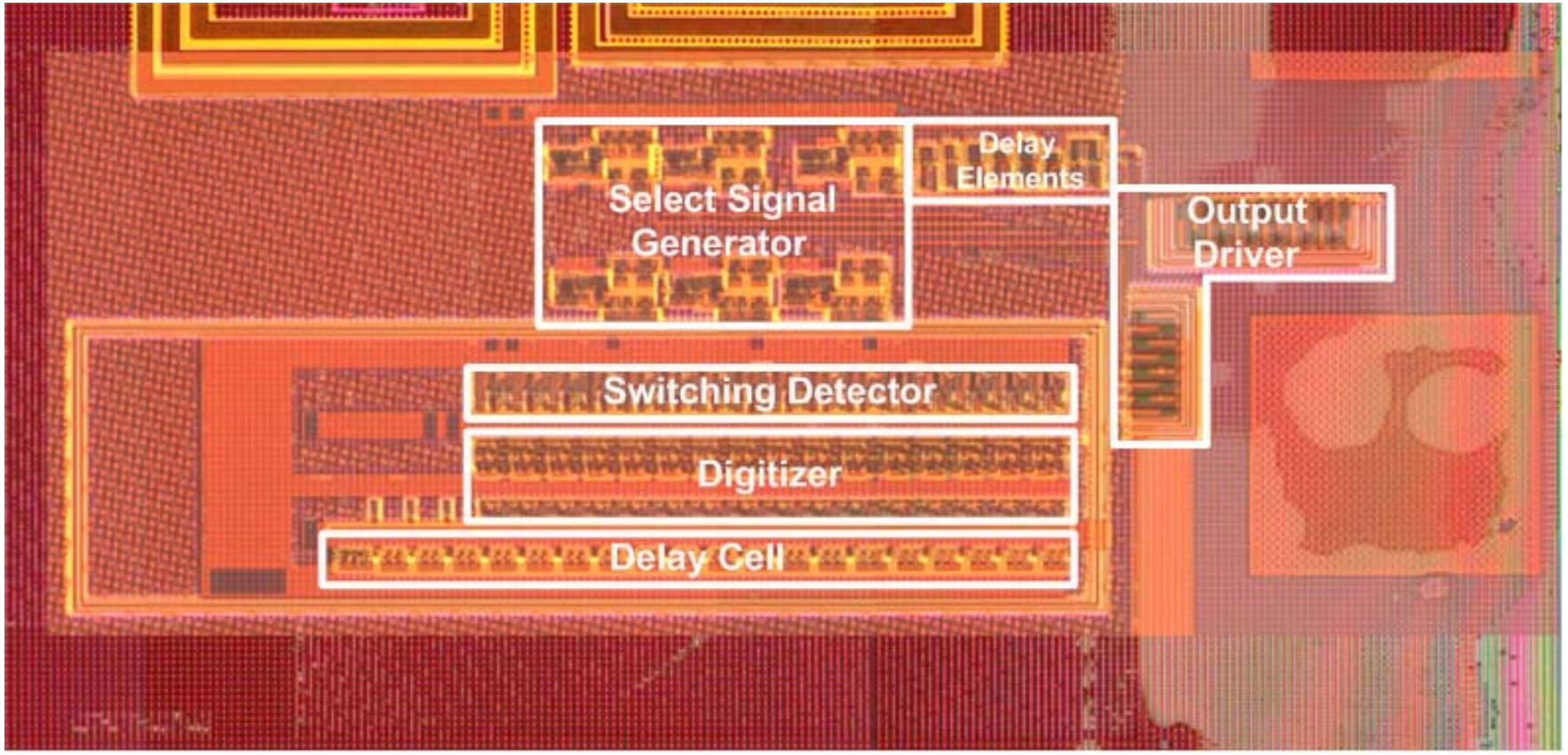
- The measured slew-rate of 2.86V/ns with 4 different supply voltages.

Shmoo Plot

Fast	1.44	1.485	1.53	1.58	1.62	1.665	1.71	1.755	1.8	1.845	1.89	1.935	1.98	2.025	2.07	2.115	2.16
25°C	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d,1	d	d	d	d	d	d	d	d	d
35°C	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d,1	d	d	d	d	d	d	d	d	d
45°C	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d,1	d	d	d	d	d	d	d	d
55°C	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d	d	d	d	d	d	d	d
65°C	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d	d	d	d	d	d	d	d
75°C	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d	d	d	d	d	d	d	d
85°C	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d	d	d	d	d	d	d
95°C	d,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d	d	d	d	d	d	d
Normal	1.44	1.485	1.53	1.58	1.62	1.665	1.71	1.755	1.8	1.845	1.89	1.935	1.98	2.025	2.07	2.115	2.16
25°C	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d	d
35°C	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d	d
45°C	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d
55°C	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d
65°C	d,3	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d,1
75°C	d,3	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d,1	d,1	d,1
85°C	d,3	d,3	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1	d,1	d,1
95°C	d,3	d,3	d,1,2	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1	d,1
Slow	1.44	1.485	1.53	1.58	1.62	1.665	1.71	1.755	1.8	1.845	1.89	1.935	1.98	2.025	2.07	2.115	2.16
25°C	d,1,3	d,1,3	d,3	d,1,2	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1	d,1
35°C	d,1,3	d,1,3	d,3	d,3	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1	d,1
45°C	d,1,3	d,1,3	d,3	d,3	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2	d,1	d,1
55°C	d,1,3	d,1,3	d,3	d,3	d,1,2	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2	d,1
65°C	d,1,3	d,1,3	d,3	d,3	d,1,2	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2	d,1
75°C	d,2,3	d,1,3	d,1,3	d,3	d,3	d,1,2	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2
85°C	d,2,3	d,2,3	d,1,3	d,3	d,3	d,1,2	d,1,2	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2
95°C	d,1,2,3	d,2,3	d,1,3	d,1,3	d,3	d,3	d,1,2	d,1,2	d,1,2	d,1,2	d,2	d,2	d,2	d,2	d,2	d,2	d,2

- Supply voltage resolution: ±2% of the normal voltage (=0.045V)
- Temperature range: from 25°C to 95°C by increasing 10°C
- Three process corners

Chip Photo



- 0.18um 1-poly 4-metal CMOS process
- Area : 0.009mm^2

Comparison with Other Works

	[1] S.-K. Shin JSSC 2003	[2] T.Matano JSSC 2003	[3] M.Baze ISSCC 2004	This work
Controller Type	Analog PLL	Mode/Digital Code	Digital SLL	Digital
Process	0.18um CMOS	0.13um CMOS	0.35um CMOS	0.18um CMOS
Operating Freq.	50Mbps	1Gbps	100Mbps	1Gbps
Power-down Mode	Difficult	Easy	Easy	Easiest
Lock Time	Hundreds of cycles	Tens of cycles	Several cycles	One cycle
Architecture	Close loop	Close loop	Close loop	Open loop
Slew Spec.	0.4–1 V/ns	2.0–4.0 V/ns	1.0–4.0 V/ns	2.0–4.0 V/ns
Measured Slew Rate	0.403–0.99 V/ns	1.6–2.2 V/ns	–	2.1–3.58 V/ns
Supply	3.3 V	1.8 V	3.3 V	1.8 V
External Resistance	–	Yes	No	No
Power Consumption	–	–	Medium (2.2mW, 0.22mW/Mbps)	Low (13.7mW, 0.013mW/Mbps)
Core Area	Large (0.16mm^2)	–	Medium (0.045mm^2)	Small (0.009mm^2)

Conclusions

- A new slew-rate-controlled output driver is proposed that is adaptive under various PVT variations.

- Proposed slew-rate-controlled output driver
  - One-Cycle Lock Time: Output-on-Demand
  - Small Area
  - Low Power Consumption