A Low-leakage Current Power 180-nm CMOS SRAM

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January 22, 2008

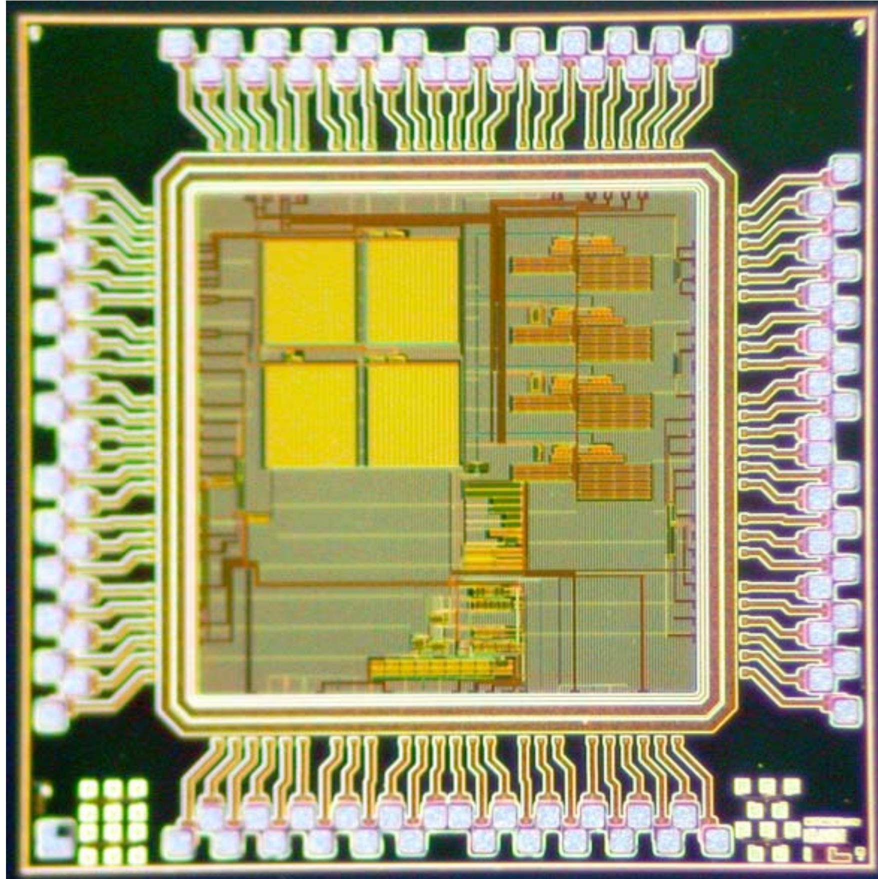
ASP-DAC'2008, ID-5

COEX, Seoul, Korea

Presentation Outline

1. Low Leakage Current SRAMs
2. Problems of Deep Submicron Devices and Requirements for Leakage Current Reduction Circuits
3. Self-controllable-Voltage-Level (SVL) Circuit
4. Speed Performance & Dynamic Power
5. “Write Margin” Expansion by SVL Circuit
6. Summary

1-Kb, 180-nm CMOS SRAM with SVL Circuit



SVL: Self-controllable-Voltage-Level

Technology:
180-nm CMOS
5-layer Al Metal
1-layer Pory Si

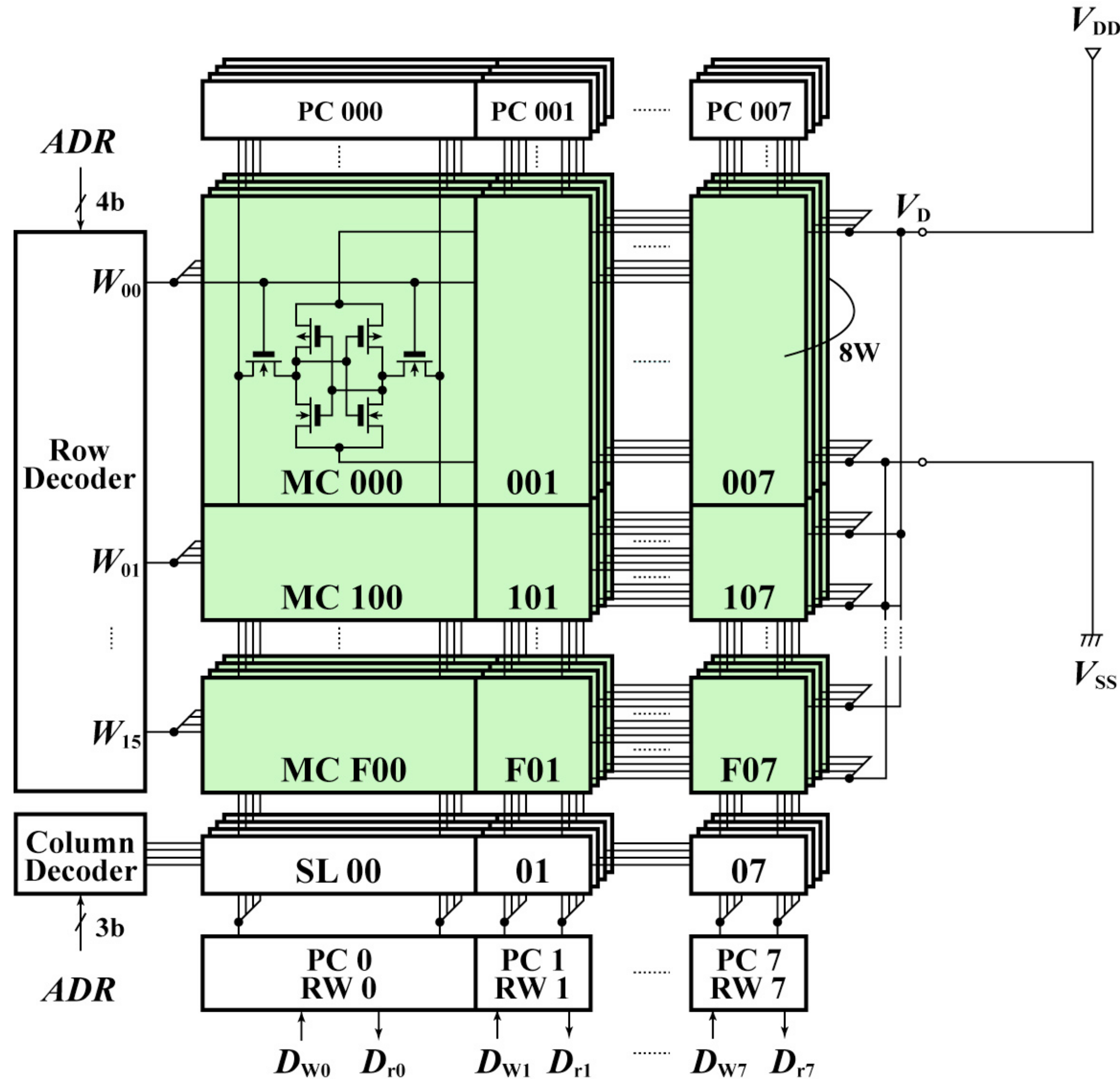
Gate Lengths :
$L_n = L_p = 0.2$ μm

Threshold Voltage :
$V_{tn} = 0.435$ V
$V_{tp} = -0.415$ V

Chip Size:
2.8 mm × 2.8 mm

Supply Voltage : 1.8 V

1-Kb, 180-nm CMOS SRAM (conventional)



Word Structure:

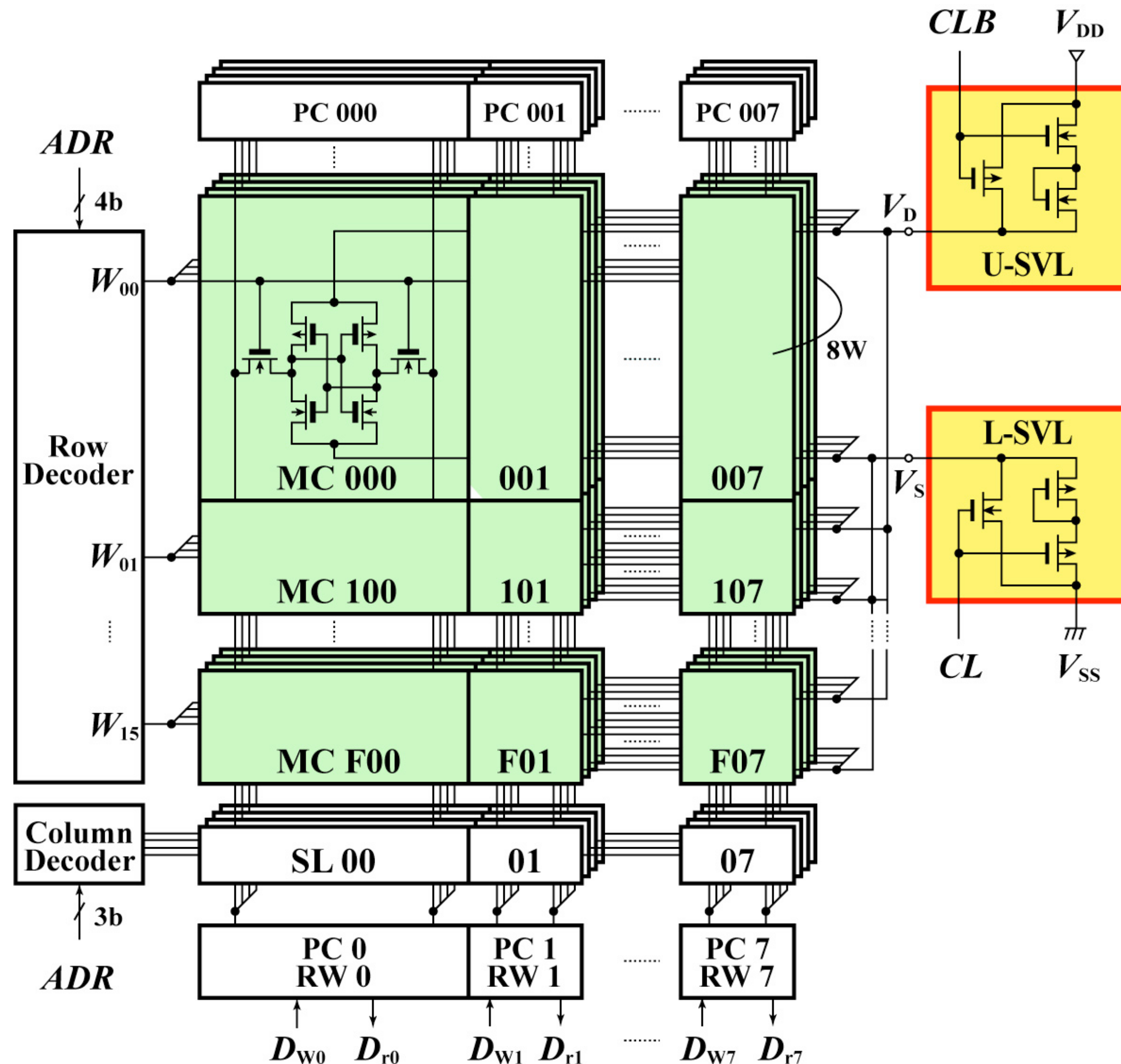
8 bit×(8×16)words

Memory Cells :

$W_p = 2.50\ \mu m$

$W_n = 1.25\ \mu m$

1-Kb, 180-nm CMOS SRAM
(with SVL Circuit)



Word Structure:
8 bit×(8×16)words

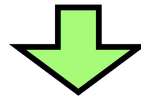
Memory Cells :
W_p = 2.50 µm
W_n = 1.25 µm

U-SVLCircuit :
W_p = 320.0 µm
W_n = 1.25 µm

L-SVLCircuit :
W_p = 1.25 µm
W_n = 320.0 µm

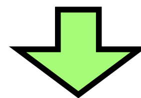
Problems of Deep Submicron Devices

Supply Voltages mast be lowered, but
Electric Fields have increased



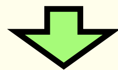
Leakage Currents
(Sub-threshold, GIDL and Tunneling)
Increased

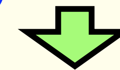
“Write” Margin of SRAM
Decreased

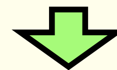


Leakage Current Reduction and
“Write” Margin Expansion Circuits
are Needed

Requirements for Leakage Current Reduction & "Write" Margin Expansion Circuits

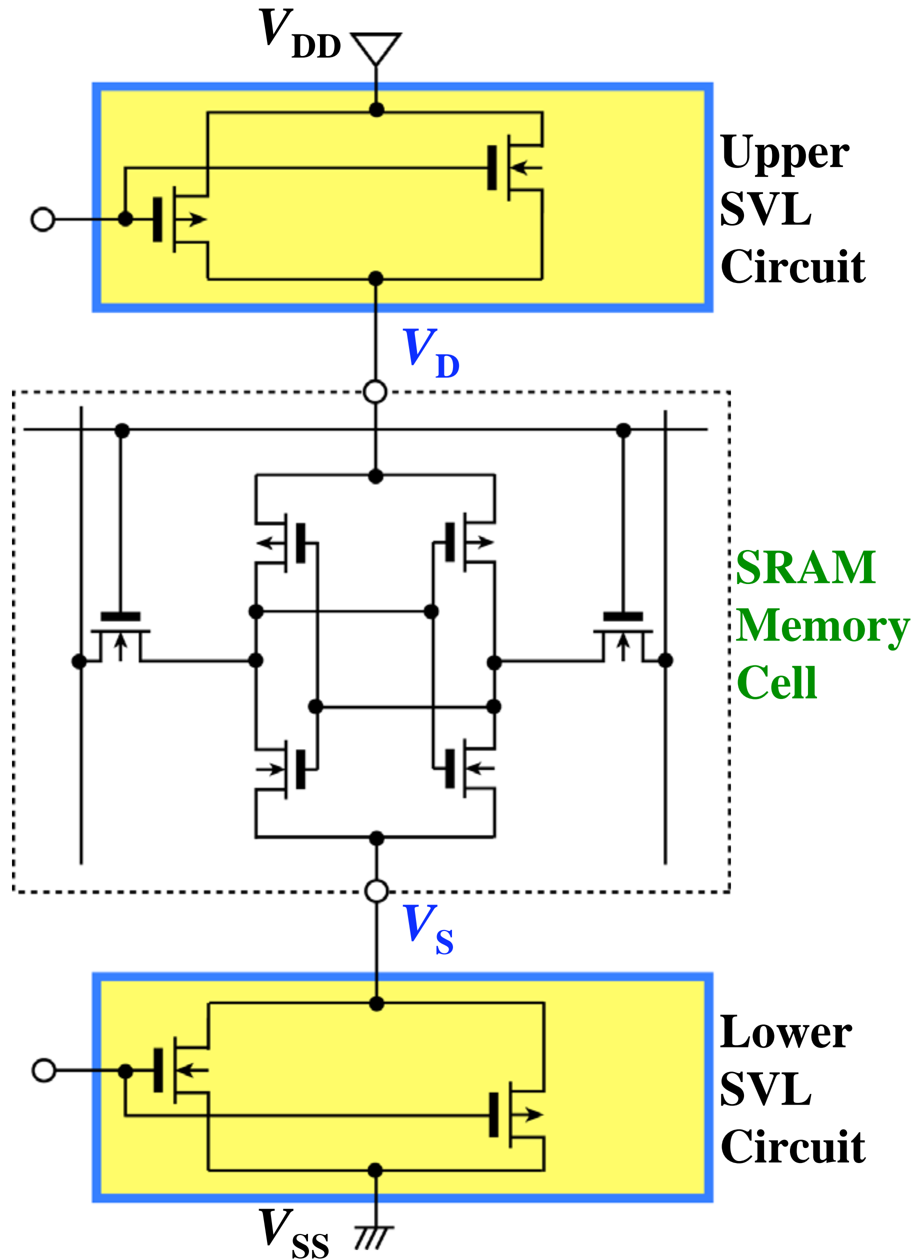
"Read" Mode
High Supply Voltage (V_{DD}, V_{SS})

High-Speed Read Operation

"Write" Mode
Low Supply Voltage (V_D, V_S)

"Write" Margin Expansion

Stand-by Mode
High Threshold Voltages (V_ts)
Low Electric Fields

Low Leakage Current
Data Retention

Memories and Flip-flops

Self-controllable Voltage Level (SVL) Circuit



Upper SVL Circuit

p-MOSFET switch
- wide channel
- low threshold voltage

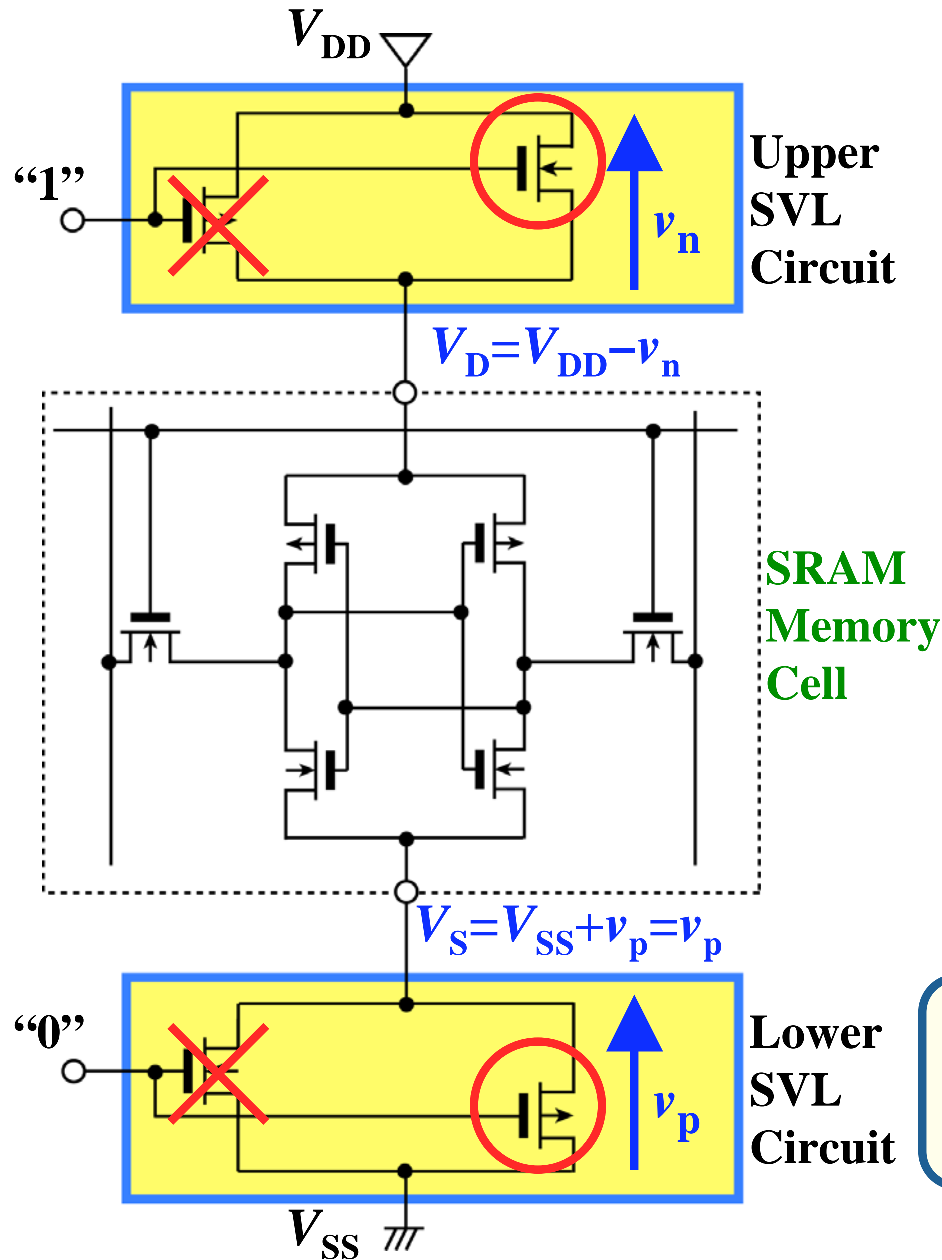
n-MOSFET switches
- narrow channel
- low threshold voltage

Lower SVL Circuit

n-MOSFET switch
- wide channel
- low threshold voltage

p-MOSFET switches
- narrow channel
- low threshold voltage

Memory Cell Array in Stand-by Mode



Upper SVL Circuit :

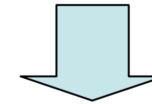
nMOS Switch is Turned on

$V_D=V_{DD}-v_n$ $(<V_{DD})$

Lower SVL Circuit :

pMOS Switch is Turned on

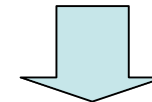
$V_S=V_{SS}+v_p=v_p(>0V)$



Memory Cells :

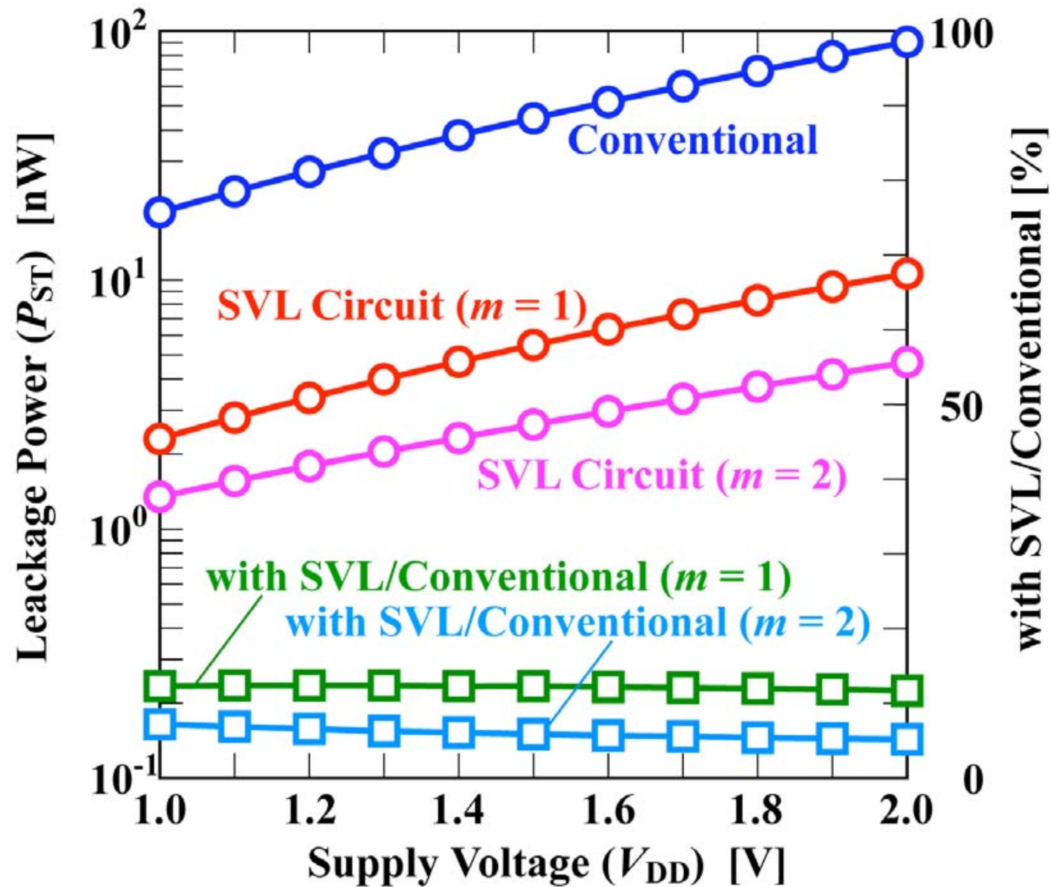
Reduced Electric Field : $V_{ds}<V_{DD}$

Increased Backward Bias : $-V_{sub}>0$



Leakage Currents; Reduced
Memory Cell Data; Rettained

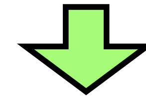
Leakage Power (P_{ST}) of 1-Kb Memory Cell Array of 180-nm CMOS SRAM (SPICE)



V_{SS}=0V, T=25 °C

Conventional

P_{ST}=69.1 nW



SVL Circuit with m = 1

P_{ST}=8.3nW at V_{DD}=1.8V

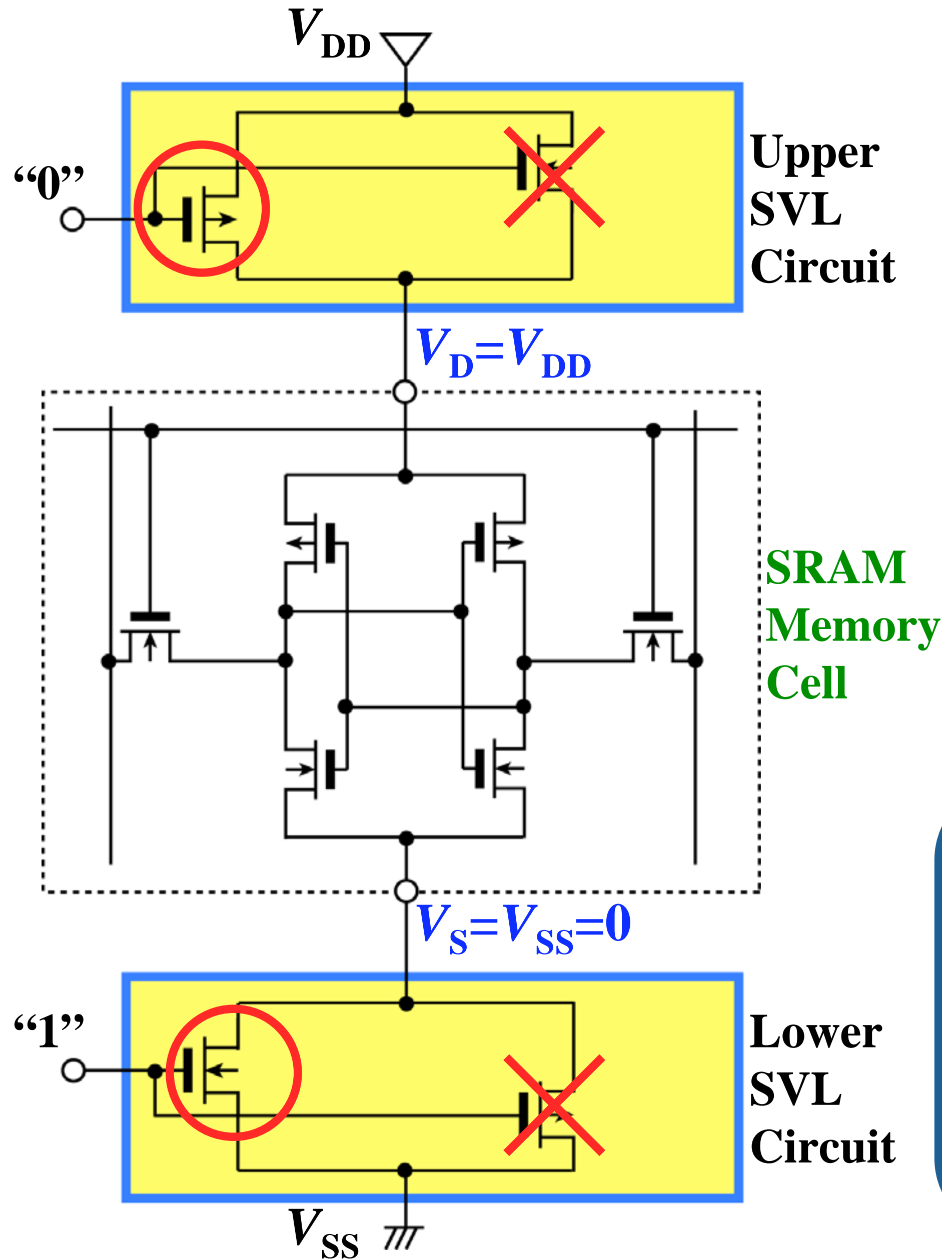
12.0%

SVL Circuit with m = 2

P_{ST}=3.7nW at V_{DD}=1.8V

5.4%

Memory Cell Array in "Read" Mode



Upper SVL Circuit :

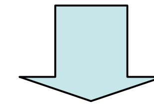
pMOS Switch is Turned on

V_{DD} is Supplied

Lower SVL Circuit :

nMOS Switch is Turned on

V_{SS} is Supplied



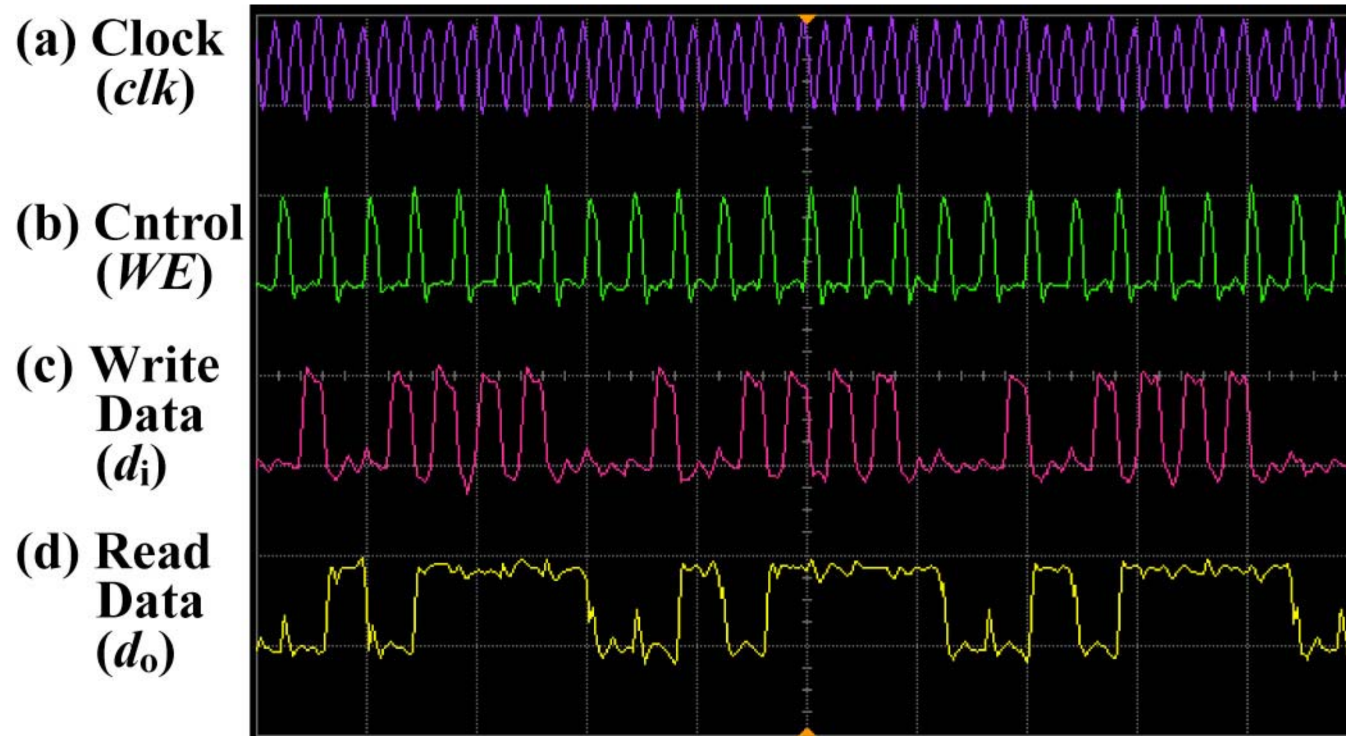
Memory Cells :

Max. Supply Voltage : $V_{ds} = V_{DD}$

No backward Bias : $V_{bs} = 0$

High-Speed "Read" Operation

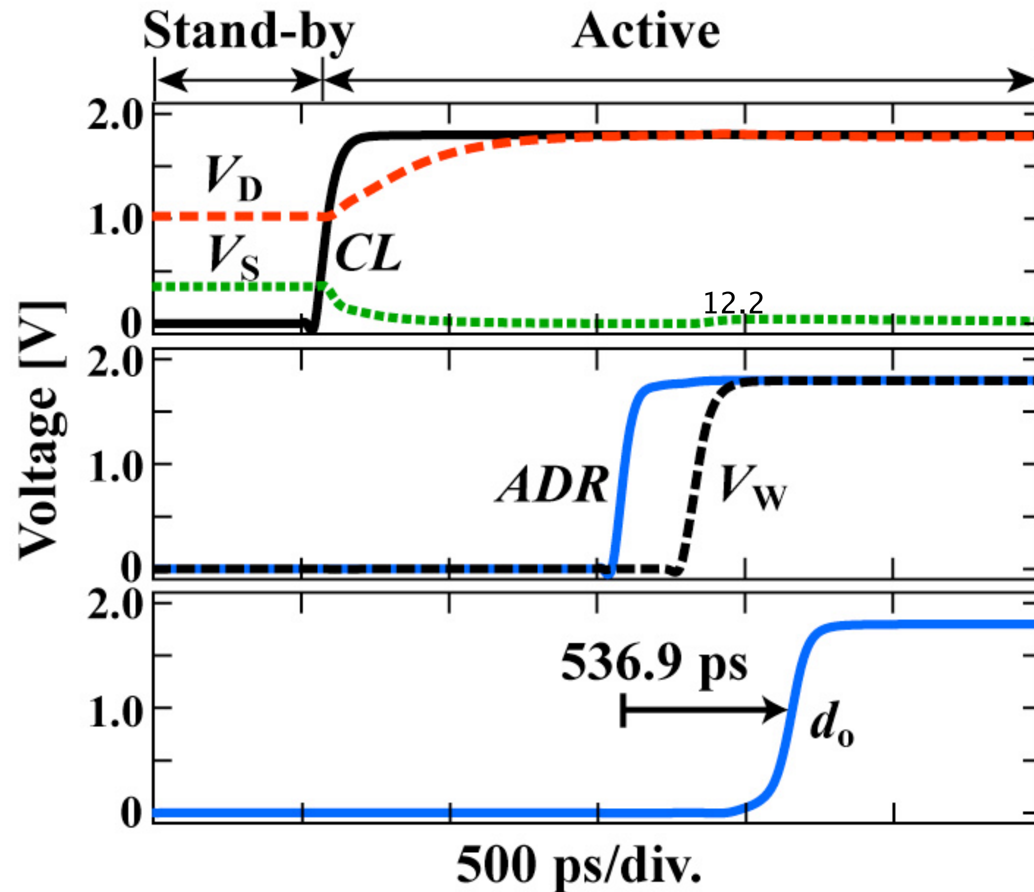
Measured Waveforms of 1-Kb, 180-nm CMOS SRAM with SVL Circuit



Write Data =1, 0, 1, 1, 1, 1, 0, 0 · · · · = Read Data

Vertical=2V/div., Horizontal=50.0 nsec/div.
V_{DD}=1.8V, V_{SS}=0V, f_c=100 MHz

Waveforms of 1-Kb, 180-nm CMOS SRAM with SVL Circuit (”1” Read)

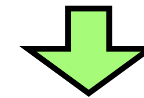


V_D = 1.026 V, V_S = 0.354 V

V_{DD} = 1.8 V, V_{SS} = 0 V

Conventional

t_a = 535.5 psec

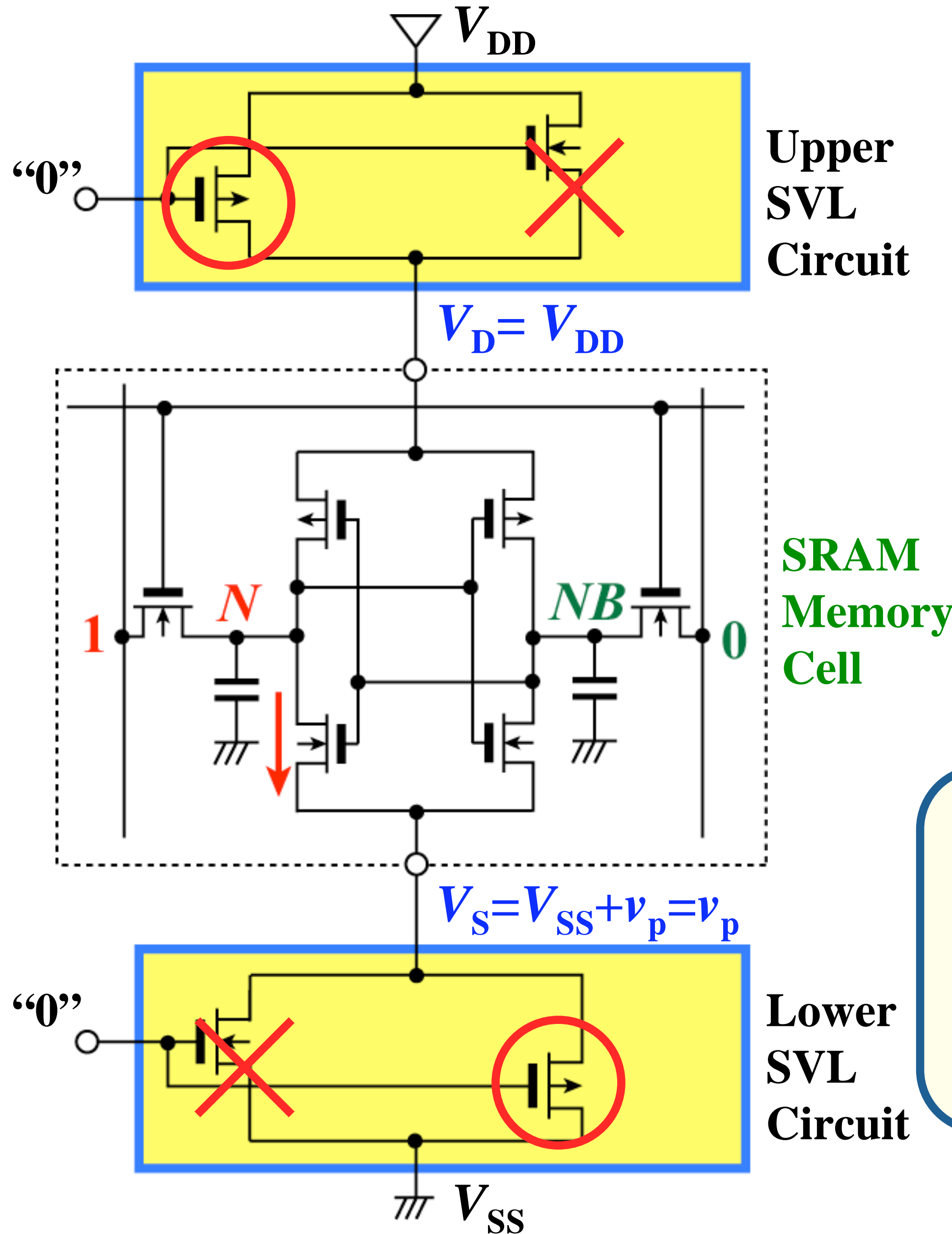


SVL Circuit with m=1, 2

t_a = 536.9 psec

at V_{DD}=1.8V

Memory Cell Array in "Write" Mode



Upper SVL Circuit :

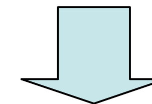
pMOS Switch is Turned on

V_{DD} is Supplied

Lower SVL Circuit :

nMOS Switch is Turned on

$V_S = V_{SS} + v_p (> V_{SS})$ is Supplied



Memory Cells :

Min. Supply Voltage : $V_{ds} = V_{DD} - v_p$

Backward Bias : $V_{bs} = -v_p$

"Write" Margin Expansion

Characteristics of 1Kb, 180-nm CMOS SRAM with SVL Circuit

		Conv.	$m = 1$	$m = 2$
"1" Read Access Time (t_a) [psec] (SVL/Conv. [%])		535.5	536.9 (100.3%)	536.9 (100.3%)
Stand-by Power (Leakage Power) (P_{ST}) [nW]	Cell Array (SVL/Conv. [%])	69.1	8.3 (12.0%)	3.7 (5.4%)
	SRAM (SVL/Conv. [%])	105.5	44.7 (42.4%)	40.7 (38.6%)
Active Power (P_{AT}) [µW] @200MHz (SVL/Conv. [%])		3,296.0	3295.6 (99.9%)	3295.6 (99.9%)
Active Area[mm^2] (SVL/Conv. [%])		0.0944	0.0959 (101.6%)	0.0960 (101.7%)

V_{DD} = 1.8 V, V_{SS} = 0 V, f_c = 200 MHz , T = 25 ℃

End of the presentation…