Area Recovery under Depth Constraint by Cut Substitution for Technology Mapping for LUT-based FPGAs

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Technology mapping problem for LUT-based FPGAs to minimize area under depth minimum constraint

Technology mapping problem for LUT-based FPGAs

- Input : Subject graph
  - DAG (Directed Acyclic Graph)
  - Each node represents a Boolean function of up to k variables

    k : the maximum number of inputs of an LUT (Lookup-table)
- Output : LUT network
  - DAG whose nodes represent LUTs

Difficult problem

- Object

  Minimize the number of LUTs of LUT network
- Constraint

  Depth of LUT network

Technology mapping based on K-feasible cut selection

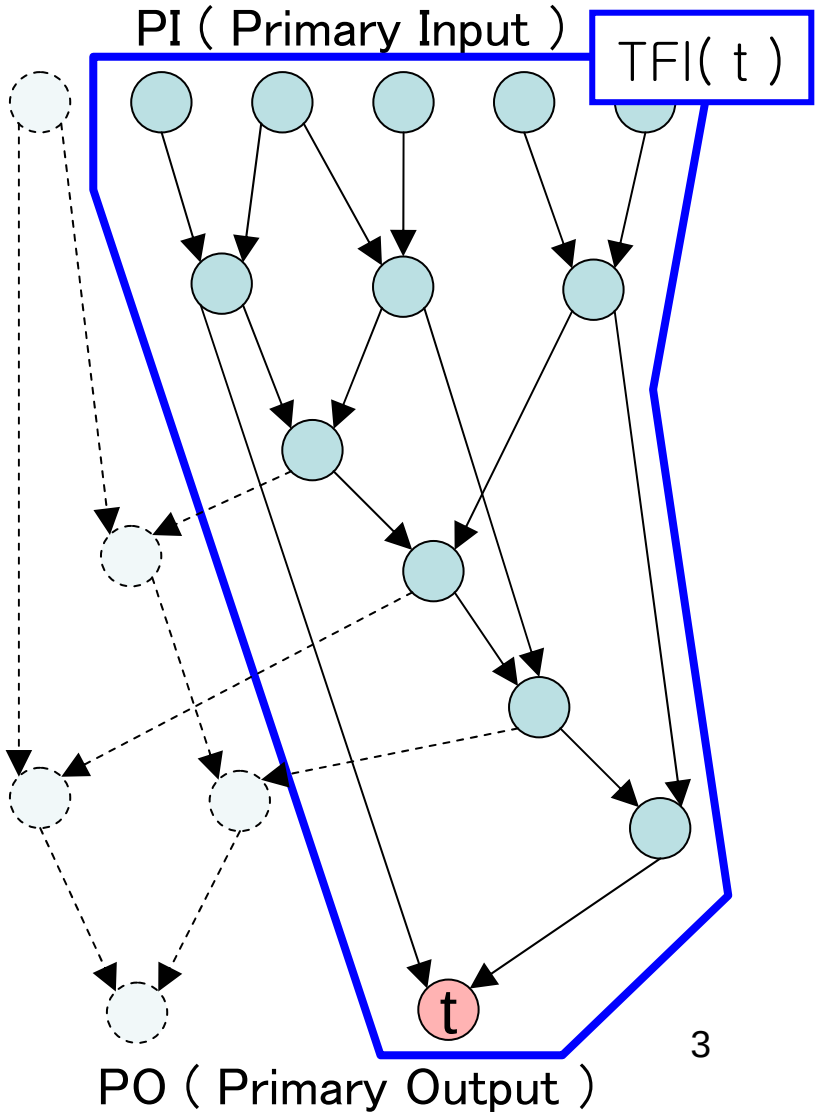
- A K-feasible cut at a node t is a partitioning $(X, \overline{X})$ of transitive fanin (TFI(t))

$$TFI(t) = fanin(t) \bigcup_{u \in fanin(t)} TFI(u)$$

$$|cutset(X, \overline{X})| \leq k$$

  - cutset is border nodes in X

- A subgraph induced by $\overline{X}$ can be implemented in a k-input LUT
  - $cutset(X, \overline{X})$ is inputs of LUT



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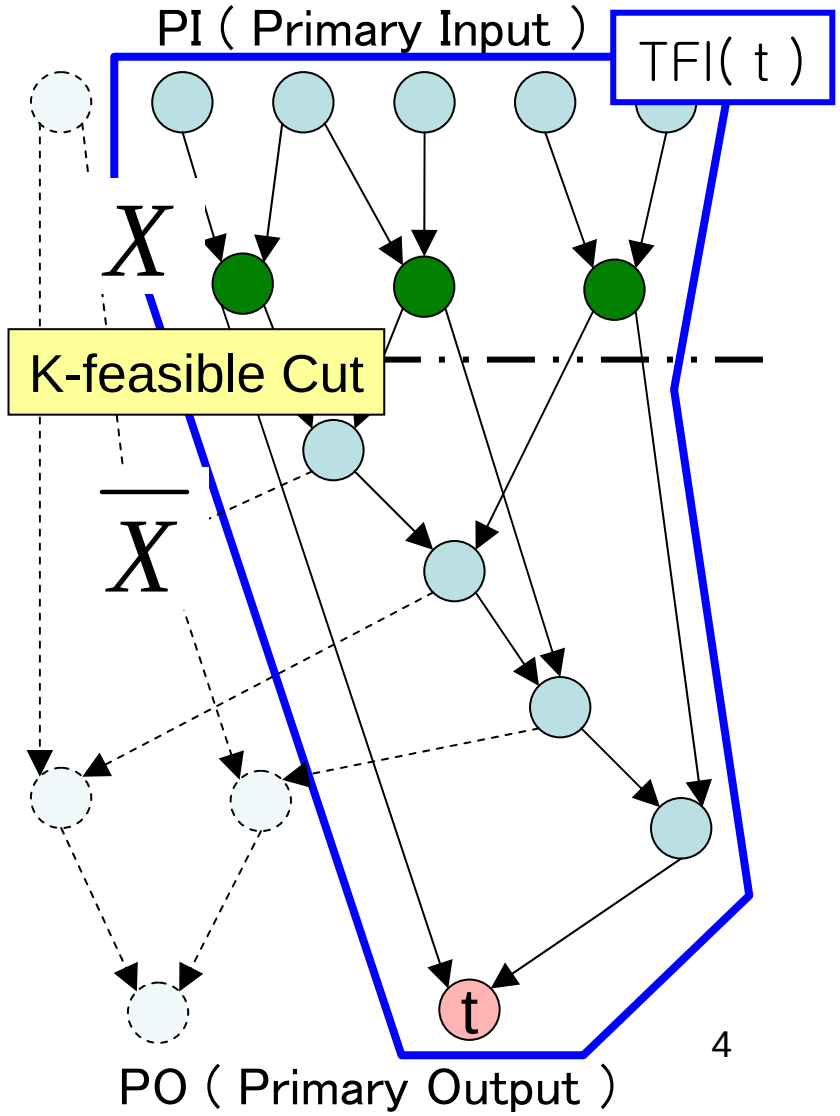

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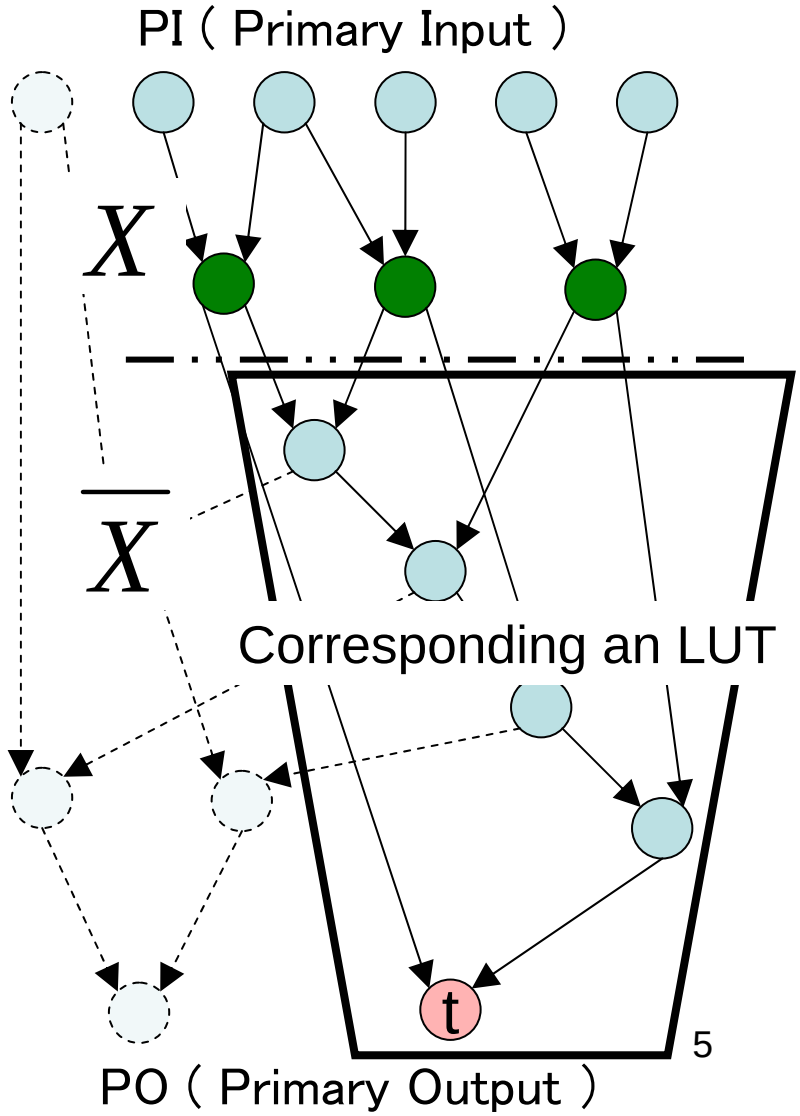
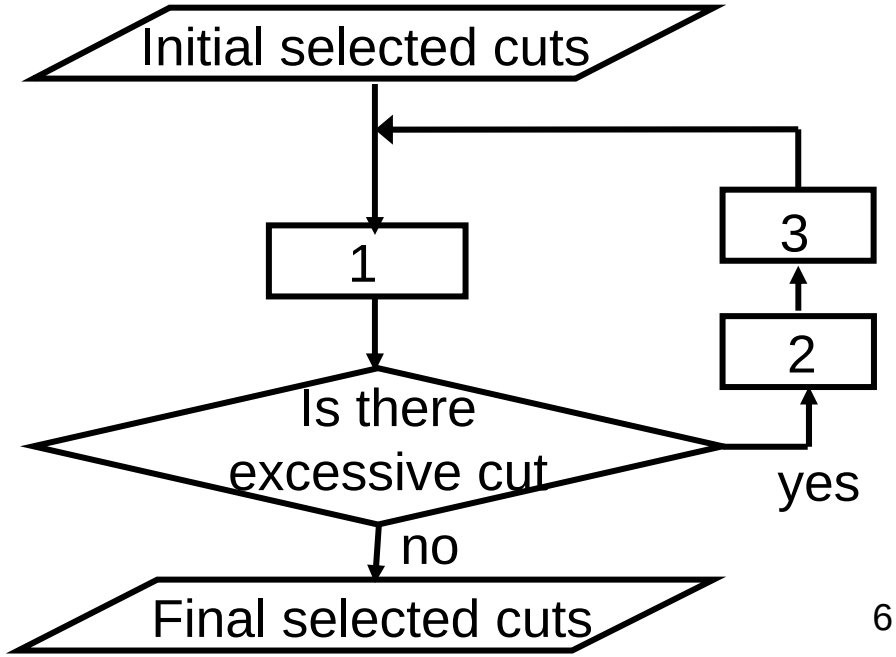


Proposed technique : Cut Substitution

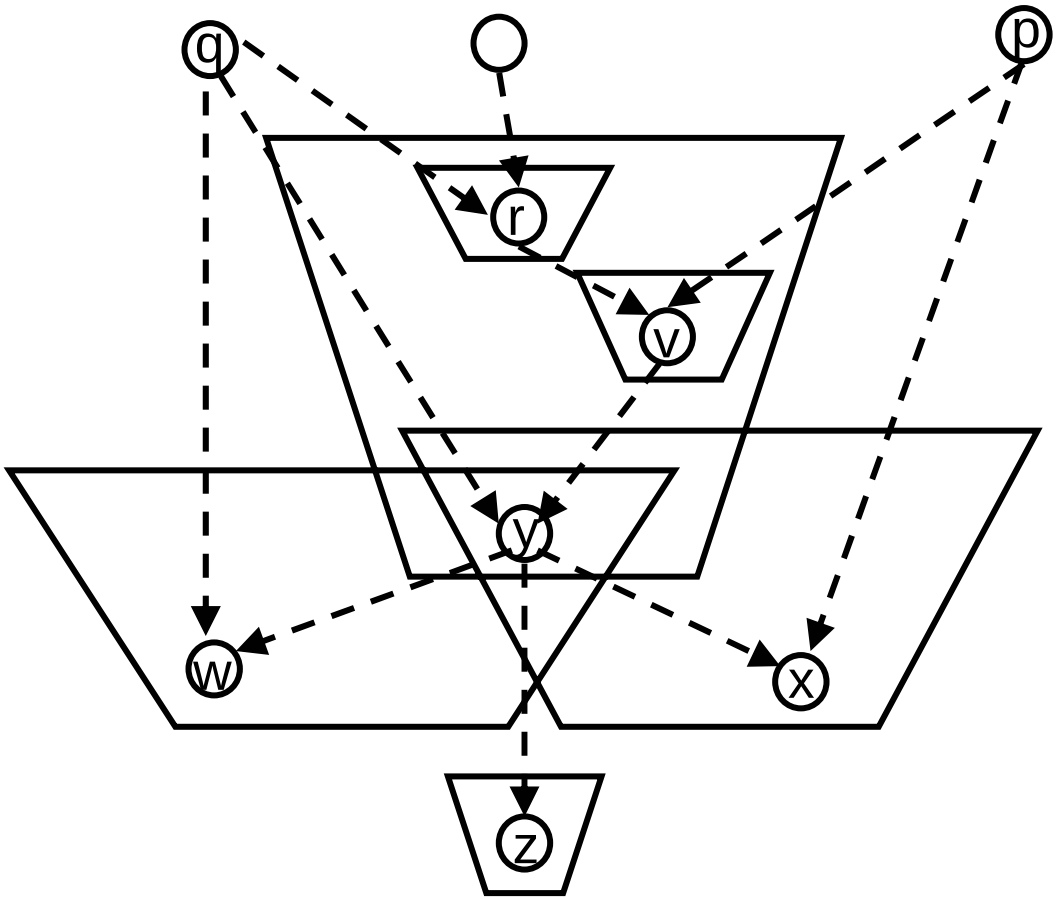
- Cut Substitution : a post-processing of technology mapping to generate a local optimum solution by eliminating excessive LUTs while the depth of network is maintained
  - Cut Substitution directly eliminates several excessive cuts from the set of cuts selected at technology mapping
- The processing of Cut Substitution is loop iteration

1. Excessive cut enumeration
2. Choice of a best-cut
3. Cut elimination



The processing of a iteration of Cut Substitution

Phase 1 : Excessive cut enumeration



LUT network

The processing of a iteration of Cut Substitution

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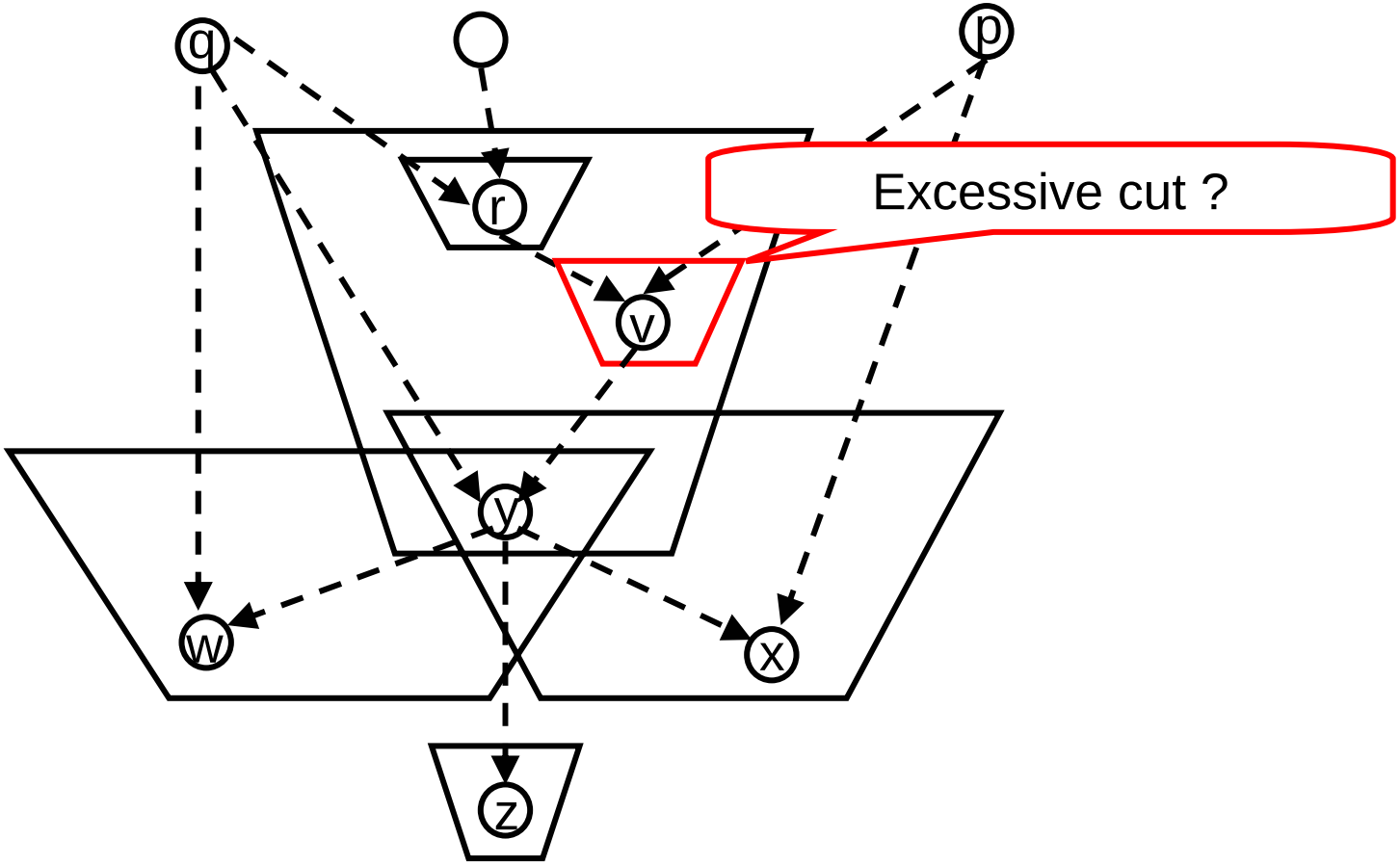
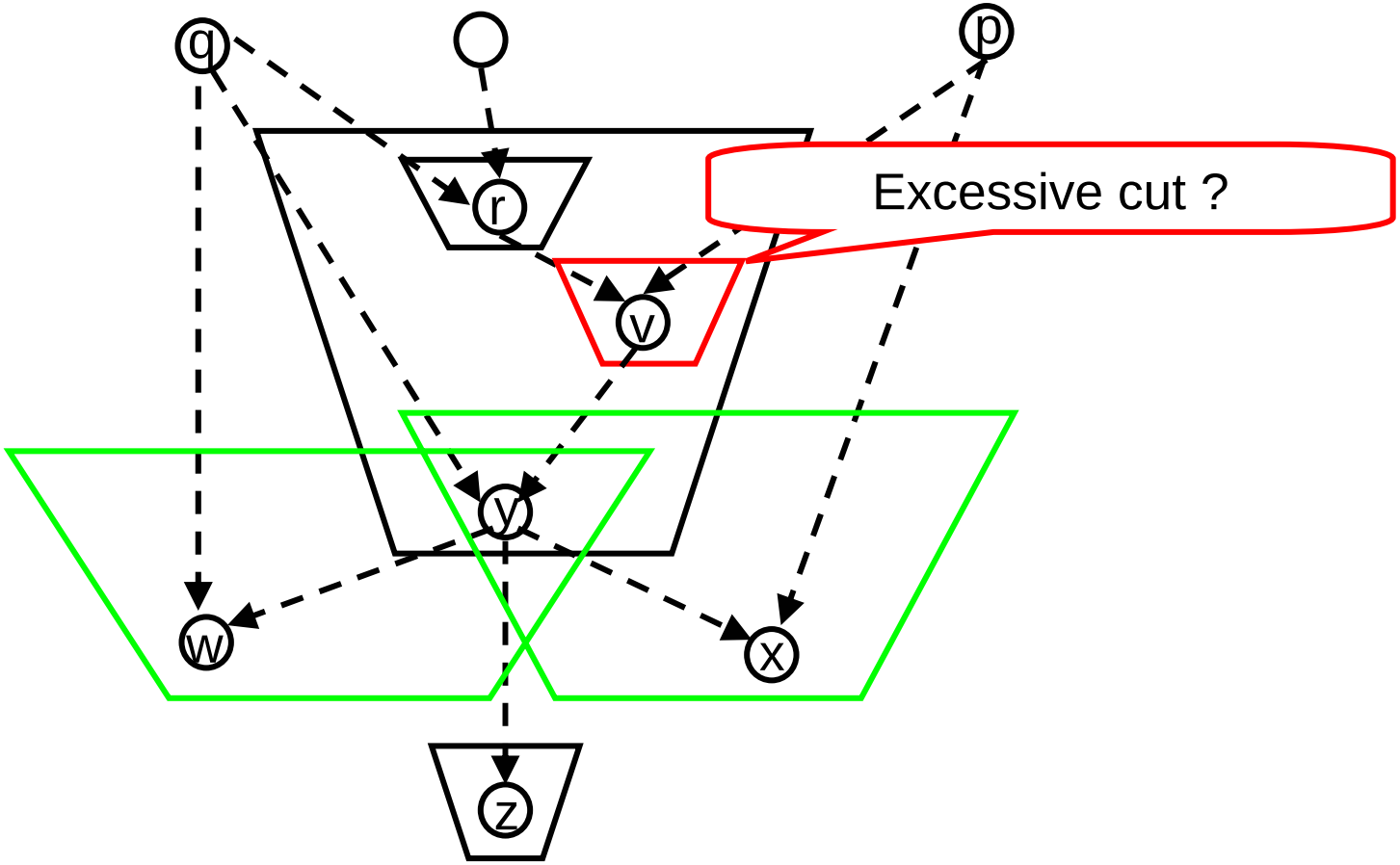


LUT network

The processing of a iteration of Cut Substitution

Are there cut at ⓧ and ⓦ not to use ⓥ as input ?



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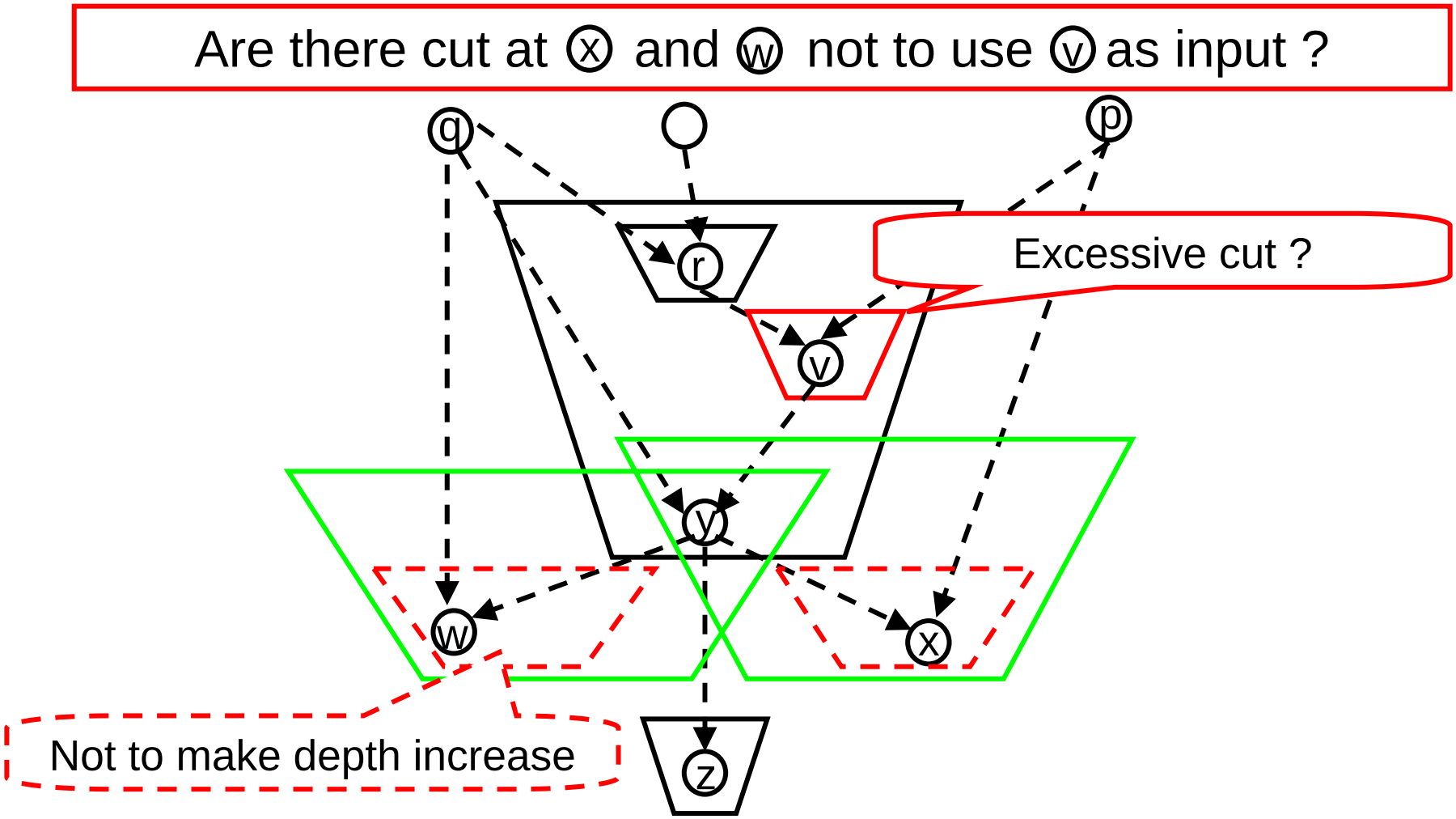

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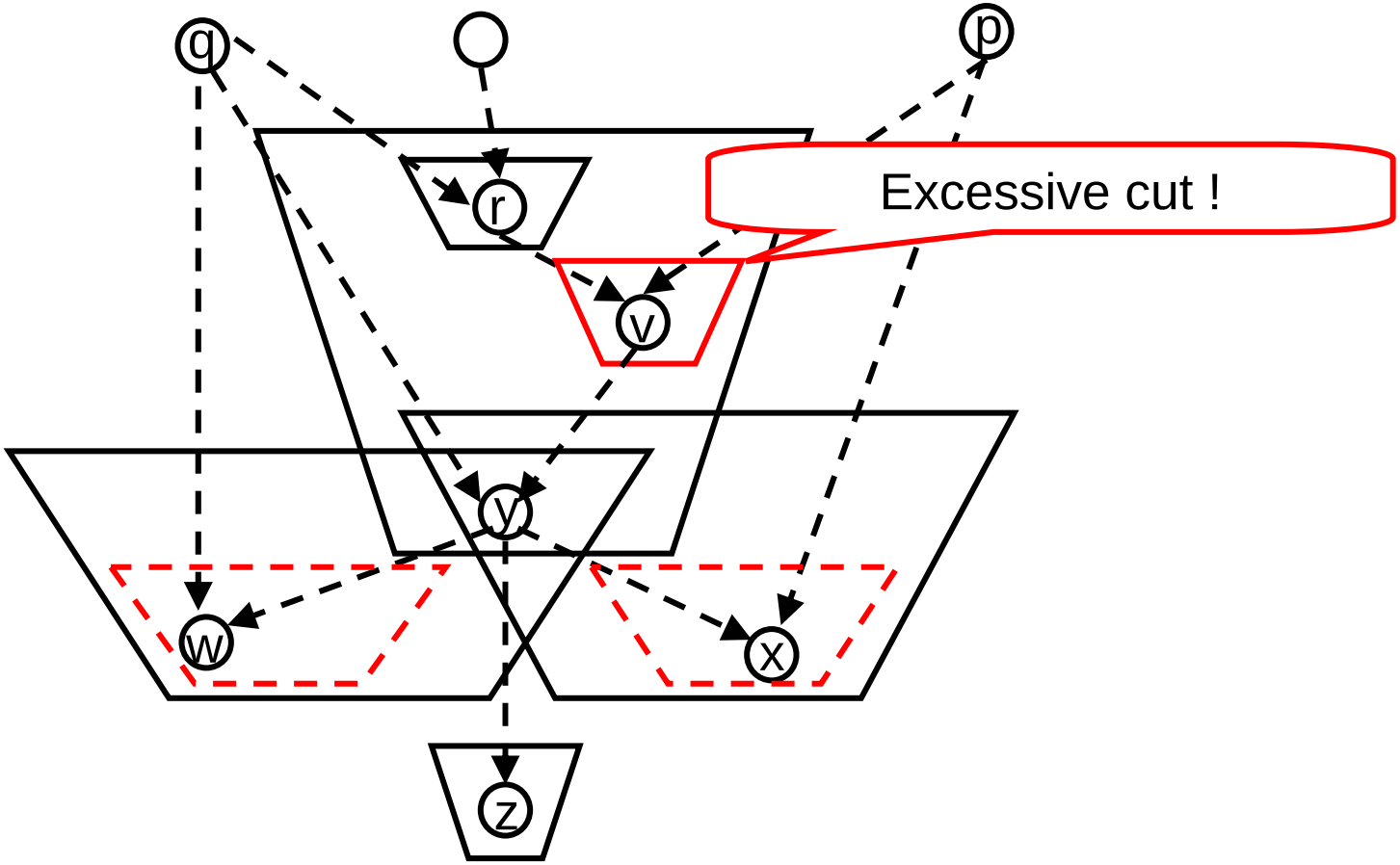
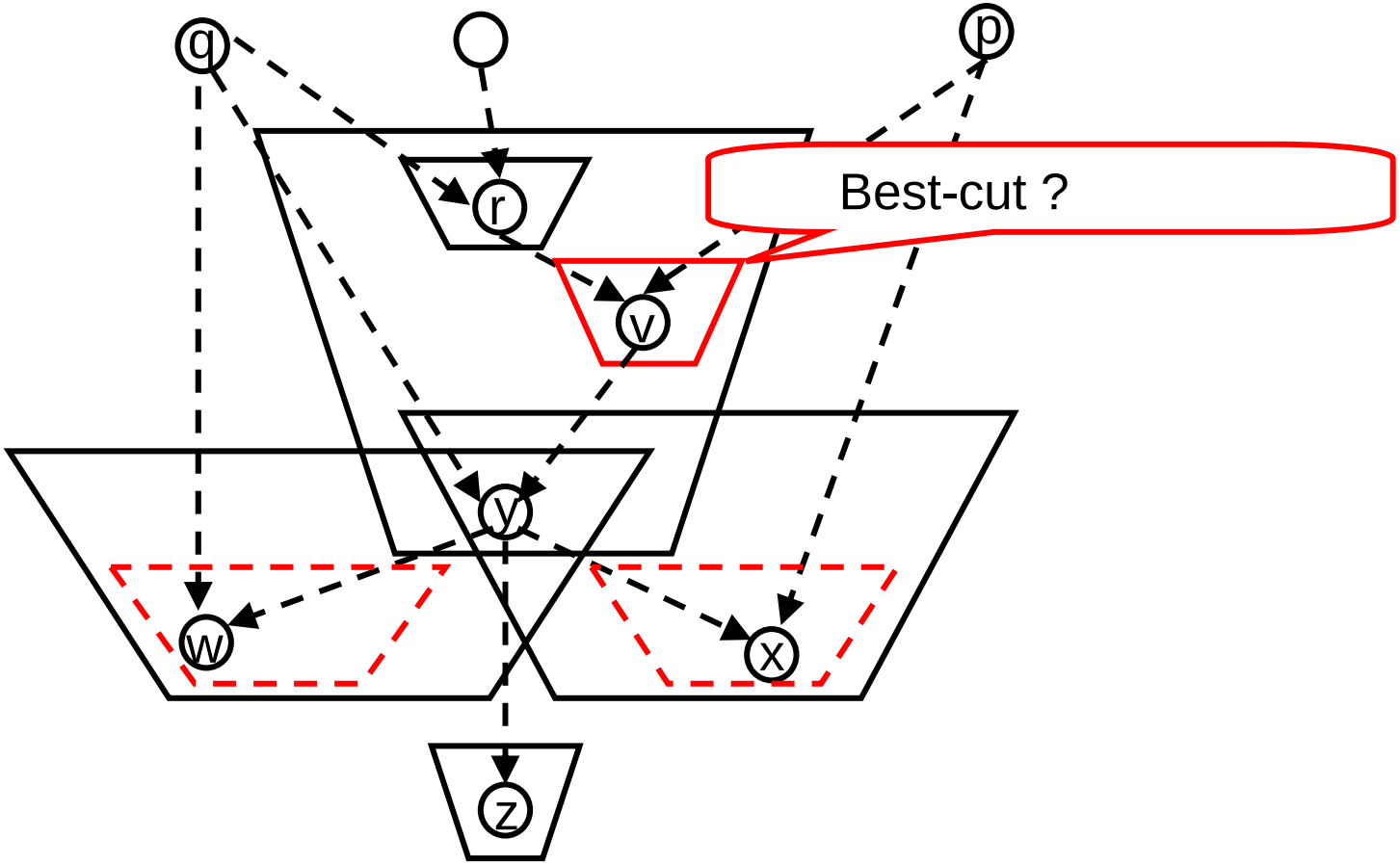


LUT network

The processing of a iteration of Cut Substitution

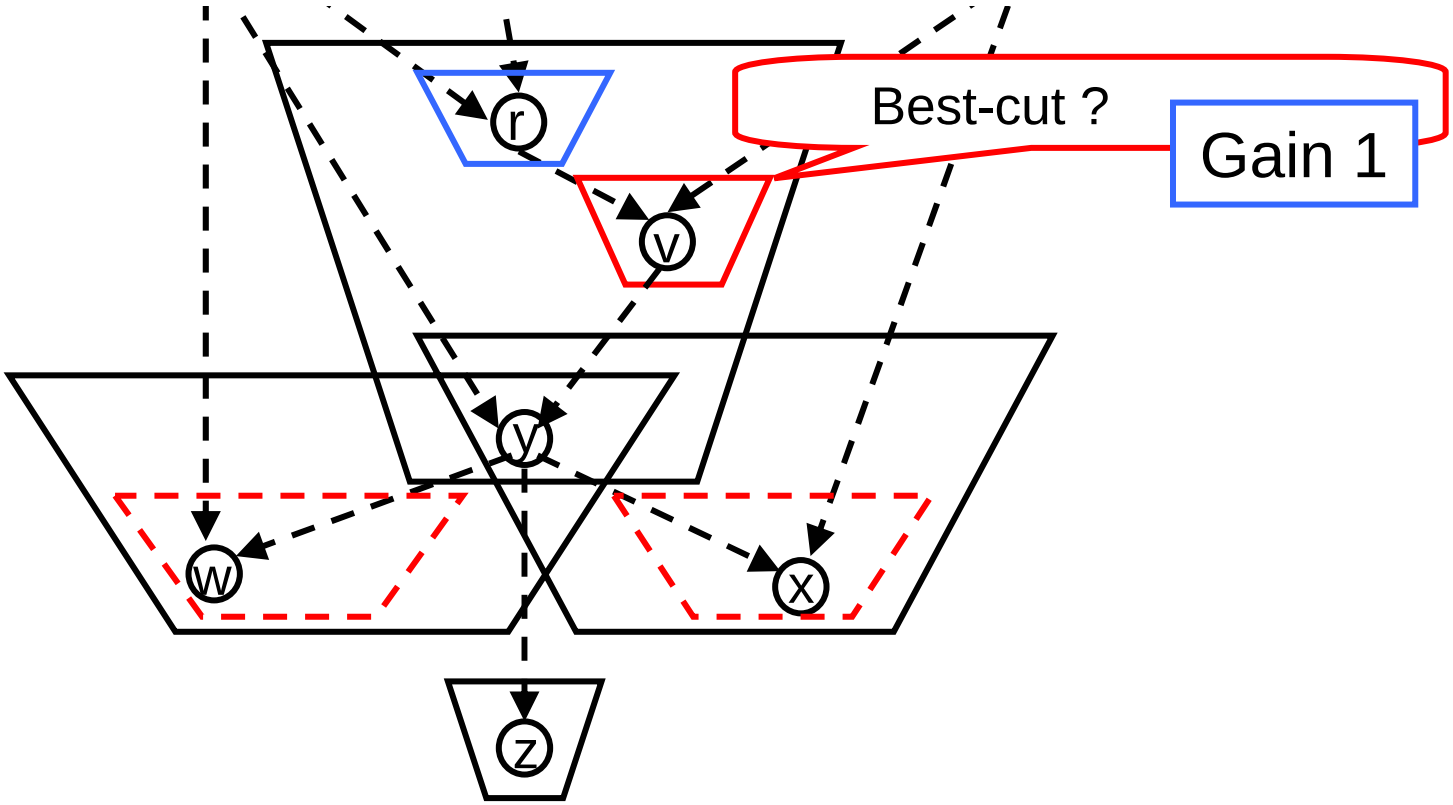
Phase 2 : Choice of a best-cut



LUT network

The processing of a iteration of Cut Substitution

Gain(v) : the number of cuts those are not necessary if v doesn't exist



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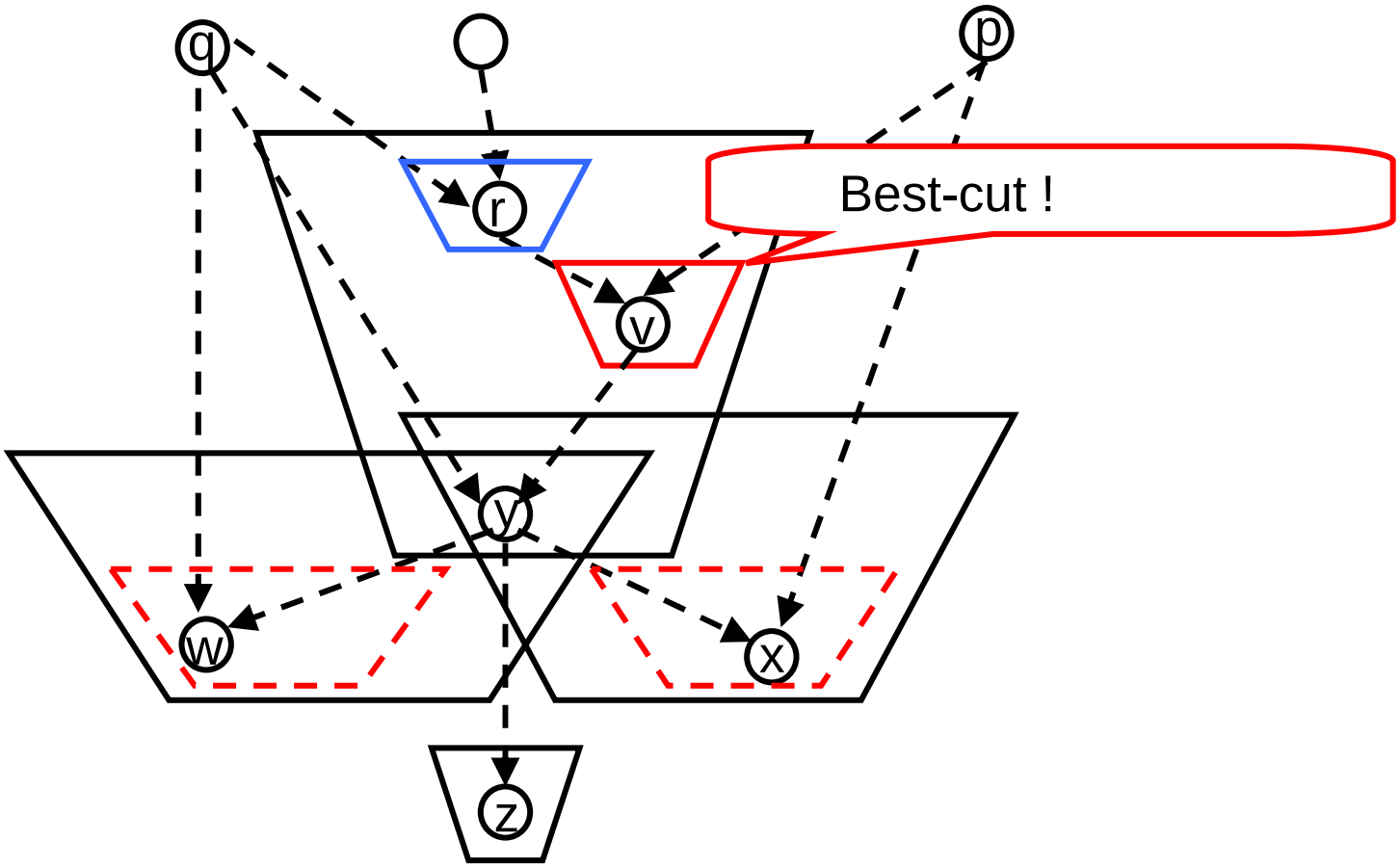

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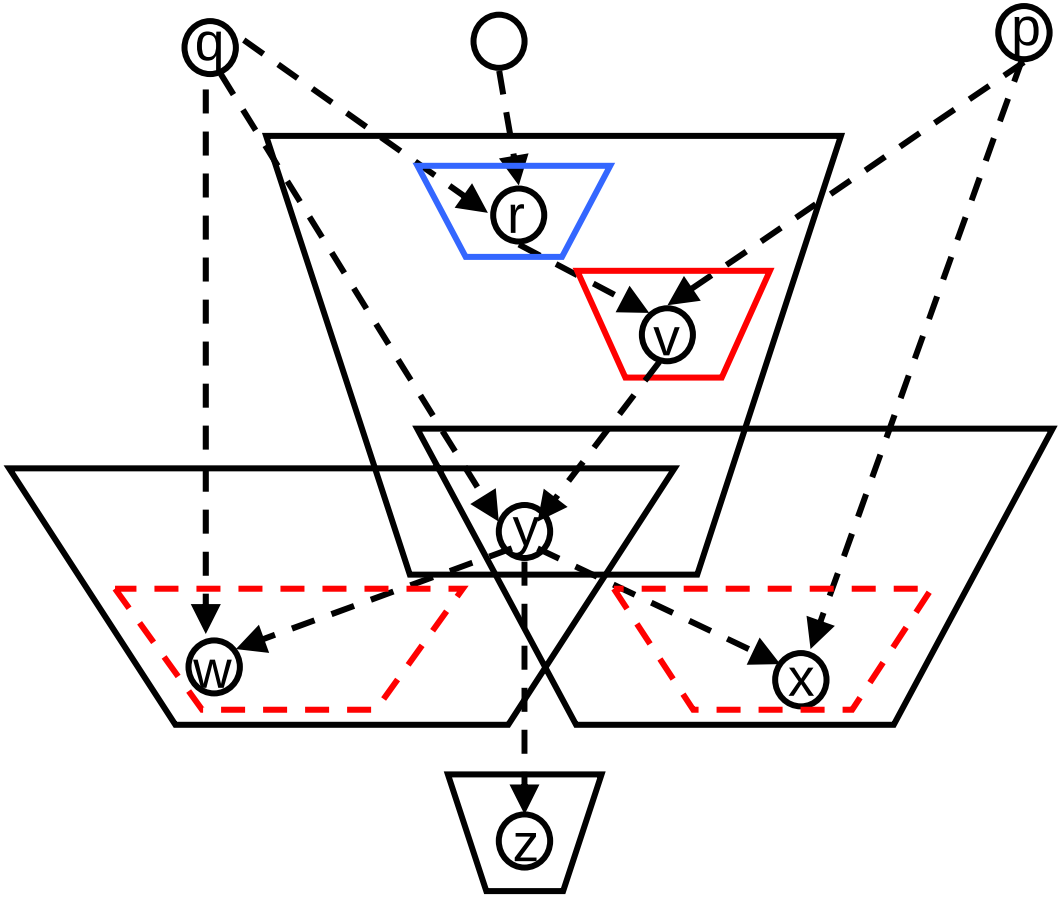
The processing of a iteration of Cut Substitution

Phase 3 : Cut elimination



LUT network

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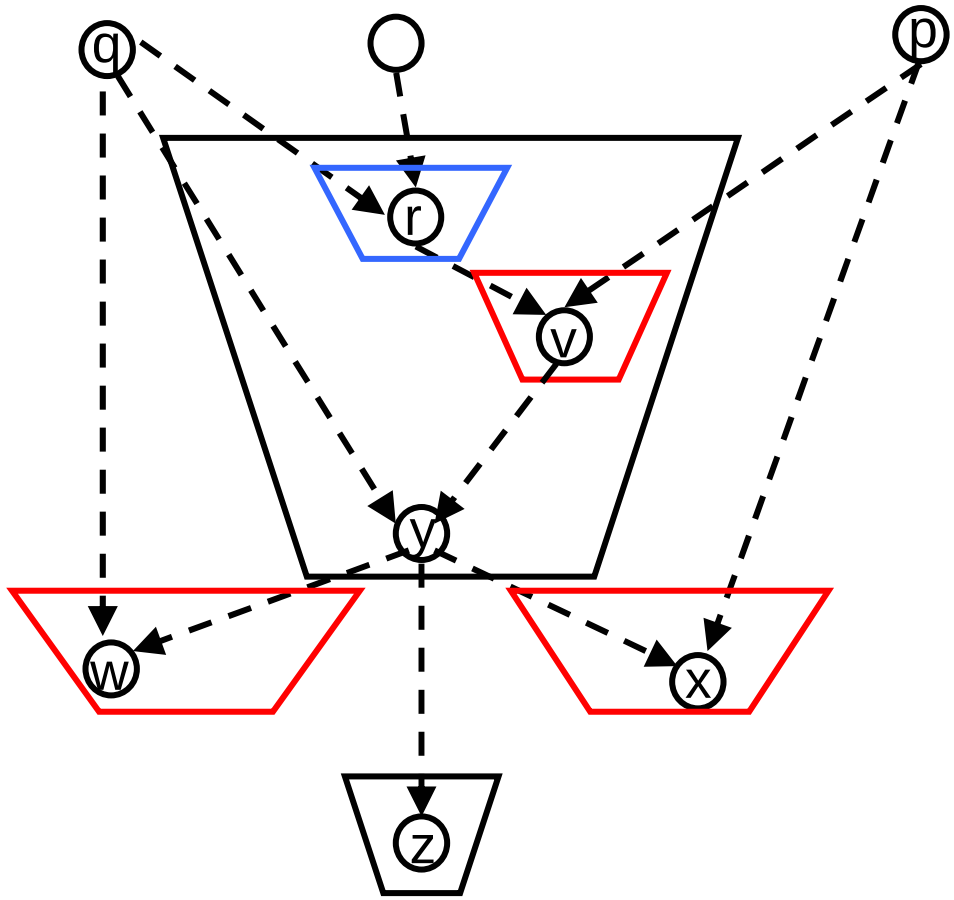

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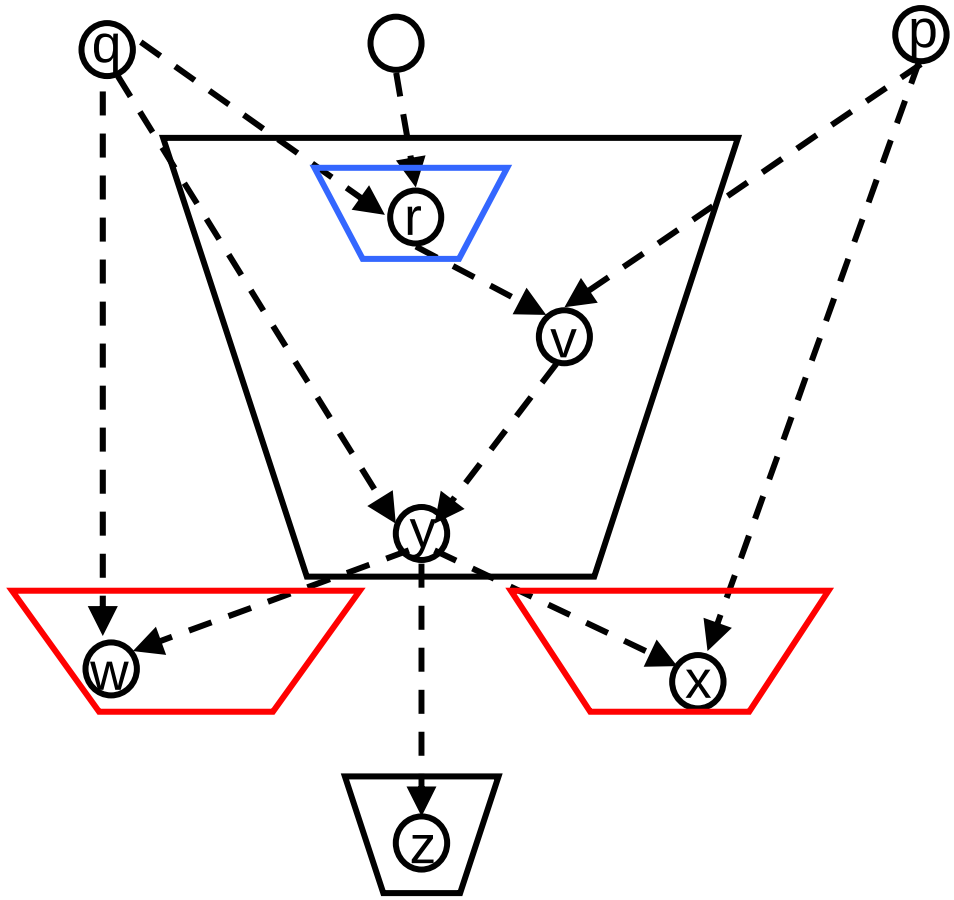

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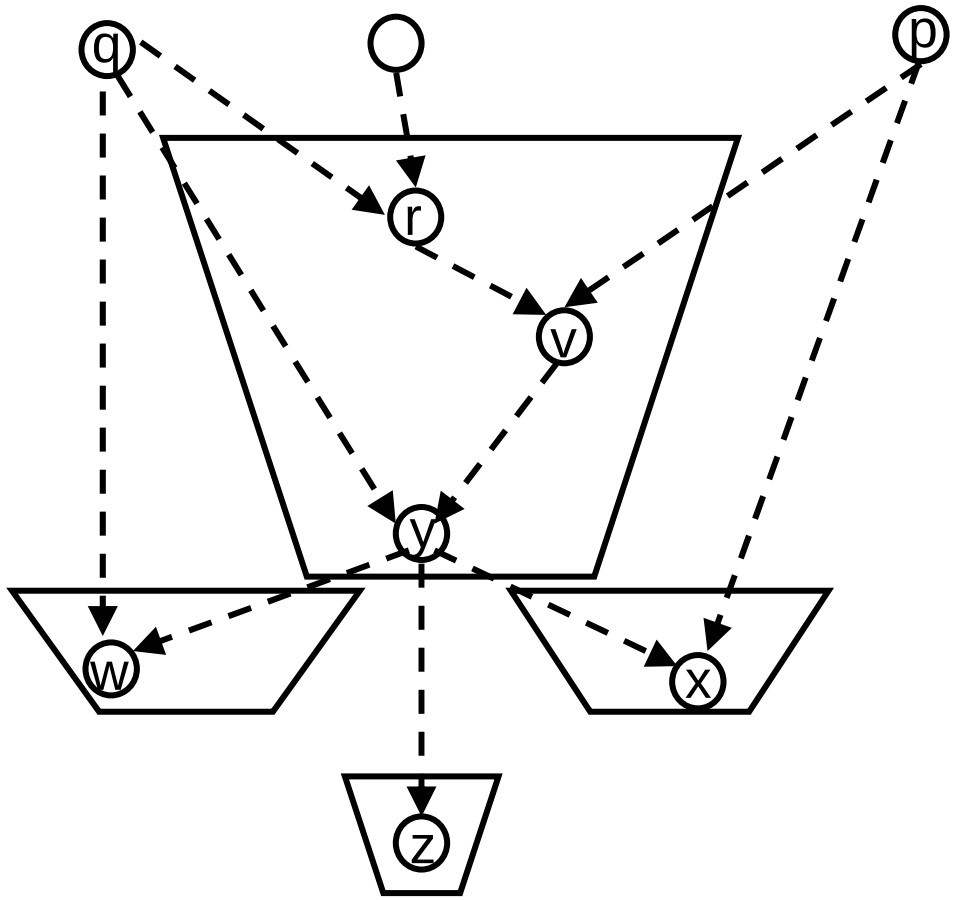
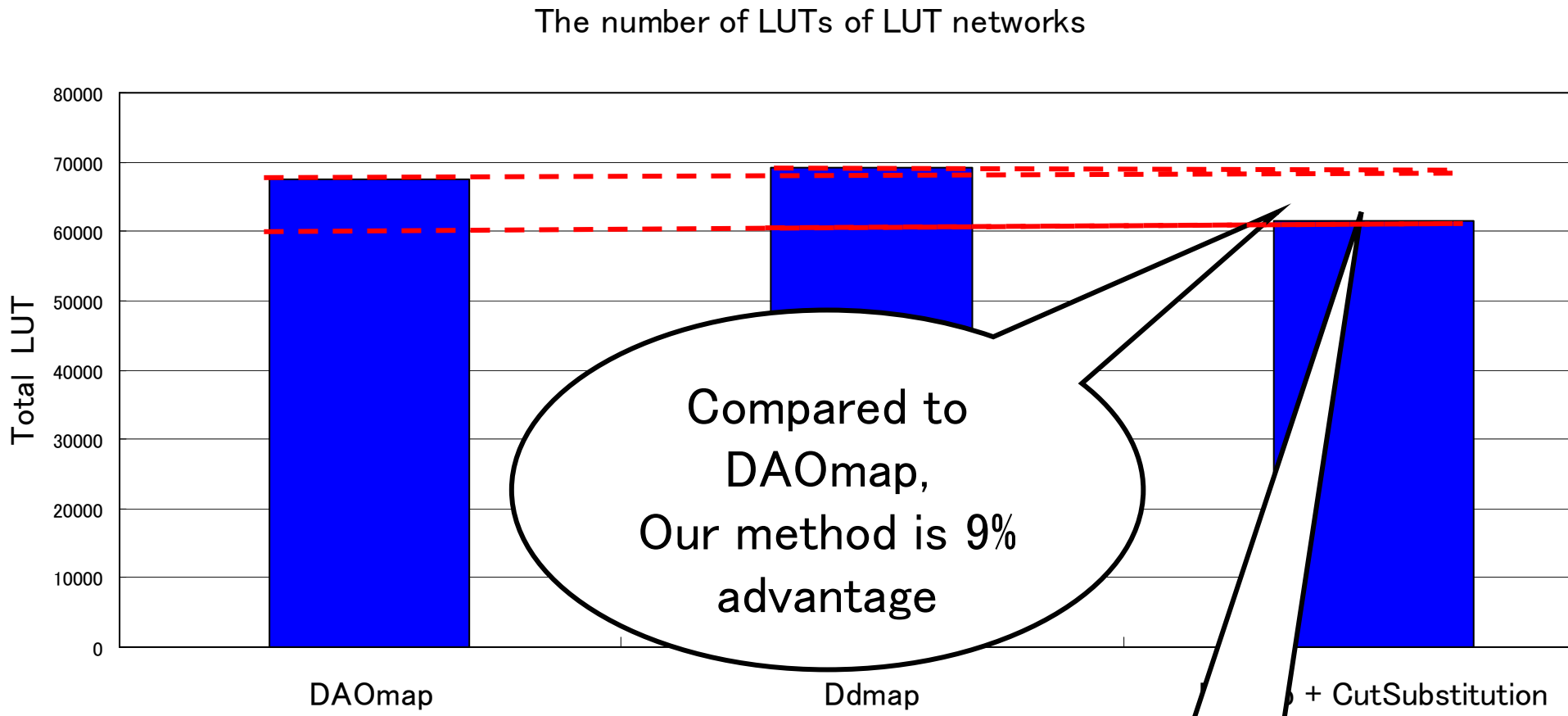


LUT network

Experiment

- Comparison of the number of LUTs of LUT networks
  - Cut Substitution --- our method
    - The initial selected cuts given to Cut Substitution are generated by Ddmap
      (Ddmap : A simple technology mapping algorithm to generate depth minimum network)
  - DAOmap --- Deming Chen, Jason Cong, 2004 [4]
    - A heuristic algorithm to generate area minimum network under depth minimum constraint
- Benchmarks
  - MCNC benchmark set
  - ITC'99 benchmark set
- Computing machine
  - CPU : Intel Xeon 3.0 GHz
  - Memory : 15 GB

Experimental results



The average run time of Ddmap + Cut Substitutio
is 3% shorter than that of DAOmap

Conclusion

- We presented Cut Substitution,
  the post-processing for technology mapping for LUT-based FPGAs to minimize area under depth constraint
- Ddmap + Cut Substitution generated networks with 9% less LUTs than the networks generated by DAOmap on average
  - The run time of Ddmap + Cut Substitution is 3% shorter than that of DAOmap
- Future work : examining the effect of Cut Substitution combined to other technology mapping algorithms

Thank you all for your attention

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  - Cut Substitution directly eliminates several excessive cuts from the set of cuts selected at technology mapping
- The processing of Cut Substitution is loop iteration

1. Excessive cut enumeration
   Enumerate all the excessive cuts among the selected cuts
2. Choice of a best-cut
   Decide a best-cut among the excessive cuts with a heuristic metric
3. Cut elimination
   Eliminate the best-cut by substitution of some other cut(s)