An optimal algorithm for sizing sequential circuits for industrial library based designs

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Motivation for sequential sizing

- Integrated circuit
  - Combinational blocks between flip-flops
- Optimize delay
  - Size each combinational block separately
    - Arrive at suitable clock frequency for circuit
  - Globally size the entire circuit
    - Combine sizing with clock skew optimization
    - Additional degree of freedom

Related work

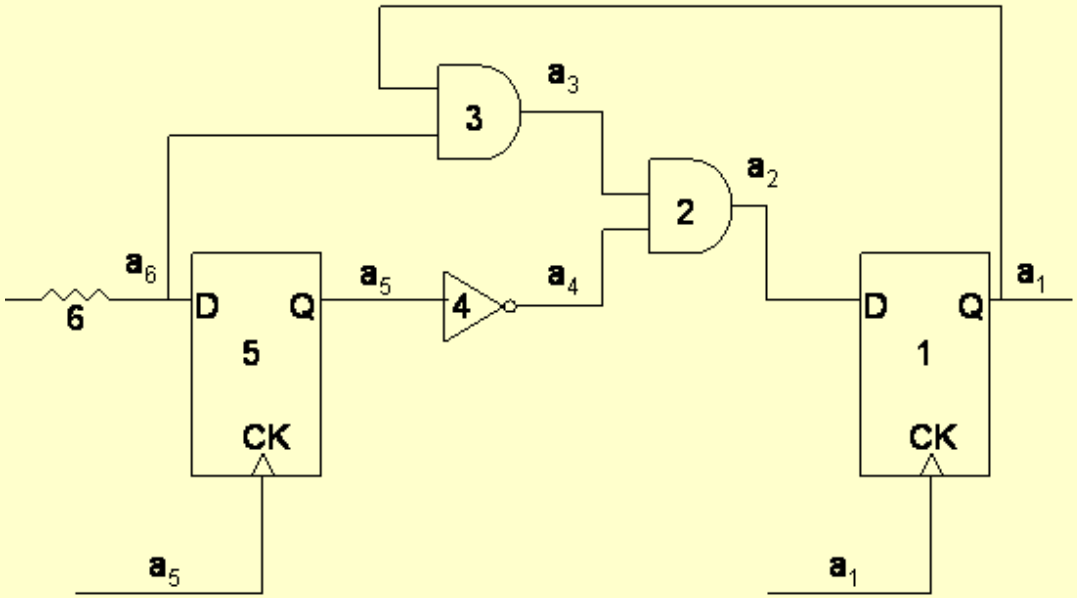
- Previous work on sequential optimization
  - Linear program [Chuang '95]
    - Piecewise linear models: limited accuracy
  - Nonlinear convex program [Sathyamurthy '98]
    - Elmore model: inaccurate for modern designs
  - Prohibitively large constraints for larger circuits
  - Previous methods target acyclic pipelines

Need efficient algorithms for handling large integrated circuits

Our sequential sizing formulation

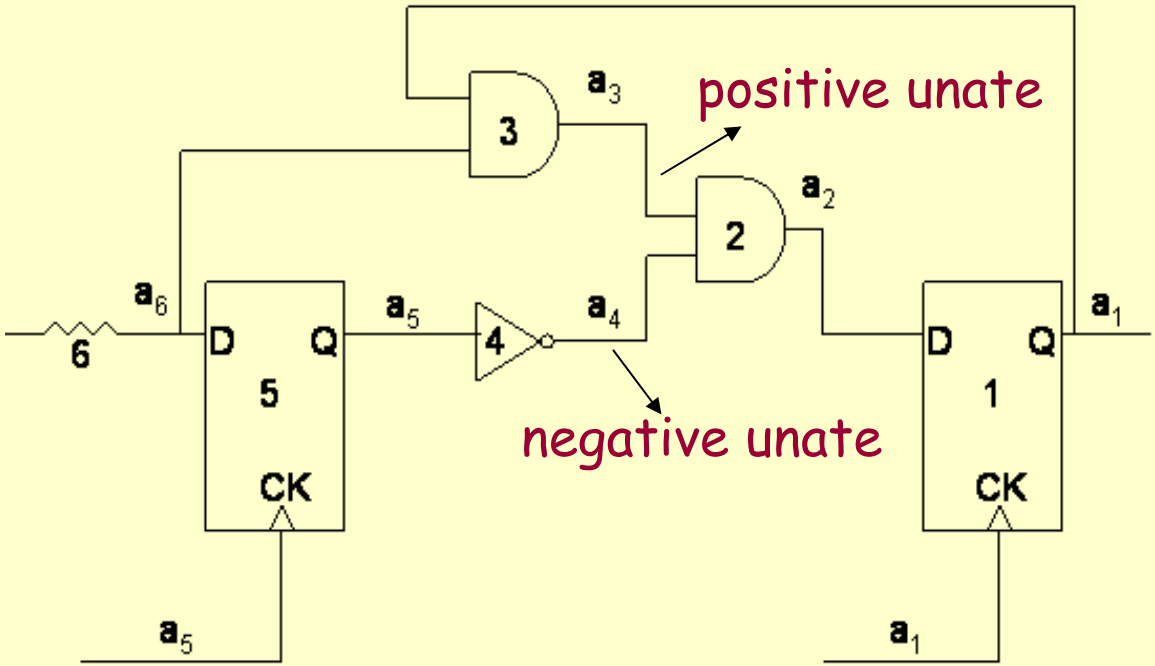
- Variables dependent on circuit components
  - Linear constraints and variables
- Can handle **cyclic** circuits
- Based on Lagrangian relaxation
- Uses posynomial models for delay
- For industrial library based designs

Sequential circuit optimization



- a_i: Arrival time of signal at output of gate i
- C: Clock period of the circuit
- Flip-flop clock-to-Q delay ignored in formulation
  - Clock skew at flip-flop i is a_i

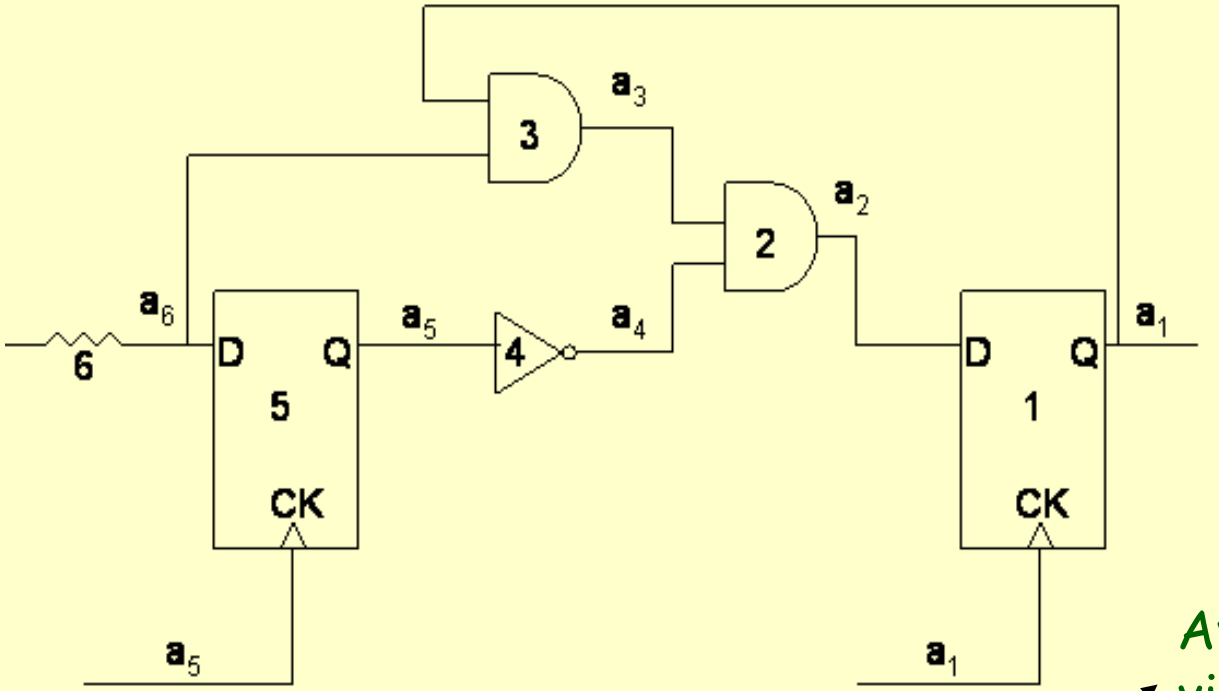
Constraints for combinational gates



$$a_3^{\,rise} + D_{32}^{\,rise}(s_3^{\,rise}, L_2, cap_2) \le a_2^{\,rise}$$

$$a_4^{\,fall} + D_{42}^{\,rise}(s_4^{\,fall}, L_2, cap_2) \le a_2^{\,rise}$$

Setup time constraints



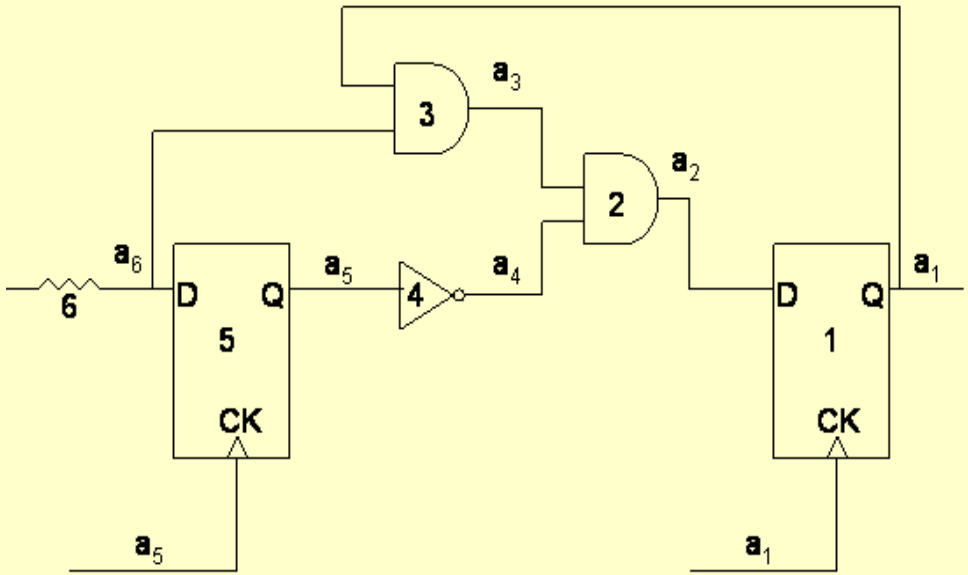
Avoid long path violations

$$Max(a_2^{rise} + t_{setup}^{rise}, a_2^{fall} + t_{setup}^{fall}) \le a_1 + C$$

$$a_2^{rise} + t_{rise}^{setup} \le a_1^{rise} + C$$

$$a_2^{fall} + t_{setup}^{fall} \le a_1^{fall} + C$$

Snapshot of problem formulation



$$\textit{minimize} \quad \alpha_1 C + \alpha_2 \sum_{j \in N} cap_j$$

s.t. *Combinational constraints*

Setup and Hold constraints

$$skew_{\min} \le a_1, a_5, a_6 \le skew_{\max}$$

Solution by Lagrangian Relaxation

- Solved using Lagrangian relaxation
- Troublesome constraints relaxed by incorporating into the objective function

$$\textit{minimize} \quad \alpha_1 C + \alpha_2 \sum_{j \in N} cap_j$$

$$\textit{s.t.} \quad a_3^{rise} + D_{32}^{rise} \le a_2^{rise}$$

$$bound_j^{lower} \le cap_j \le bound_j^{upper}$$

Solution by Lagrangian Relaxation

- Solved using Lagrangian relaxation
- Troublesome constraints relaxed by incorporating into the objective function

$$L_\lambda = \alpha_1 C + \alpha_2 \sum_{j \in N} cap_j + \lambda_{32}^{rise}(a_3^{rise} + D_{32}^{rise} - a_2^{rise})$$

Solution by Lagrangian Relaxation

- Solved using Lagrangian relaxation
- Troublesome constraints relaxed by incorporating into the objective function

$$\begin{aligned} &minimize && L_\lambda \\ &s.t. && bound_j^{lower} \le cap_j \le bound_j^{upper} \end{aligned}$$

Results: Optimized clock period

Circuit	Optimized clock period		Percent improvement %
	Sizing + skew (ns)	Sizing only (ns)	
s27.v	0.341	0.426	19.95
s298.v	0.866	1.269	31.76
s386.v	0.902	0.968	6.82
s444.v	1.070	1.192	10.23
s820.v	1.693	1.818	6.88
s5378.v	1.990	2.129	6.53
s13207.v	2.718	3.129	13.14

12.6% improvement in optimal clock period

Results: Area of optimized netlist

Circuit	Commercial Synthesis Tool $(\mu m)^2$	Sizing + skew $(\mu m)^2$	Reduction %
s27.v	168	99	41.07
s298.v	694	653	5.91
s386.v	554	499	9.93
s444.v	923	836	9.43
s820.v	1183	1011	14.54
s5378.v	7773	7688	1.09
s13207.v	20730	20283	2.16

11.3% average improvement in area

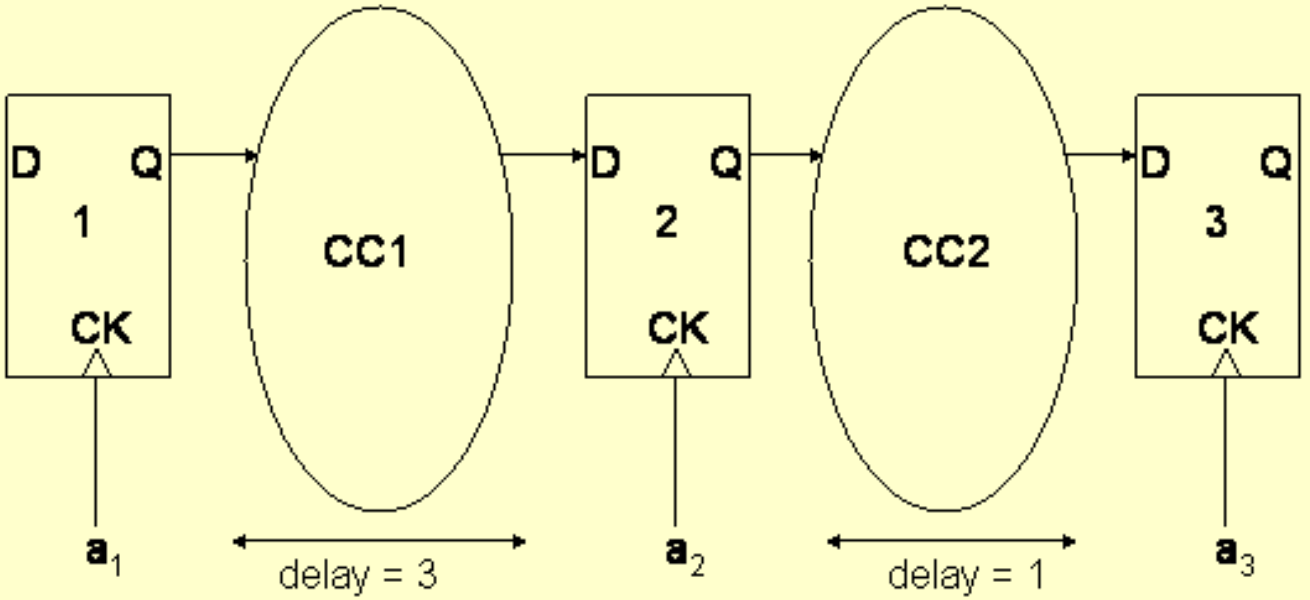
Conclusion

- Optimal gate sizing and clock skew optimization algorithm
- Target synchronous sequential circuits
- First algorithm to handle cyclic sequential circuits
- Results for industrial libraries

Thank You!

Backup slides

Clock skew optimization



- Intentional clock skews: better performance
- Minimum period 3 units: no skew
- With skew a_2 = +1 minimum period 2 units