Statistical Gate Delay Model for Multiple Input Switching

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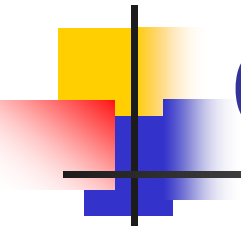
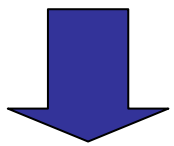


Outline

- Motivation
- Effect of Multiple Input Switching on the gate delay
- Gate Delay Model for Multiple Input Switching
- Experimental results
- Conclusions

Motivation

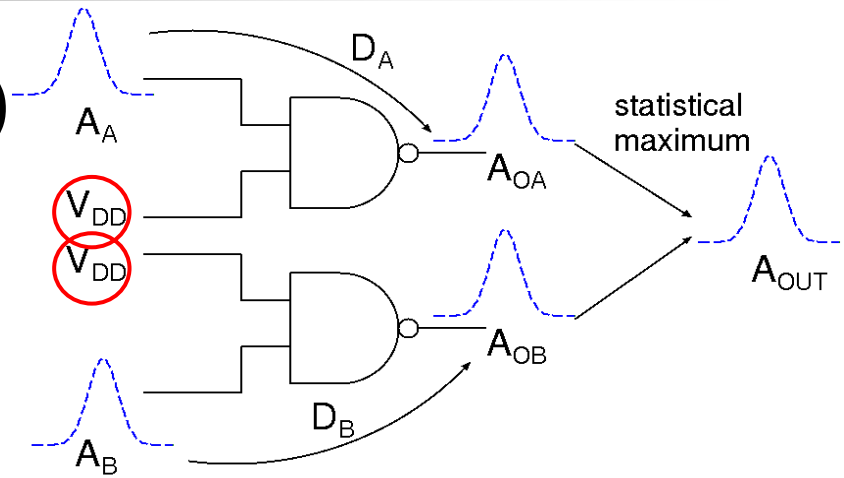
- Technology scaling
  - Increasing significance of process variations
  - Corner-based timing analysis become too pessimistic



- Statistical Static timing analysis (SSTA)
  - Statistical Max operation
  - Multiple input switching

Multiple Input Switching

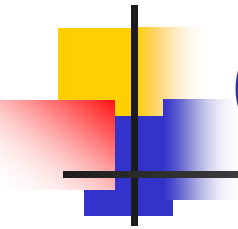
- Single Input Switching (SIS)
  - Only one of inputs switches
  - SIS assumption is correct when one input transition is away from the other



$$A_{OUT}=MAX(A_A+D_A,\ A_B+D_B)$$

- Multiple Input switching (MIS)
  - Two inputs switch at the same time
  - Gate delay is different from that of SIS

We propose gate delay model considering MIS effect



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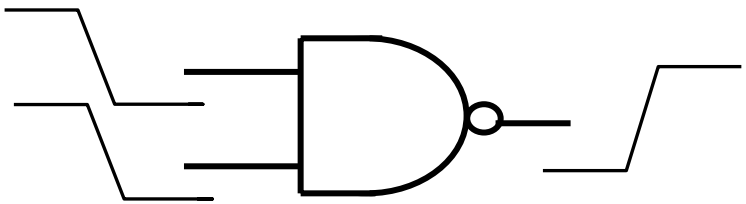
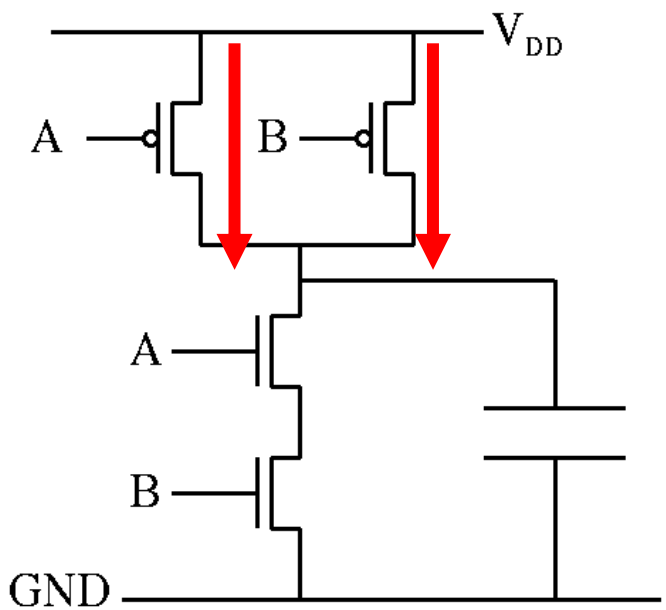
Multiple Input Switching

- SIS
  - One p-channel transistor turns on

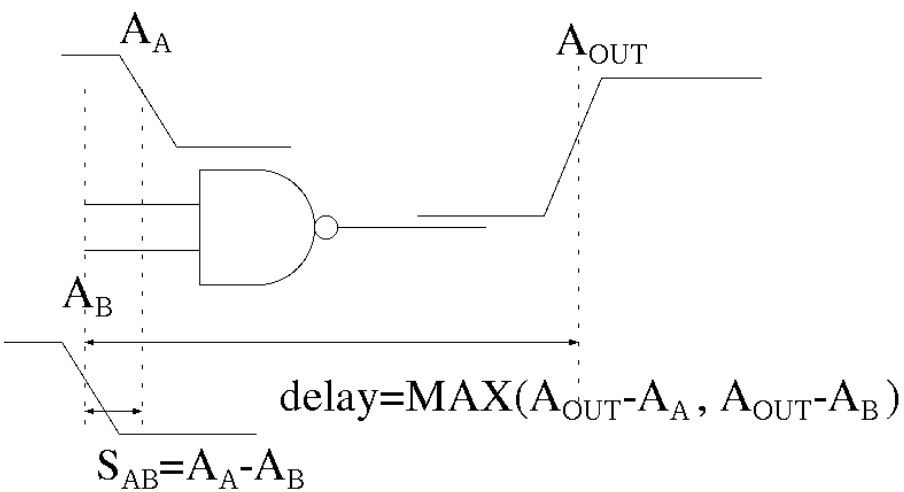


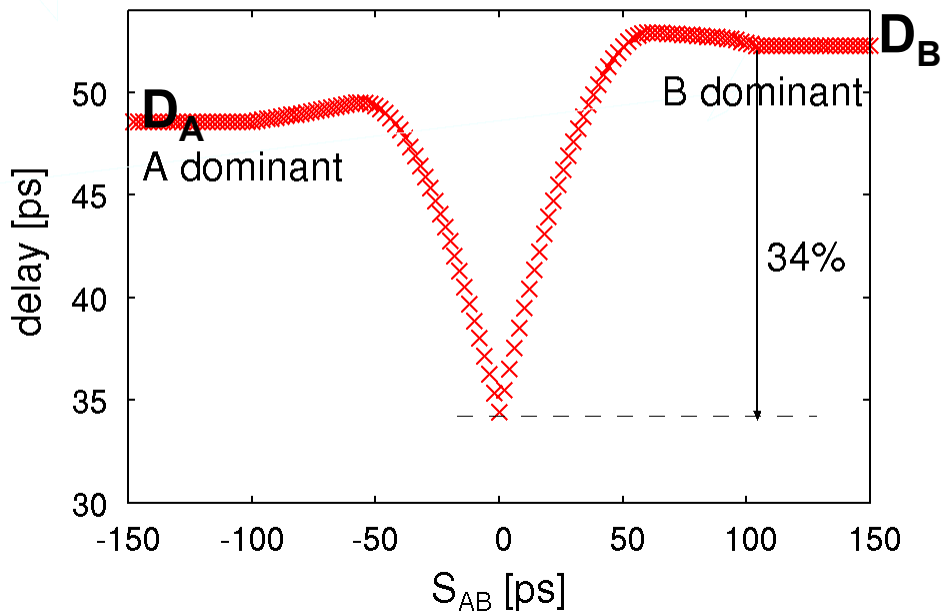
- MIS
  - Inputs A and B rise simultaneously
  - Two P-channel transistors turn on
  - Actual gate delay becomes smaller than that of SIS



Example of MIS effect

- Output rise when input A or B fall





A_A /A_B: Arrival time of input A / B

S_{AB}: Separation between A_A and A_B

Input transition time: 100ps

Output capacitance: FO4

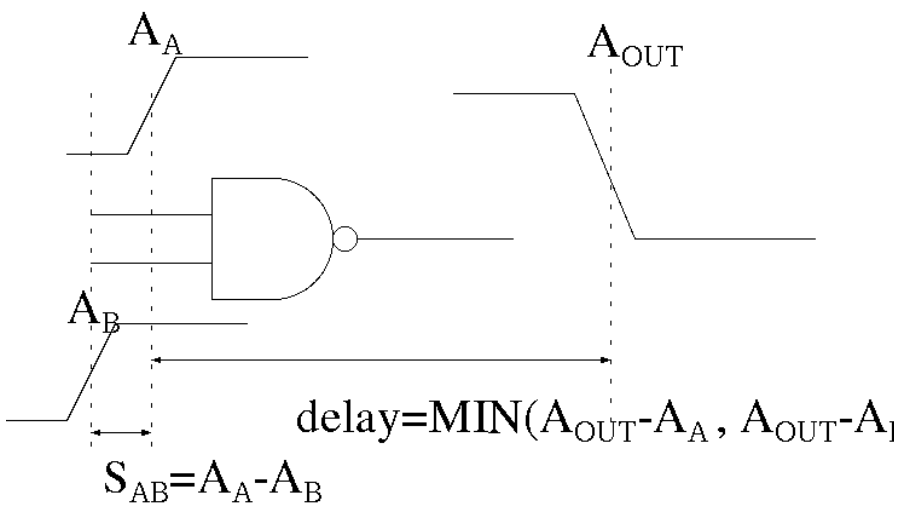
SIS: D_A 49ps

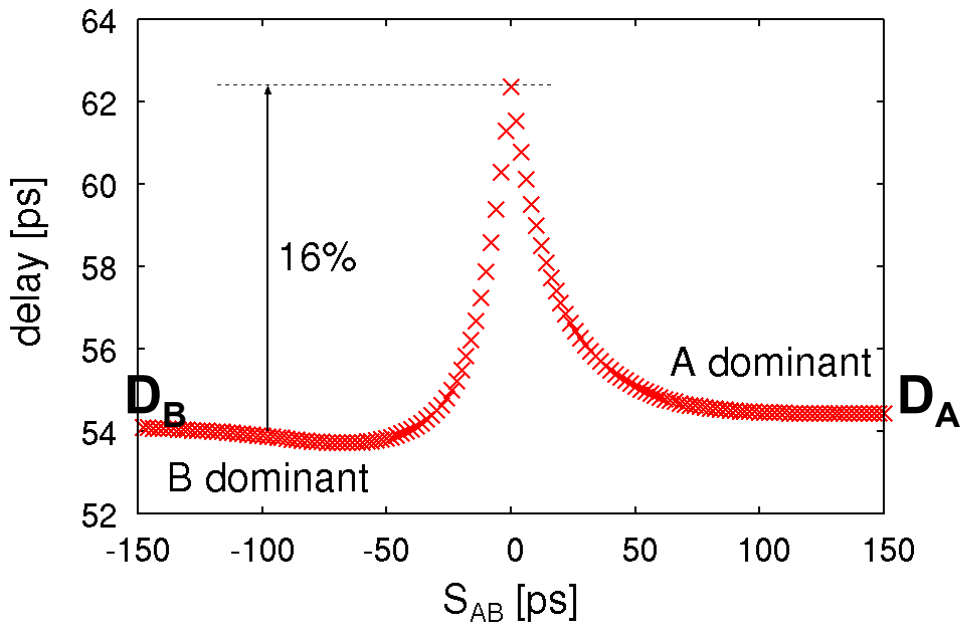
D_B 53ps

Actual gate delay changes by S_{AB} up to 34%

Example of MIS effect

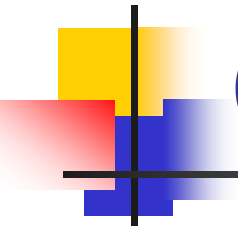
- Output fall when both inputs A and B rise





- Actual gate delay increases as S_{AB} gets close to 0
- MIS also affects output transition time

It is necessary to consider MIS effect



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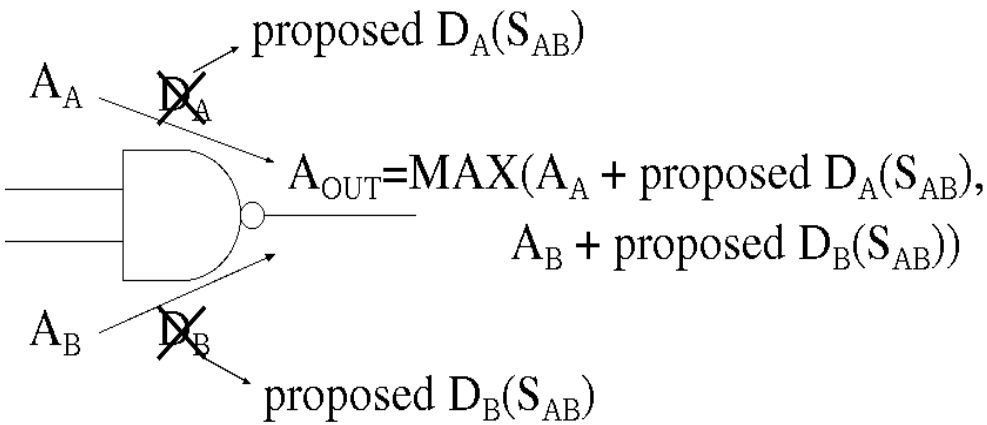
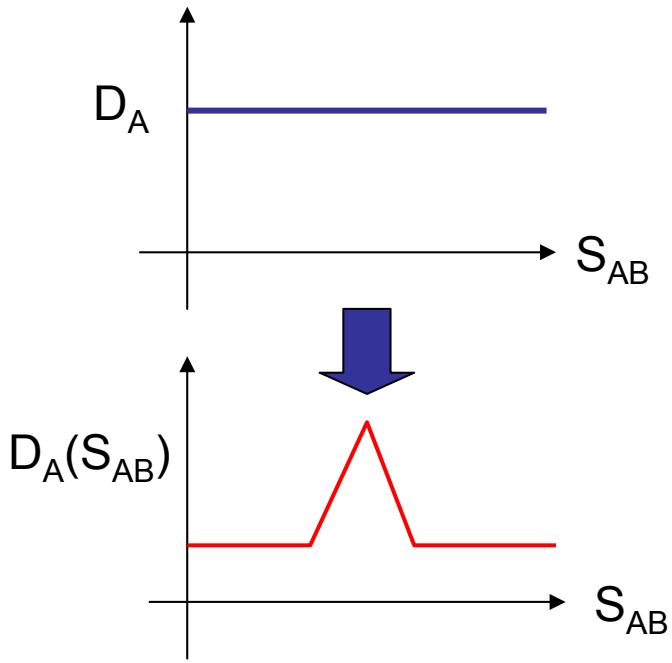
Proposed Gate Delay Model

- Replace conventional gate delay with the proposed gate delay
- Proposed gate delay model as a function of S_{AB}





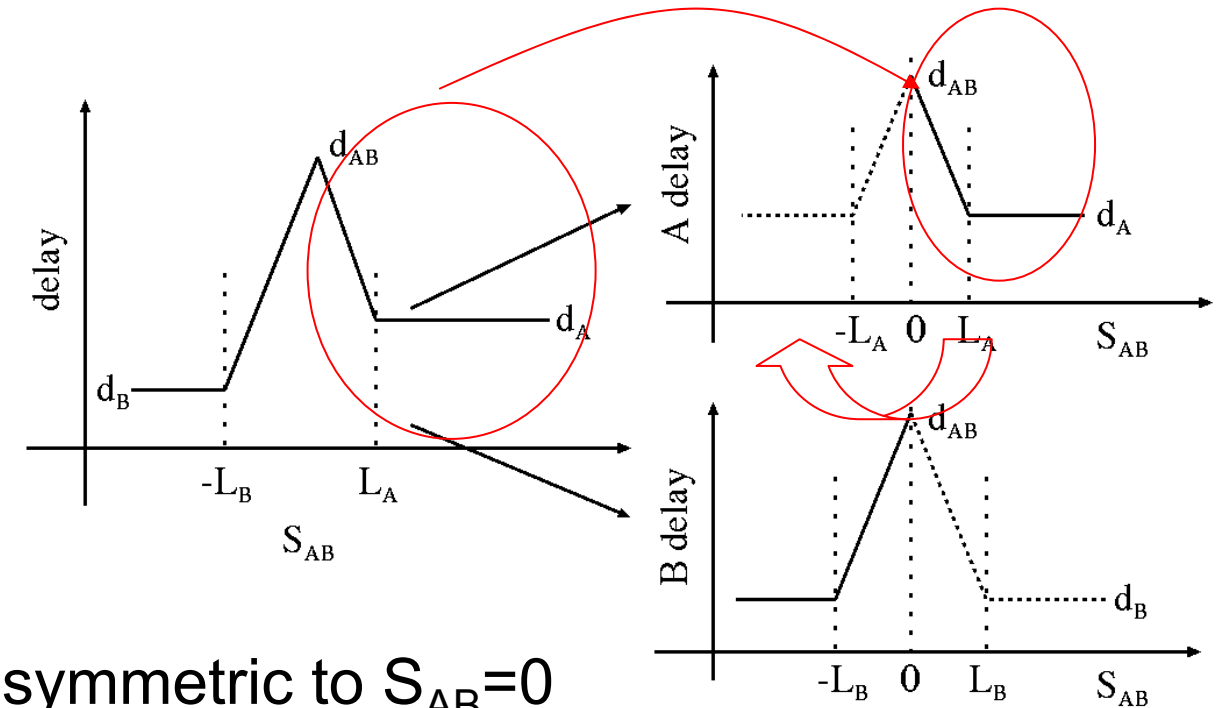
- Other parts are not changed (e.g. Max operation)

Estimation of proposed gate delay

- Proposed gate delay is a function of S_{AB}
- We estimate the proposed gate delay from SPICE results
- SPICE results: $A_{OUT}=MAX(A_A+D_A, A_B+D_B)$

When $A_A + D_A > A_B + D_B$,
$D_A = A_{out} - A_A$

When $A_A + D_A < A_B + D_B$,
$D_A = ?$



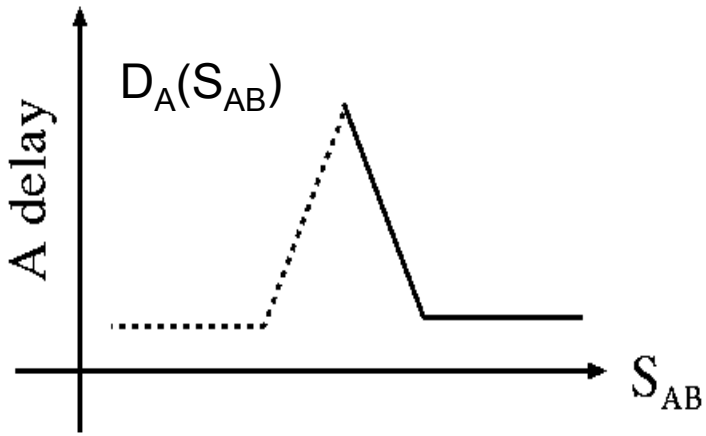
We assume $D_A(S_{AB})$ is symmetric to $S_{AB}=0$

μ and σ of Gate delay model

- Assume that all variations are normally distributed
- Calculate the mean and variance of $D_A(S_{AB})$, $D_B(S_{AB})$

$$\mu(D_A) = \int D_A(S_{AB}) p(S_{AB}) dS_{AB}$$

$$\sigma^2(D_A) = \int (D_A(S_{AB}) - \mu(D_A))^2 p(S_{AB}) dS_{AB}$$



Probability density function of S_{AB}: $p(S_{AB}) = \frac{1}{\sqrt{2\pi}\sigma_{AB}} \exp\left(\frac{(S_{AB} - \mu_{AB})^2}{2\sigma_{AB}^2}\right)$

- A_{OUT} = MAX(A_A + proposed D_A , A_B + proposed D_B)
  - MAX is calculated by Clark's method

Proposed method under gate length variations, etc.

- Canonical gate delay model can handle the effect of gate length variations, etc

Conventional gate delay $D_A = \mu_A + \sum_j \alpha_{A,j} r_j$

μ_A : mean of D_A

$r_j \sim N(0,1)$

Gate length variations, etc

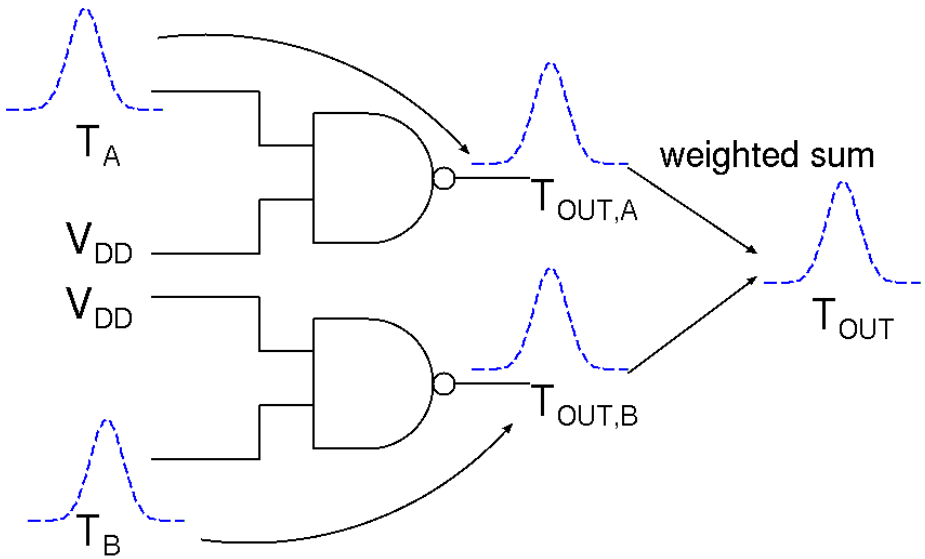
Proposed gate delay $D_A' = \mu_A' + \sum_j \gamma_{A,j} r_j + \sum_j \beta_{A,j} r_j$

S_{AB} variations

$$\gamma_{A,j} = \frac{\mu_A'}{\mu_A} \alpha_{A,j}$$

Estimation of output transition time

- Output transition time
  - $T_{OUT} = p\,T_{OUT,A} + (1-p)\,T_{OUT,B}$



$$p = P(A_A + D_A > A_B + D_B)$$

- Proposed method
  - Similar way to the proposed gate delay model
  - $T_{OUT,A}$ → proposed $T_{OUT,A}$ (S_{AB})
  - $T_{OUT,B}$ → proposed $T_{OUT,B}$ (S_{AB})

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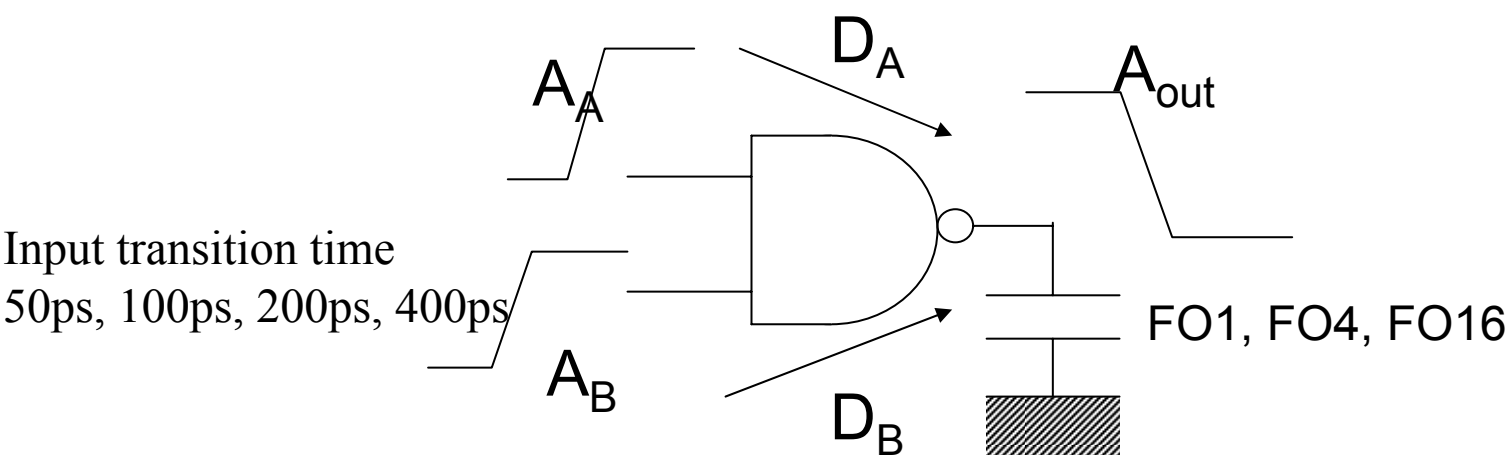
- Effect of Multiple Input Switching on the gate delay
- Gate Delay Model for Multiple Input Switching
- Experimental results
  - Result1 : only Sab is a statistical parameter
  - Result2 : Sab, Gate length, input transition time are statistical parameters
- Conclusions

Experimental setup

- Comparison with SPICE-based Monte Carlo Sim.
  - Conventional method

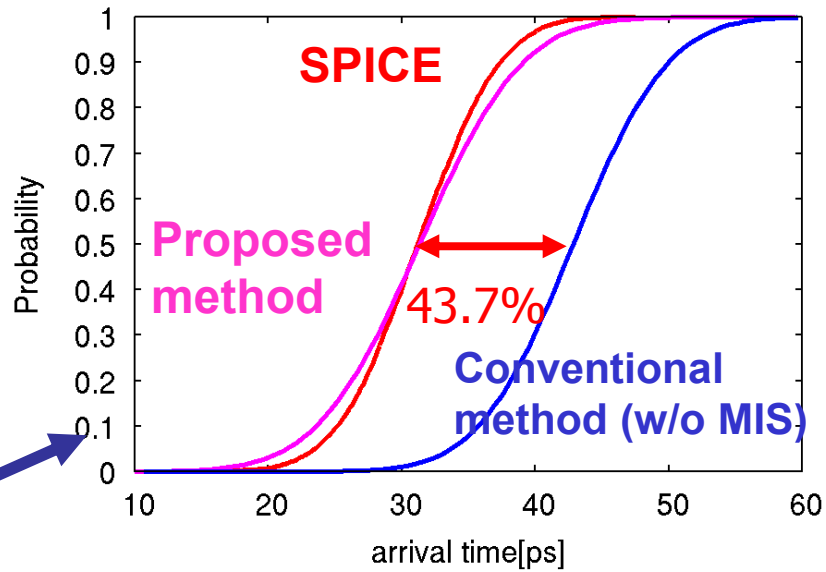
    A_{OUT} = MAX/MIN(A_A+D_A , A_B+D_B)
  - Proposed method

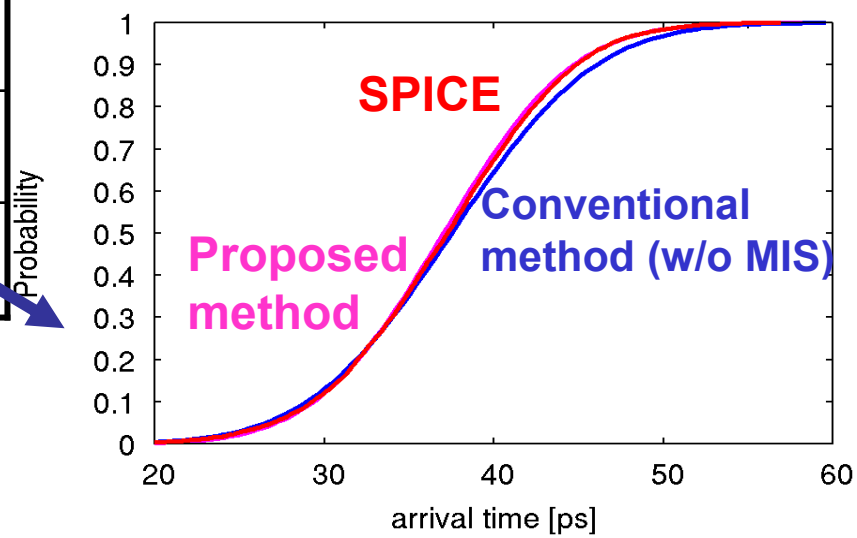
    A_{OUT} = MAX/MIN(A_A + proposed D_A , A_B + proposed D_B)
- S_{AB}: statistical parameter with normal distribution
  - e.g. S_{AB} ~N(0, 10), N(10,10) and so on



Example of experimental result

Mean of S_{AB} [ps]	Proposed method			w/o MIS		
	% error in μ	% error in σ	% error in $\mu+3\sigma$	% error in μ	% error in σ	% error in $\mu+3\sigma$
0	0.5	27.6	11.4	43.7	17.6	37.9
10	-0.7	5.9	1.6	34.1	22.3	33.3
20	-1.0	-0.7	-1.0	21.1	32.7	17.2
50	-0.2	-1.9	-0.8	0.9	9.1	3.7

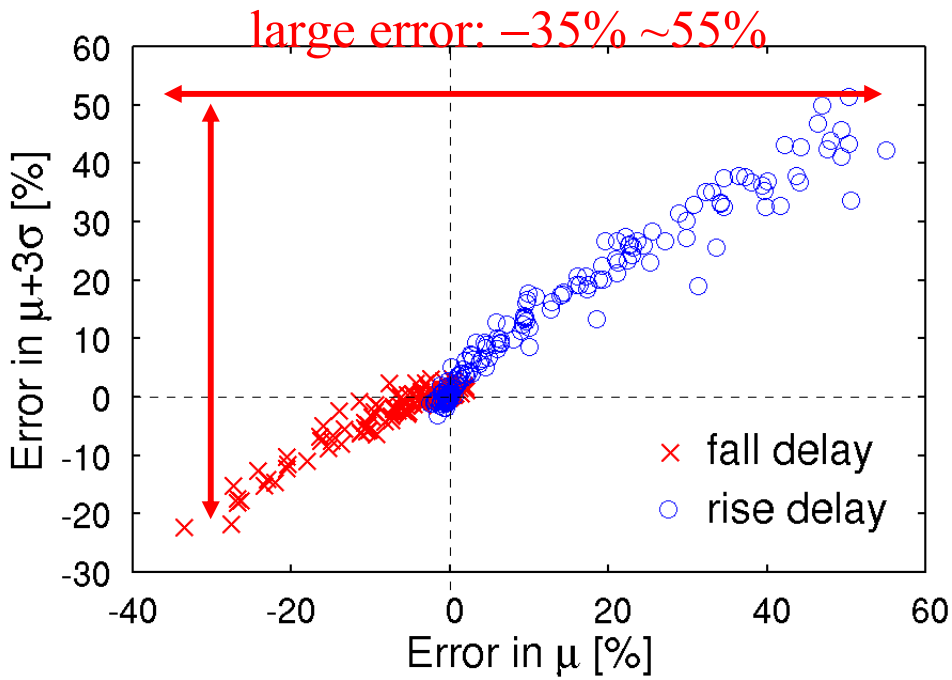




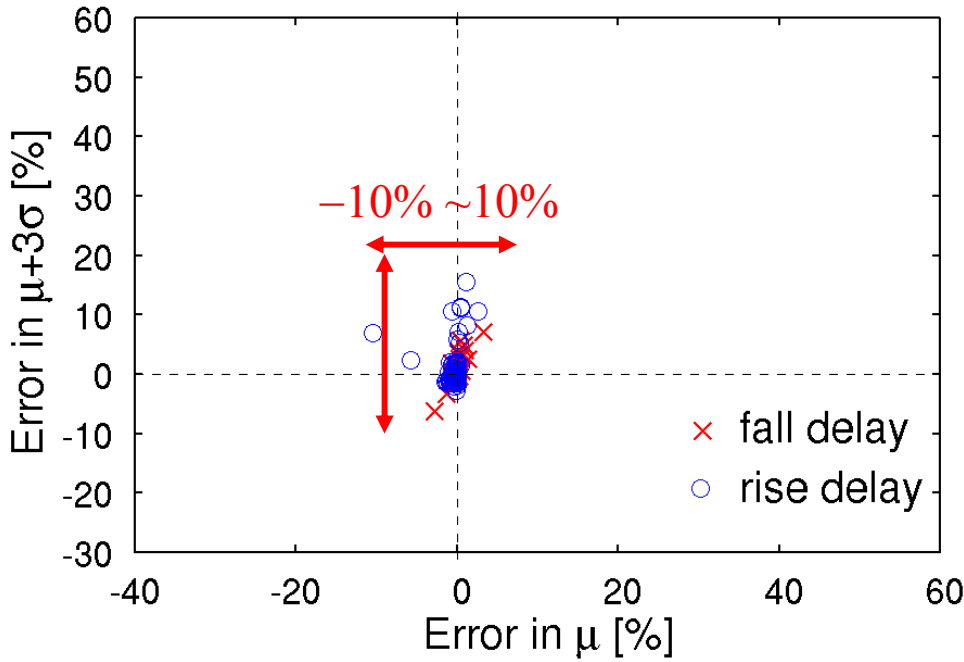
@ Rise delay
Input transition time: 100ps
Output capacitance: FO4

Result1

Input transition time: 50ps, 100ps, 200ps, 400ps
Output capacitance: FO1, FO4, FO16



Conventional method

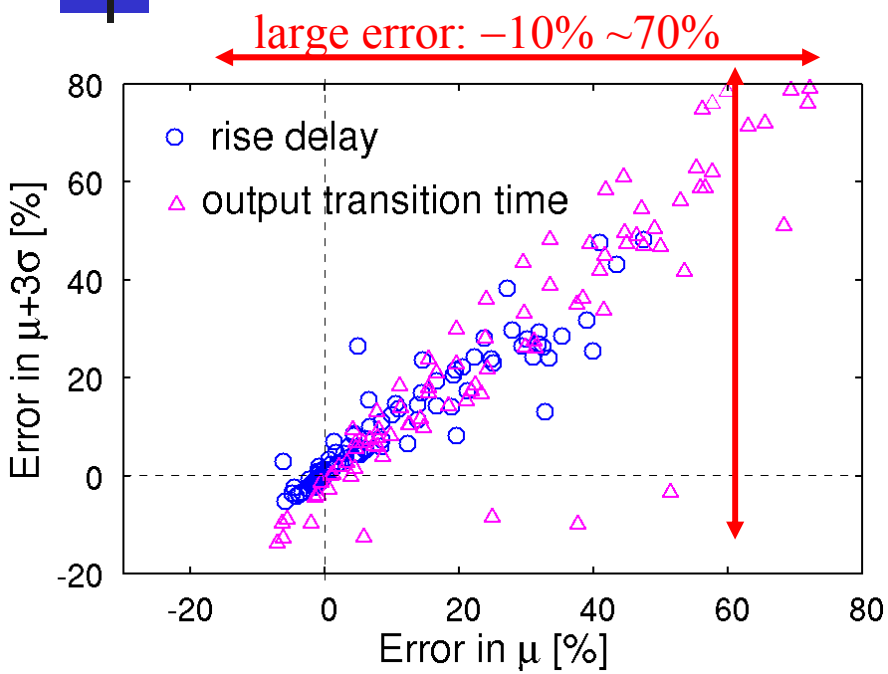


Proposed method

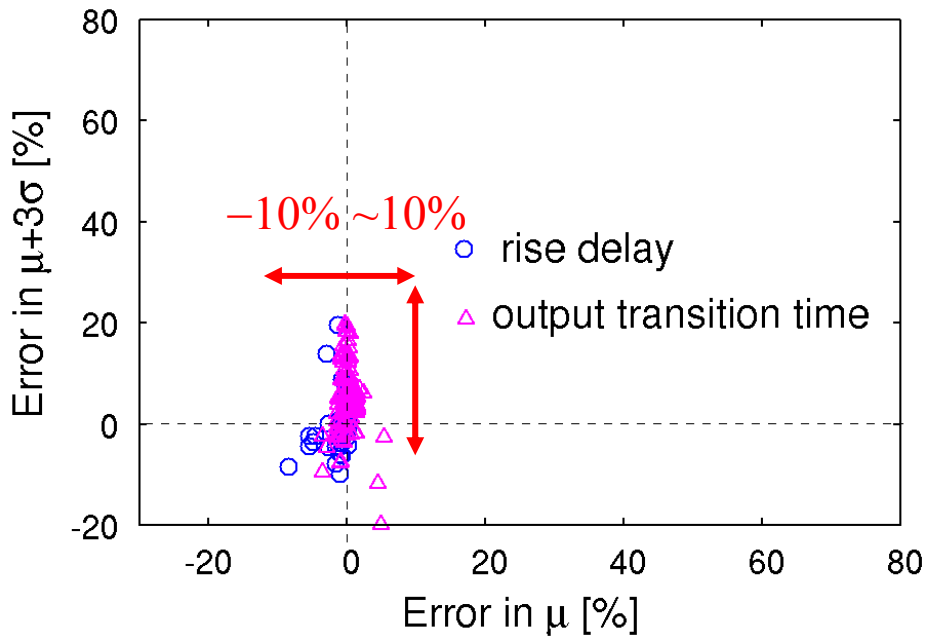
- Proposed method reduces the error

Result2

Rise delay
Gate length: ±20%, Input transition time: ±20%



Conventional method



Proposed method

- MIS have a significant effect on gate delay and output transition time
- Proposed method reduces the error by considering MIS effect

Conclusions

- Ignoring MIS cases the large error in statistical maximum operation in SSTA
- We propose the gate delay model considering MIS
- We show the proposed method reduce the error from 70% to 10%
- Future works
  - We need to reduce cell characterization cost