

Non-Gaussian Statistical Timing Models of Die-to-Die and Within-Die Parameter Variations for Full Chip Analysis

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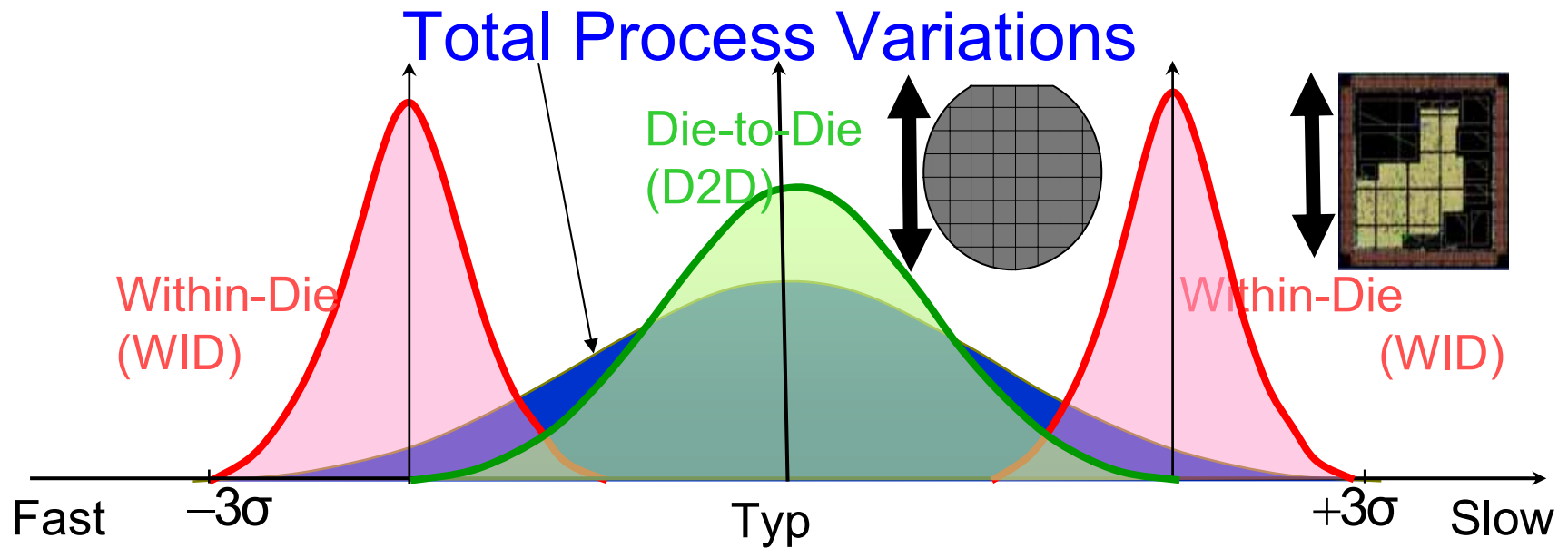
Motivation

- Process random variations are increasing with the advent of deep sub-micron technologies.
- Statistical Static Timing Analysis (SSTA) tools can be employed to verify timing and to predict timing yield.
 - Timing yield is essential for high-performance microprocessor designs to fabricate high ranked chips as many as possible.
- However, SSTA tools are still not efficient to handle the high-performance designs with so many critical paths.
 - Errors of statistical MAX operation are accumulated to be too large to ignore.
 - The delay distribution is not a Gaussian anymore.

Objectives:

- Propose fast, accurate, practical timing yield calculation method for high-performance designs.
 - Calculate statistical MAX iteratively with considering D2D correlation.
 - Adopt piecewise linear approximation to express the delay distribution.

Die-to-Die and Within-Die Variations



Delay Variation Model:

$$D = D_{typ} + dD_{intra_1} + \dots + dD_{intra_K} + dD_{inter}$$

dD_{intra_i} : WID elements, dD_{inter} : D2D element

Requirement for Delay Variation Model

- Non-Normality expression for statistical MAX
- Simple model for fast statistical calculation.

Our Delay Variation Model

We propose the following delay model for D2D and WID variations.

$$D = D_{\text{typ}} + dD_{\text{intra}} + dD_{\text{inter}}$$

dD_{intra} : WID element

- Independent for each gate or wire.
- Adopting piecewise linear approach.

dD_{inter} : D2D element + WID correlation

- $dD_{\text{inter}} = a_p * z$ ($z \geq 0$), $= a_n * z$ ($z < 0$) a_p, a_n : constant
 z : normal random variable common on the chip.

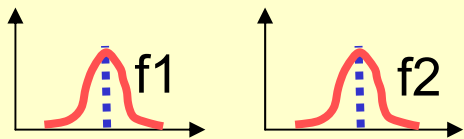
Timing yield can be practically predicted by using this model.

Y.Komatsu, H.Matsuoka, et al. , IPSJ Symposium Series vol.2006, no.7

Statistical Operations in SSTA

Statistical operations of WID and D2D elements.

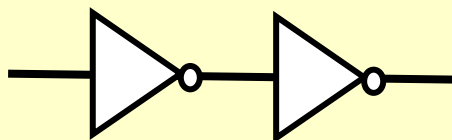
WID



$$f(t) = \int_{-\infty}^{\infty} f_1(t-s)f_2(s)ds$$

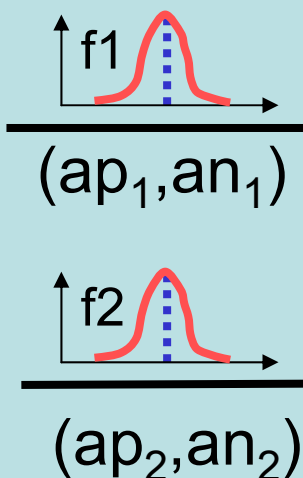
Convolution

Statistical
ADD



$$\text{D2D } (ap_1, an_1) (ap_2, an_2) = (ap_1 + ap_2, an_1 + an_2)$$

Statistical
MAX

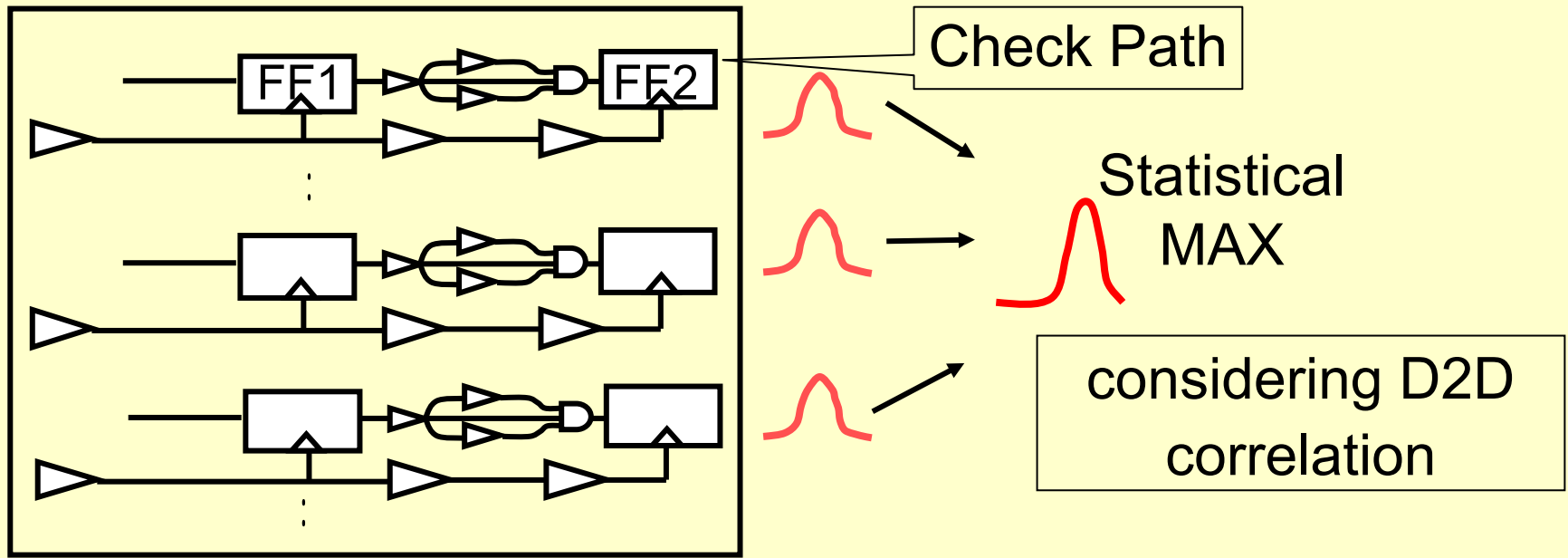


$$f(t) = f_1(t)F_2(t) + F_1(t)f_2(t)$$

F_1, F_2 : CDF of f_1, f_2
 f_1, f_2 : non-independent
 then f : upper bound

$$= (\max(ap_1, ap_2), \min(an_1, an_2))$$

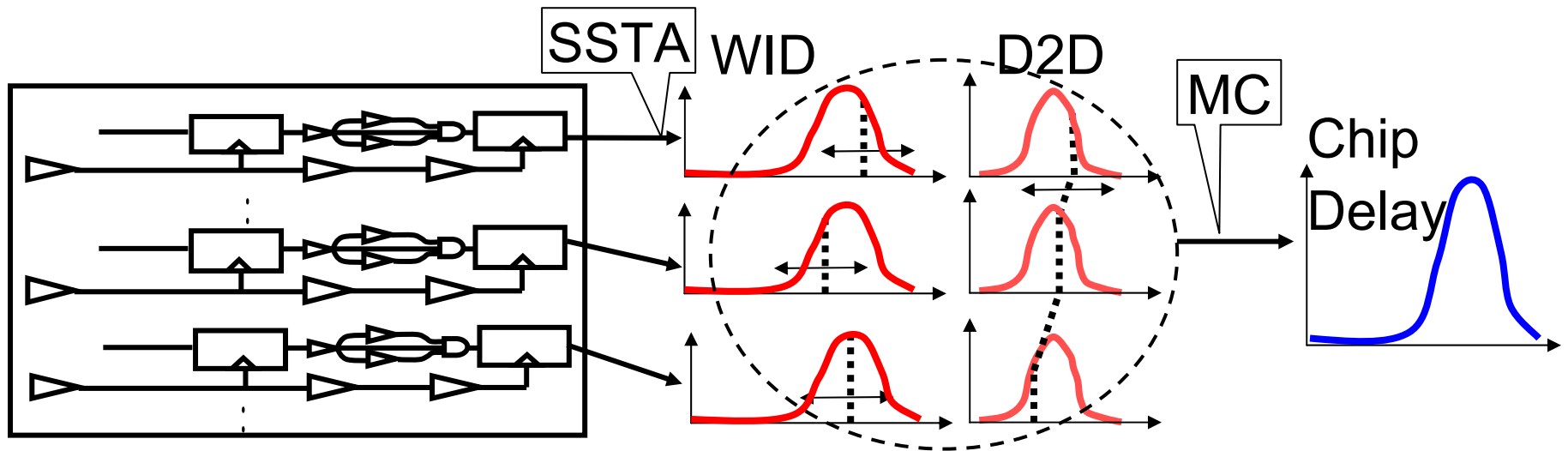
Definition of Chip Delay Distribution



Chip Delay Distribution = $S_{\max}(\text{Check Path Delay Dist.})$

Precise method considering WID and D2D is full-chip Monte Carlo simulation but too time-consuming.

Practical Monte Carlo Method

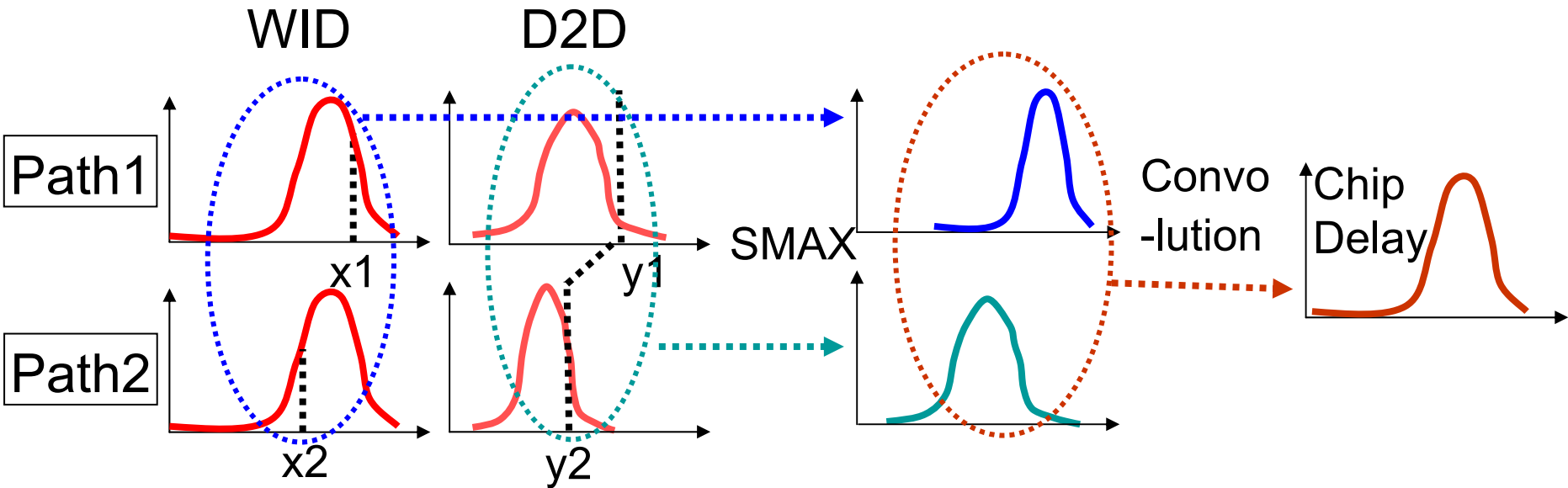


- Step1: Calculate WID and D2D distributions of each check path by SSTA method.
- Step2: Calculate the chip delay distribution by Monte Carlo using each path WID and D2D distributions

Practical Monte Carlo Method is still time consuming

A. Agarwal et al. proposed fast computing methods in Proc. ICCAD'03, pp900-907.

Previous Method 1

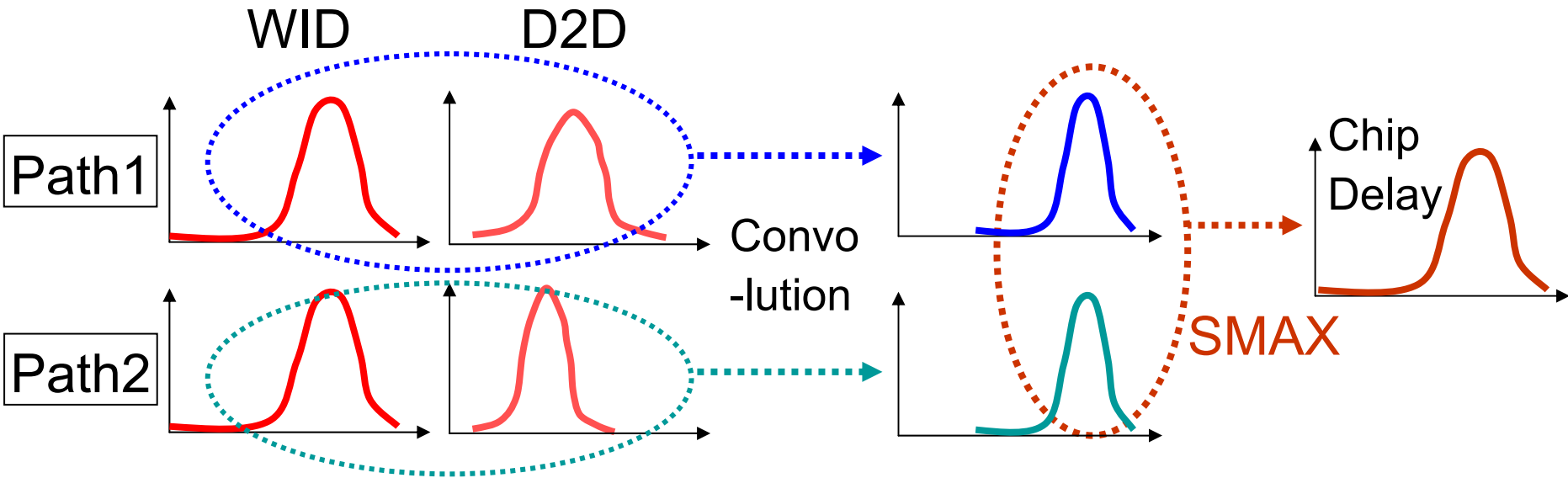


- Step 1: Calculate SMAX of WID distributions and SMAX of D2D distributions.
- Step 2: Calculate the convolution of these two distributions.

Error increases with the number of paths.

- The method calculates the distribution of $\max(x_1, x_2) + \max(y_1, y_2)$.
 - The random variable of SMAX is $\max(x_1 + x_2, y_1 + y_2)$.
- $$\max(x_1, x_2) + \max(y_1, y_2) \geq \max(x_1 + x_2, y_1 + y_2).$$

Previous Method 2

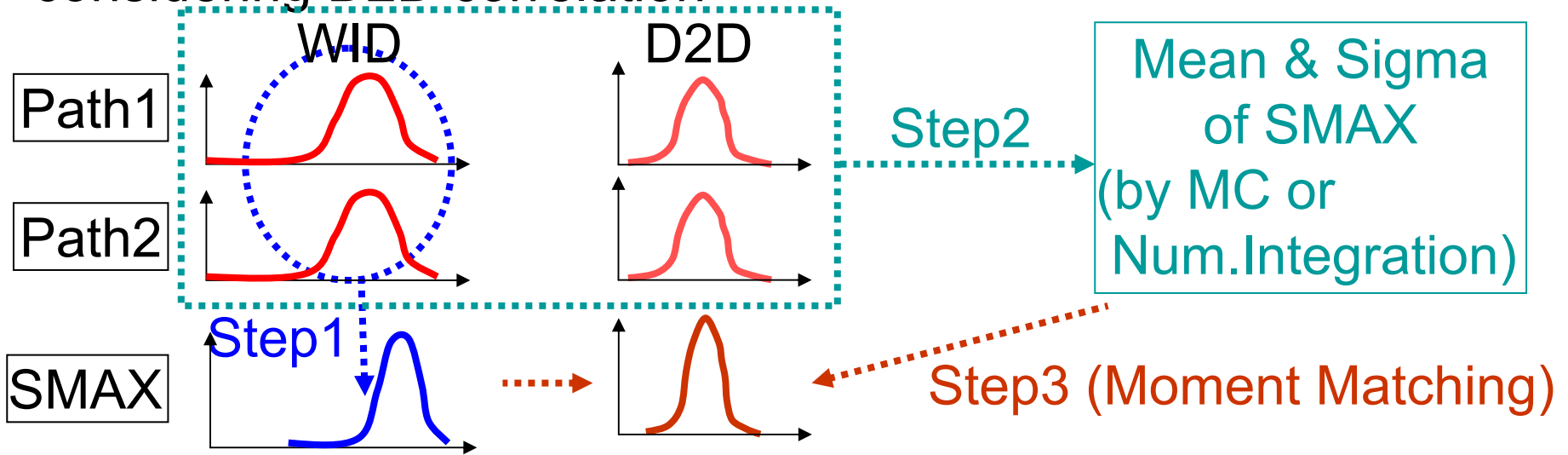


- Step1: Calculate the convolution of WID and D2D distributions of each path.
- Step2: Calculate SMAX of these distributions for all paths.

Error increases with the number of paths.
•The method ignores D2D correlations.

Proposed Method (1)

Calculate WID and D2D elements of Statistical MAX distribution considering D2D correlation

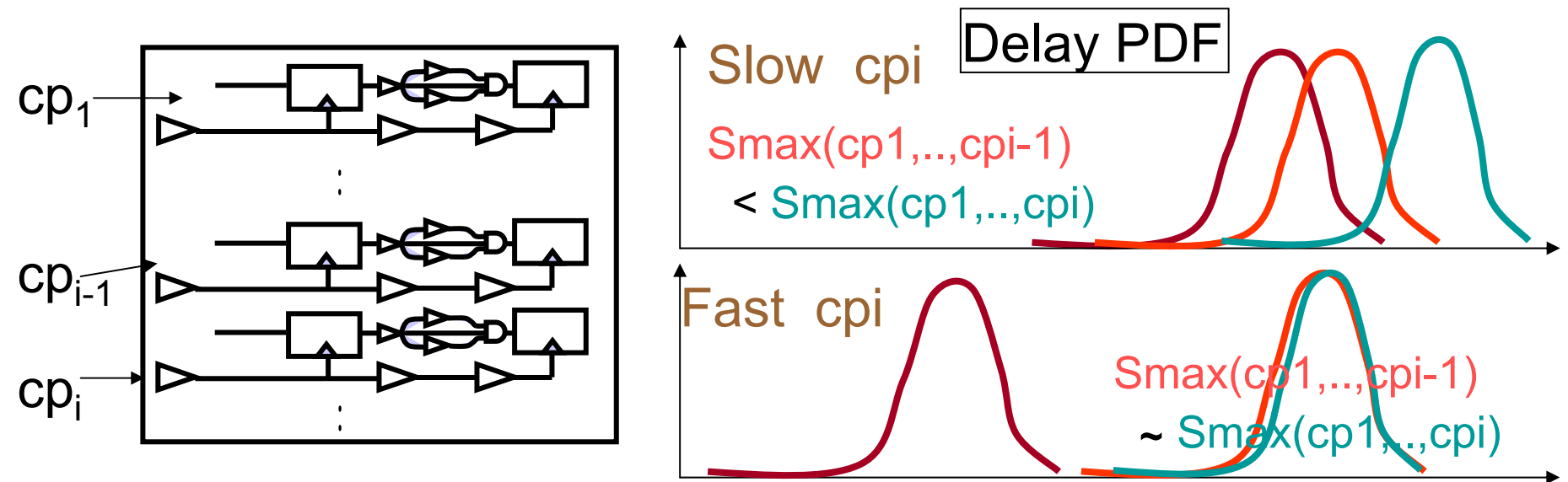


- Step1: Calculate SMAX of WID distributions and let this result be WID element of Statistical MAX distribution.
- Step2: Calculate mean and sigma of the Statistical MAX distribution of path1 and path2 considering D2D correlation.
- Step3: Use moment matching method to calculate D2D element of Statistical MAX distribution from results of Step1,2.

For three or more paths, apply Step1 to 3 iteratively

Proposed Method (2)

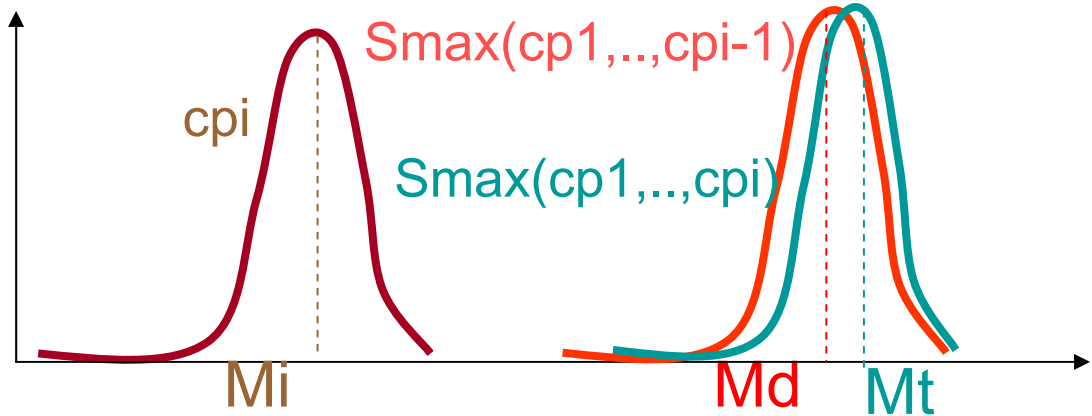
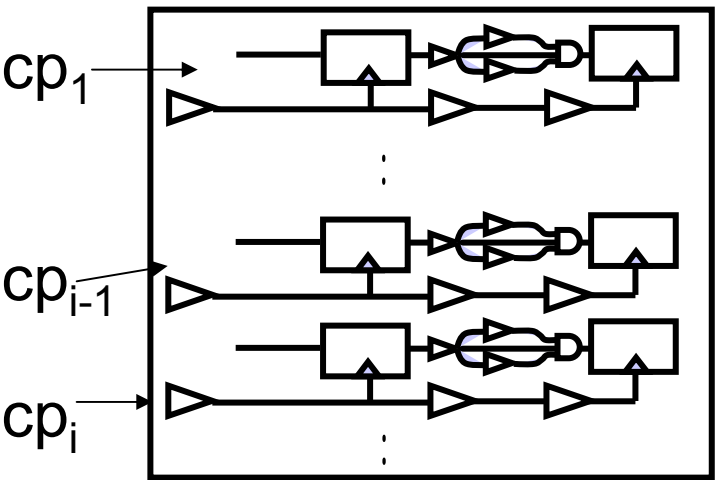
- More accurate than previous methods.
 - Considering the correlation of D2D statistically in Step2.
- The proposed method is time consuming.
 - Mean and sigma calculation of the SMAX considering D2D correlation (Step2) is time-consuming.
- Speed up technique of the proposed method is needed.



Speed up by skipping the SMAX operation (Step1 to 3) for check path having small delay.

Speed up of Proposed Method

Dominance of $cp_i = |Mt - Md| / Md$



- If the dominance of cp_i is small,
 - $S_{\max}(cp_1, \dots, cp_{i-1}) \sim S_{\max}(cp_1, \dots, cp_i)$.
 - cp_i does not affect chip delay.
 - cp_i can be skipped in the SMAX operation.

- Dominance of cp_i can be estimated using only statistics of cp_i and $S_{\max}(cp_1, \dots, cp_{i-1})$ without Mt .
- The estimated dominance enable us to prune check paths effectively.

Experiment

The following four methods are applied to actual chip designs.

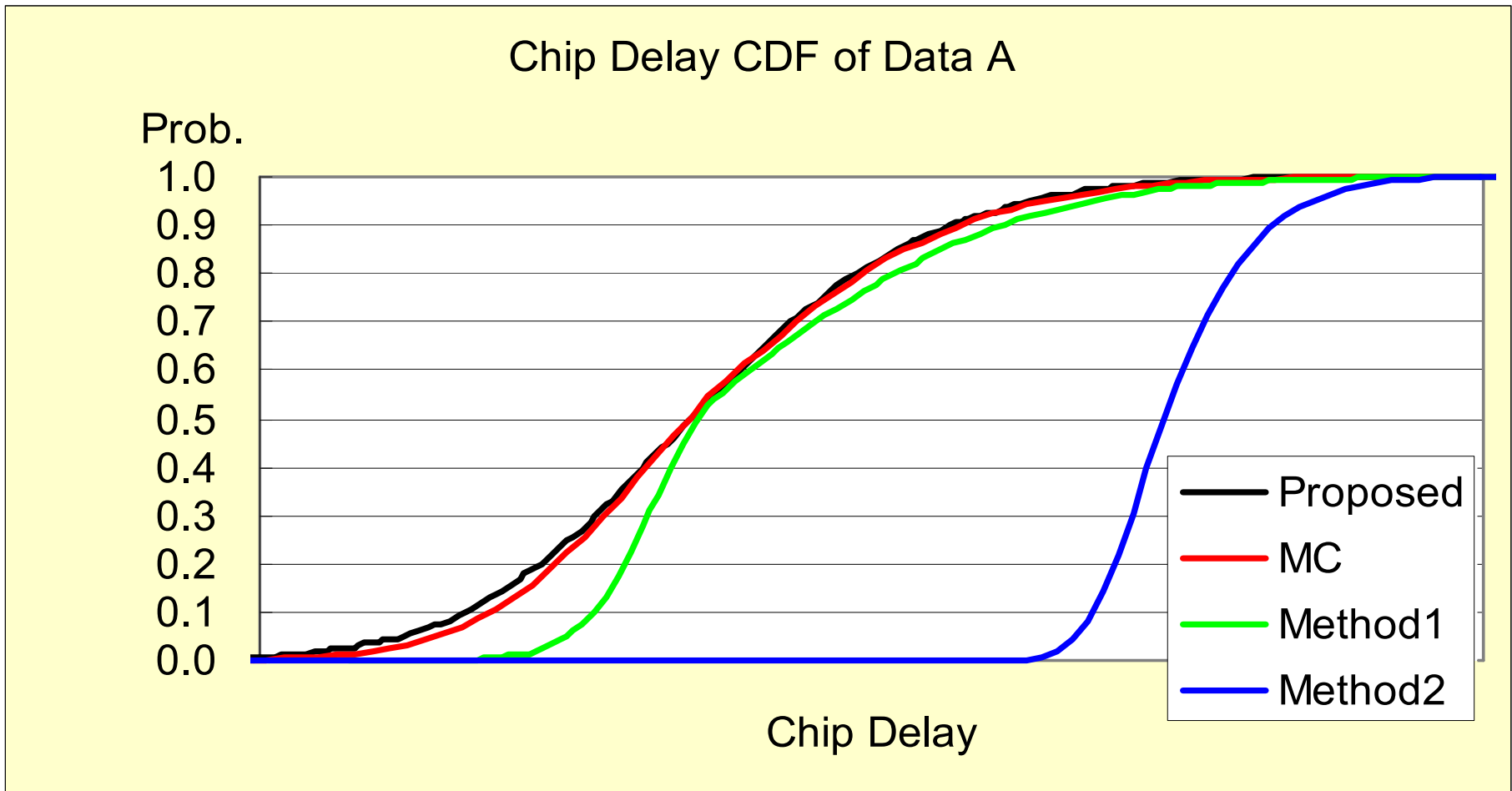
- Proposed Method (Check paths having dominance less than 3×10^{-4} are pruned)
- Practical Monte Carlo Method (10,000 iterations)
- Previous Method 1
- Previous Method 2

The following three Chip designs, 130nm to 65nm, are evaluated

- Data A : 60,116 paths
- Data B : 701 paths
- Data C : 100,000 paths

Accuracy

The proposed method is more accurate than previous methods.



Execution Time

The proposed method is much faster than Monte Carlo because of the path pruning technique. (pruned less than 3×10^{-4})

SunOS 1.1GHz

Chip	Proposed Method	Monte Carlo	<u>Proposed Method</u> Monte Carlo	Rate of dominant check paths
Data A	51m16s	6h26m42s	13.3%	16.3%
Data B	13s	4m29s	4.8%	6.8%
Data C	1m06s	10h40m33s	0.2%	0.2%

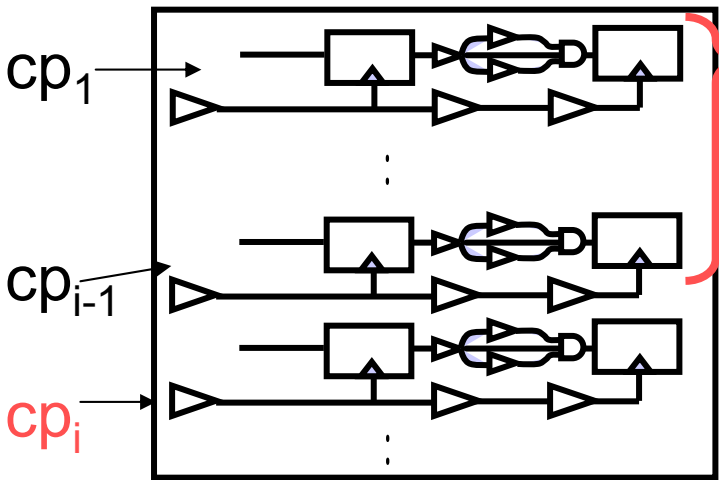
Conclusion

- Provide new method to calculate a full chip delay distribution considering D2D and WID variations.
 - New statistical MAX operation considering non-Gaussian D2D and WID variations.
- Propose a path pruning technique to speed up the method.
 - Path pruning with dominance of path delay distribution.
- Demonstrate the accuracy and efficiency of proposed methods on typical actual designs.
 - More accurate than previous methods.
 - Faster than Monte Carlo method.

Thank you

[Appendix] Dominance Estimation

Dominance of cp_i can be estimated by only WID and D2D parameters of cp_i and $S_{\max}(cp_1, \dots, cp_{i-1})$.



$S_{\max}(cp_1, \dots, cp_{i-1})$

$$M_d - M_i - k * \sigma_d - k * \sqrt{\sigma_i^2 + d^2} > 0$$

$$\Rightarrow \text{Dominance} < A * (3 * \Phi(-k))^{3/4}$$

M_i, σ_i : mean & sigma of WID of cp_i .

ap_i, an_i : D2D coefficients of cp_i .

M_d, σ_d : mean & sigma of WID of $S_{\max}(cp_1, \dots, cp_{i-1})$.

ap_d, an_d : D2D coefficients of $S_{\max}(cp_1, \dots, cp_{i-1})$.

$d = \max(|ap_i - ap_d|, |an_i - an_d|)$.

Φ : standard normal CDF

$k > 0, A > 0$: constant ¹⁸