Low Power Clock Buffer Planning Methodology in F-D Placement for Large Scale Circuit Design

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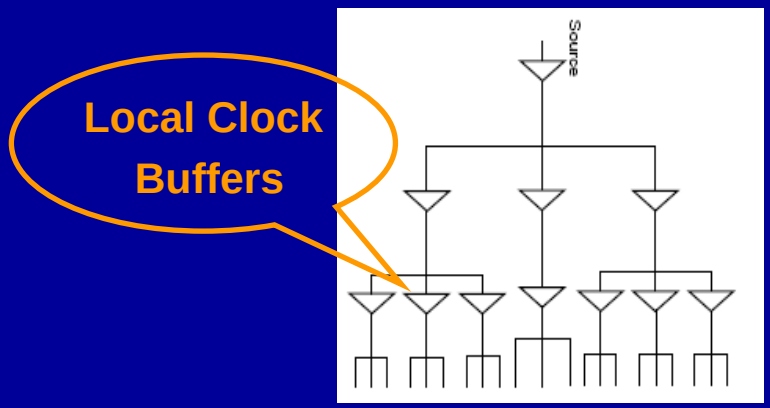
Outline

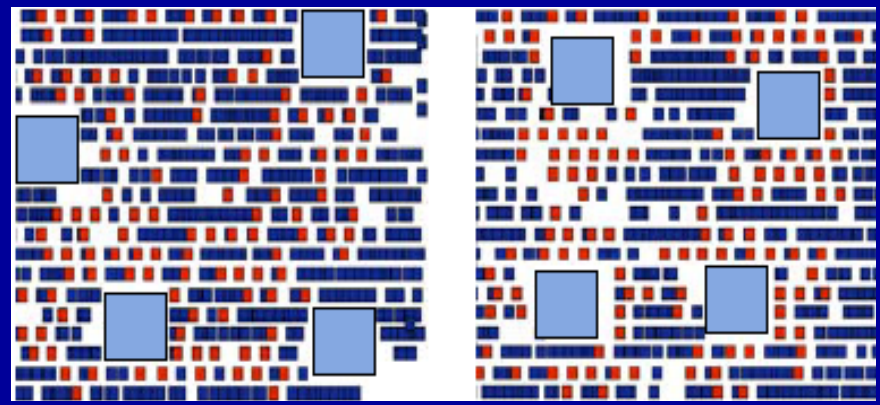
- Research Background
- Low Power Clock Buffer Planning Method
- Experimental Results
- Conclusion

Background

- Clock Buffer Insertion
  - Distributed buffering scheme
  - Huge buffer for better robustness against process variation
- Traditional Clock Buffer insertion Method
  - ECO ---- Clock Buffers placed far from ideal locations
- Clock Buffer Planning Method
  - Explicitly modeling the clock buffers during placement
  - Planning the latch distribution and clock buffer locations
  - Enough space for clock buffers can be reserved



distributed buffering



Traditional Method vs Buffer Planning Method

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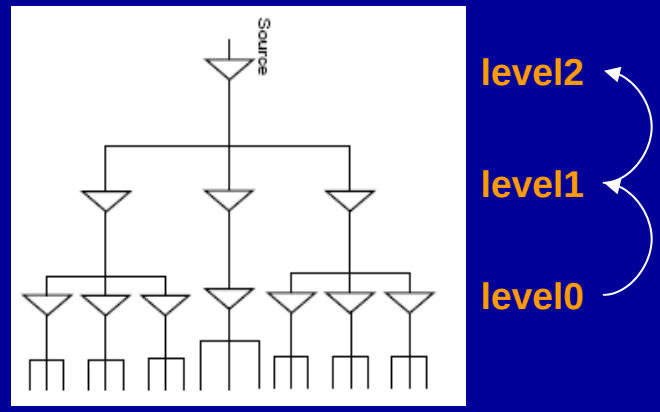
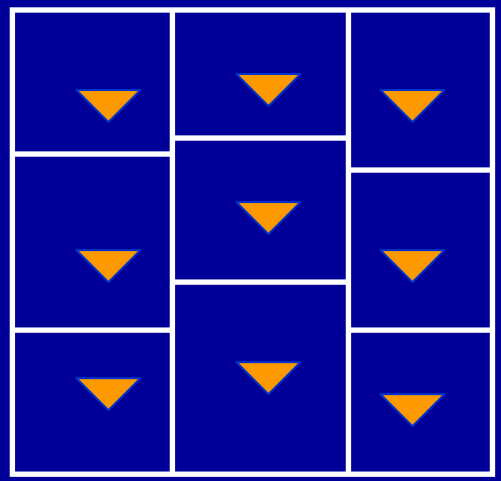
Low Power Clock Buffer Planning (LPBP)

- Virtual Buffer Tree (VBT)
  - Model the latches and clock buffers
- Dynamic Clock Tree Rebuilding (DCTR)
  - For better combination between clock planning and placement
- Latch Clumping
  - Achieve low power design
- Force-Directed Placement
  - Various force for multi-objective optimization

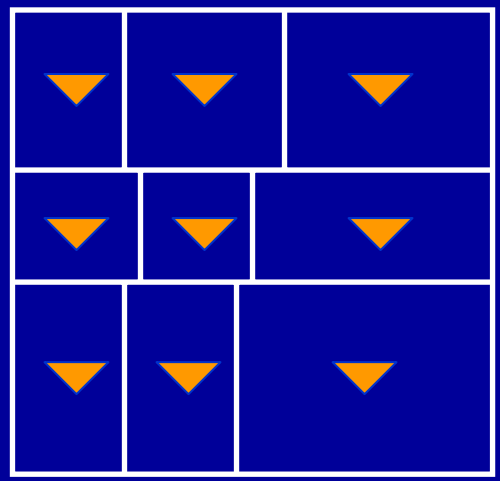
Virtual Buffer Tree

- Buffering scheme
  - Balanced manner
  - Built level by level
  - Group-and-insert process
- Center Force

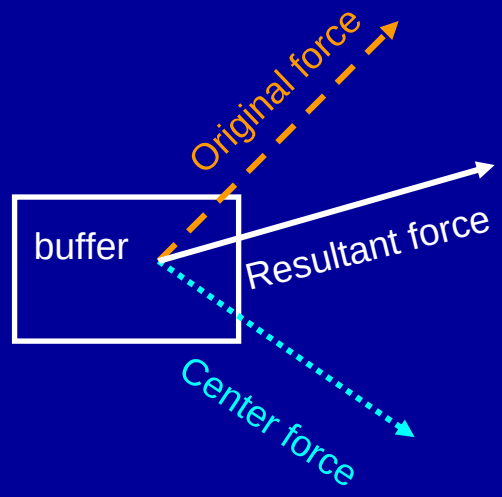




X-first cut grouping

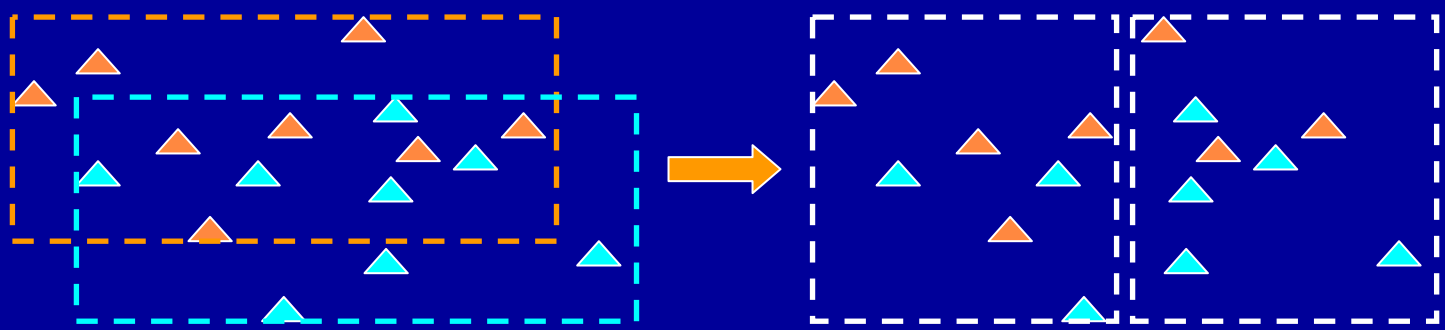


Y-first cut grouping



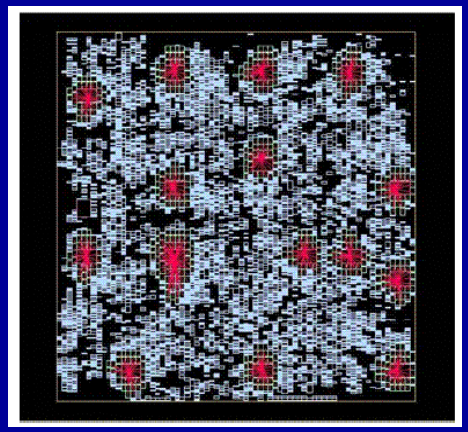
Dynamic Clock Tree Rebuilding

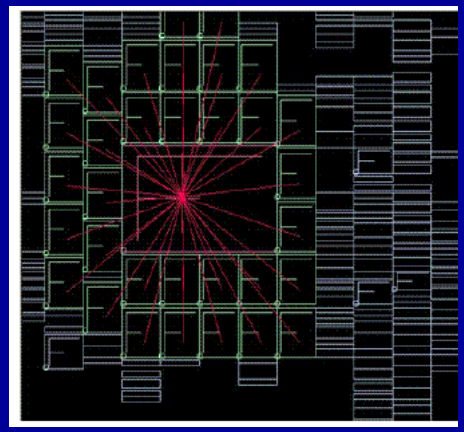
- Reasons for DCTR
  - The instability of the latch position during placement
  - The construction of VBT in placement
    - Too early: the tree topology may be unreasonable
    - Too late: hurt the convergence badly
- What DCTR can?
  - Update the topology of the VBT to reflect the latch placement
  - Preserve better interaction between VBT and placement

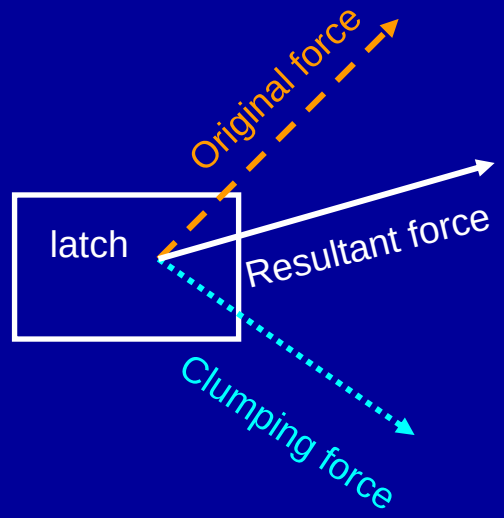


Latch Clumping

- For power optimization
- Implemented by force







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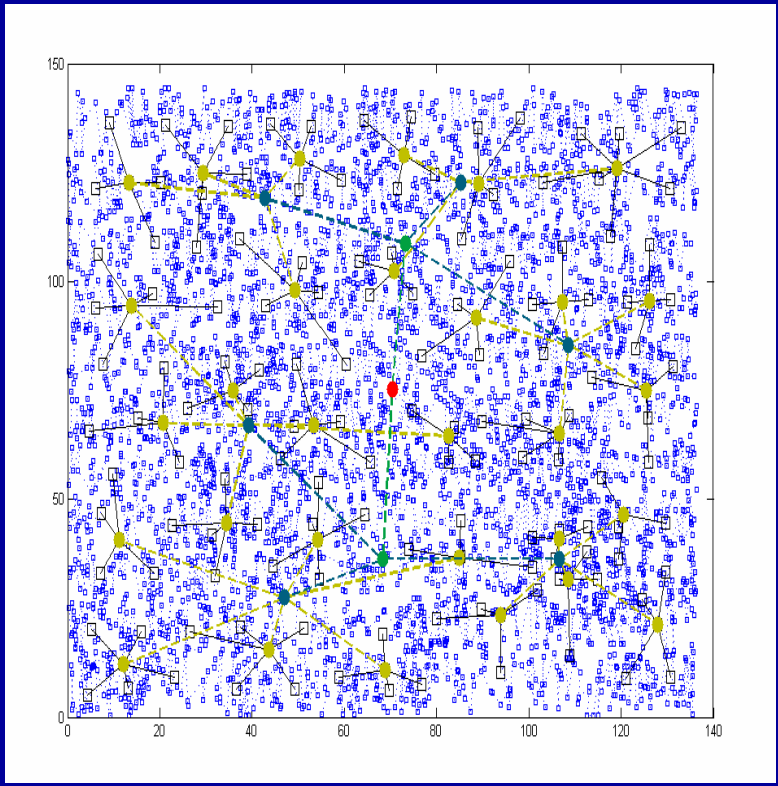
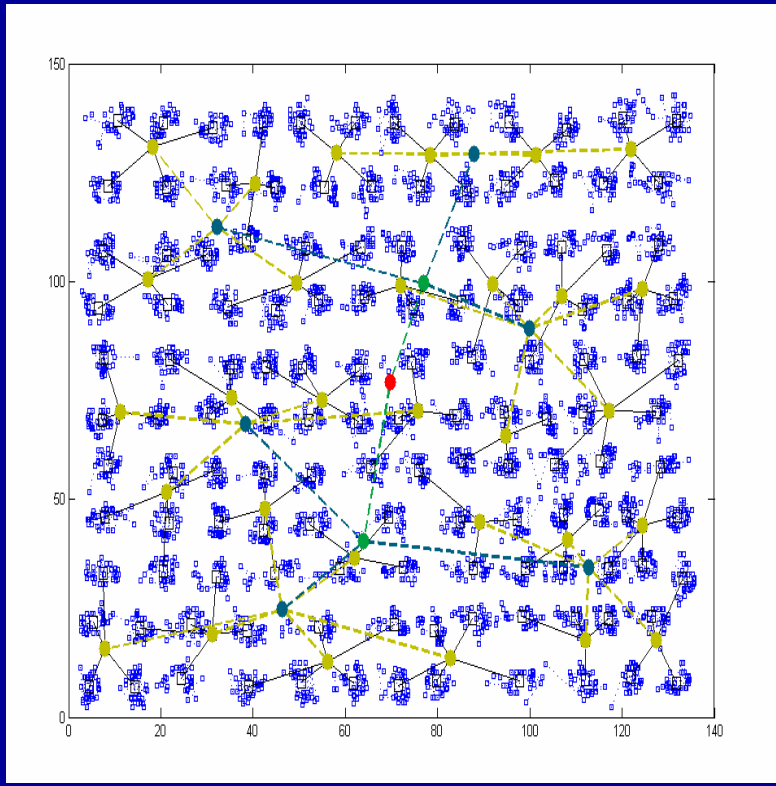
Experimental Results

Design	Scheme	Signal WL	CPU Time	Clock WL (e03)	Power (w)
Ben1	ECO	1.93	22	4.55	1.35
	LPBP	2.03	14	2.92	1.06
Ben2	ECO	4.21	54	6.75	1.96
	LPBP	4.36	52	4.10	1.54
Ben3	ECO	5.98	42	8.16	2.42
	LPBP	6.15	38	5.19	1.90
Ben4	ECO	6.87	67	9.94	2.93
	LPBP	7.08	52	6.46	2.31
Ben5	ECO	11.29	73	10.24	3.07
	LPBP	11.57	56	6.35	2.39
Ben6	ECO	6.29	90	10.07	3.31
	LPBP	6.46	60	6.8	2.63
Ben7	ECO	10.72	91	15.68	4.78
	LPBP	10.98	65	9.48	3.72
Ben8	ECO	11.81	74	17.23	5.38
	LPBP	11.59	57	10.23	4.16
	Avg Impr.	**-3.1%**	**20.0%**	**37.1%**	**21.6%**

Global layout result (ECO *vs* LPBP)



ECO method



LPBP method

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Conclusions

- We propose a low power clock buffer planning method integrated with placement process
- By VBT model, enough space can be reserved at suitable locations for clock buffers to be inserted
- By DCTR technique and Latch Clumping, we can achieve the design with largely improved clock power with the traditional signal wirelength preserved very well

THE END

THANK YOU!