A Fast Two-pass HDL Simulation with On-Demand Dump

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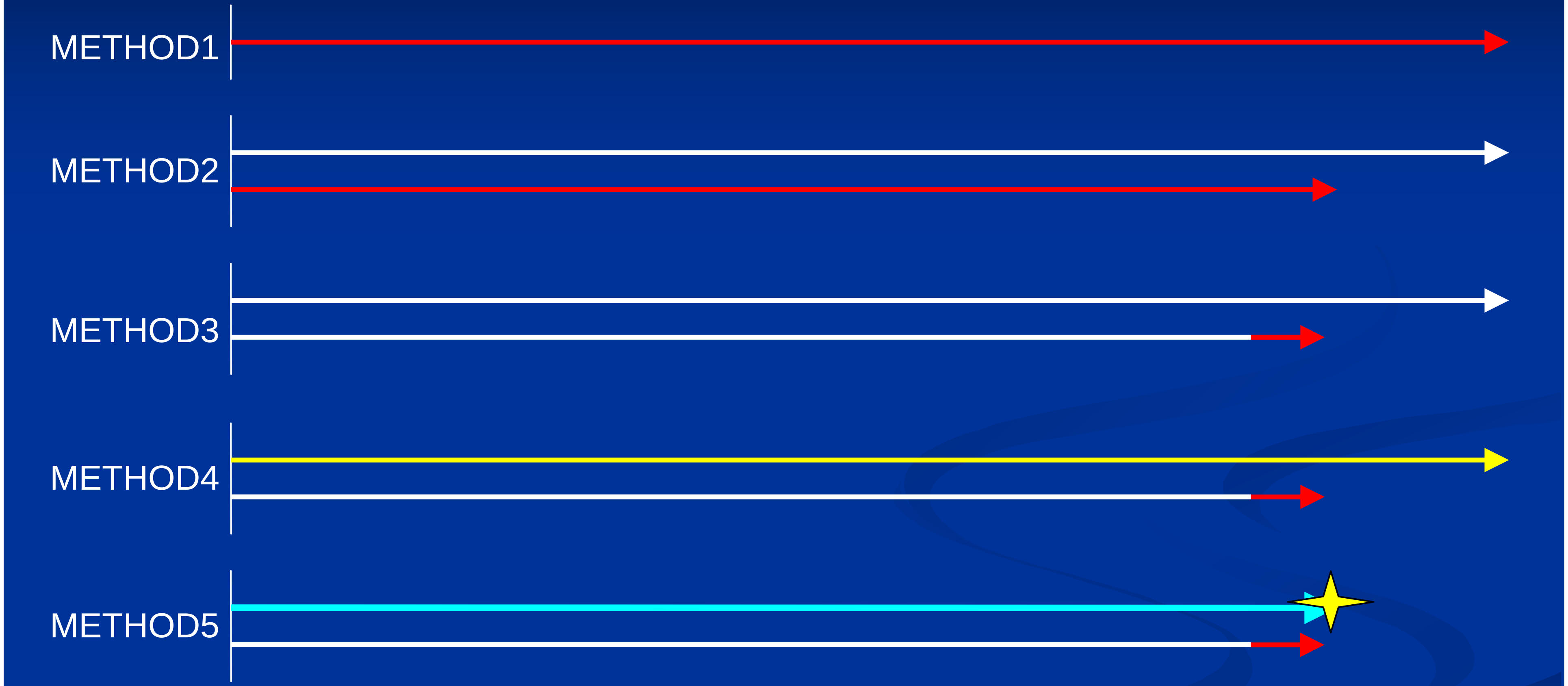
Motivation

- HDL simulation is still the most widely used verification method
  - Pros: 100% visibility
  - Cons: Very slow
- 100% visibility is essential for debugging
  - You cannot debug with no visibility
- But 100% visibility in traditional HDL simulation comes with very high cost
  - Its speed is down significantly
- Therefore, simulation needs to be kept fast even when 100% visibility is needed
  - But, how?

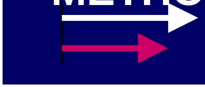
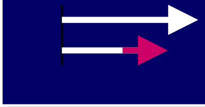
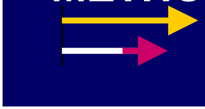
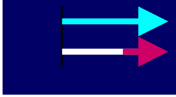
Traditional Simulation/Debugging Methods

→ Simulation run with full dump
→ Simulation run without dump
→ Simulation run with partial dump
→ Simulation run with assertions



Method 1 (always full dump) is not practical for large designs.
Other methods require at least 2nd simulation for enough visibility. However, the 2nd simulation must always start from the simulation time 0.

Traditional Simulation/Debugging Methods

	Pros	Cons	Verdict
METHOD1 	- 100% visibility	- Slowest speed - Highest disk overhead	Not practical
METHOD2 	- 100% visibility	- Repeated simulation - Highest disk overhead	Not practical
METHOD3 	- Lowest disk overhead	- Very low visibility - Repeated simulation, possibly two or more	Not practical
METHOD4 	- Low disk overhead	- Low visibility - Repeated simulation, possibly two or more	Practical, but room for significant improvement
METHOD5 	- Low disk overhead	- Low visibility - Repeated simulation, possibly two or more	Practical, but room for significant improvement

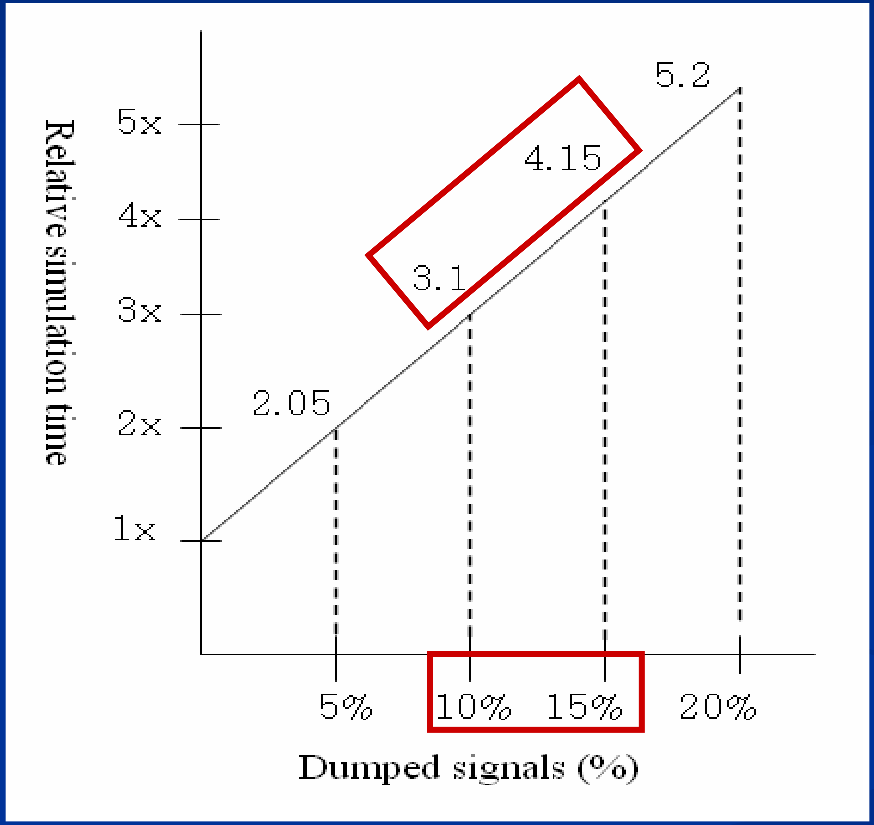
Previous Works

Signal re-construction [Mar98] and visibility enhancement [Hsu06]

- Idea
  - During a simulation run, dump essential signals (all primary inputs and outputs of storage elements) only
  - Interpolate the missing non-essential signals, i.e. outputs of combinational logics, from the essential signals by re-construction
- Problem
  - There are too many essential signals, so the simulation is still slowed down considerably

Previous Works

Signal re-construction [Mar98] and visibility enhancement [Hsu06]



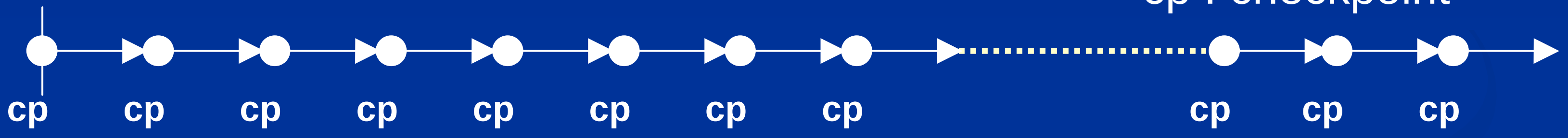
Estimated simulation overhead for essential signals dump for a large design with 22x simulation overhead for full dump

SSi-1: Two-pass Simulation for Debugging Acceleration

Smarter Simulation with SSi-1 is two-pass simulation based on our unique design state checkpoint and re-start

- Checkpoint Simulation (1st Pass)

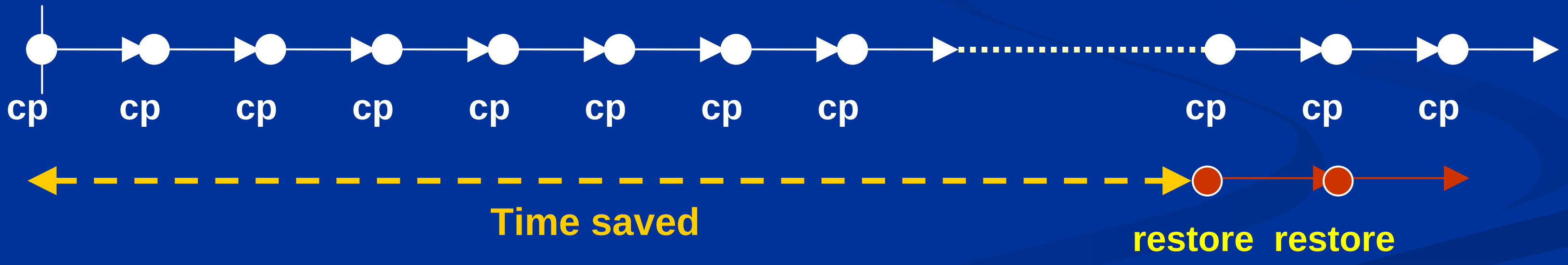
* cp : checkpoint



cp cp cp cp cp cp cp cp cp cp cp

- The simulation time only slightly increases by our unique checkpointing

- Slice Re-Simulation (2nd Pass)



cp cp cp cp cp cp cp cp cp cp cp

Time saved

restore restore

- No need for LONG re-simulation from simulation time 0
- Once any single slice re-simulation is done, the actual debugging process can start

SSi-1: Two-pass Simulation for Debugging Acceleration

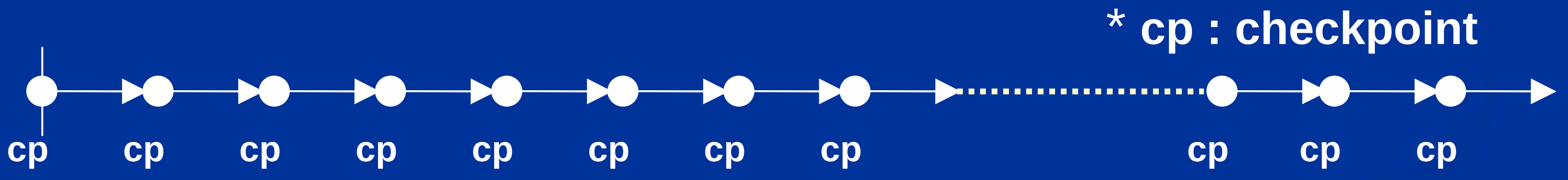
Our unique design state checkpoint and re-start vs. simulation state checkpoint and re-start

	Our checkpoint and re-start	Simulation state checkpoint and re-start
Checkpoint	Design state	Simulation state
One checkpoint file size	Very small, Mega bytes even for very large designs	Very large, Giga bytes for very large designs
# of checkpoint made	Could be made large, e.g. 1,000 or more	Only can be made small
Re-start simulation time	Very short	Still long

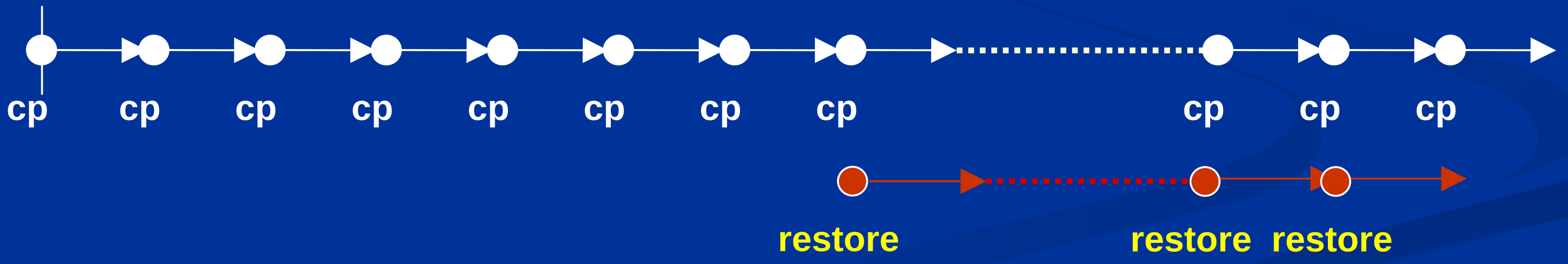
SSi-1: Two-pass Simulation for Debugging Acceleration

If the full signal visibility is needed for very wide simulation time window, perform slice re-simulation in *parallel*

- Checkpoint Simulation (1st Pass)



- Slice Re-Simulation (2nd Pass)



Overall Experimentation Results

- All designs are real SOC designs from industry

Designs	Type	Reduced Debugging Time Ratio (Simulation time reduction) in Single Simulation Run	Reduced Disk Space Ratio (Disk space saving)
SAM	RTL	19.7 x (165.0 hours reduction)	1/14 (48GB saved)
DV	RTL	3.6 x (8.8 hours reduction)	1/20 (32GB saved)
MED	Gate	1.7 x (52.8 hours reduction)	1/5 (145GB saved)
CHA	Gate	3.0 x (265.7 hours reduction)	1/96 (372GB saved)
PRO	RTL	1.9 x (22.9 hours reduction)	1/1.1 (0.3GB saved)
Average		5.98 x (103.0 hours reduction)	1/27 (119GB saved)

Expected Benefits

- **Achieving BOTH full visibility AND highest simulation speed**
  - Fast Checkpoint Simulation (1st Pass)
  - (On-demand based) Slice Re-Simulation (2nd Pass)

- **Completely eliminates repeated, long re-simulation for obtaining signal visibility**
  - Greatly reduces the debugging turn-around time

- **Saving hard disk space for storing dump data**

Conclusions

- Our unique method definitely delivers the higher verification and debugging productivity with accelerating simulation and debugging process

- The benefit from SSi-1 is orthogonal to any other simulation speed-up, e.g. improvements from simulator engine implementation or faster machine

Thank you.
Question?