A Design- for-Diagnosis Technique for Diagnosing Integrated Circuit Faults with Faulty Scan Chains

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Outline

- **Introduction**
- Background
- Proposed Technique
- Experimental Results
- Conclusion
Introduction

- **Design for Diagnosis**
  - Methodology to reduce the complexity of diagnosis
- **Why diagnosis with faulty scan chain**
  - Scan is a widely used design-for-testability technique
    - to improve test quality
  - **Scan chains may occupy 30% silicon area [Kundu 94]**
    - accounts for almost 50% of chip failures [Yang 05]
  - Defects can occur in scan chains
    - Chips with faulty chains fail production diagnosis
  - To improve yield
    - Must identify source of problem
Previous Research

Hardware solutions
- Partner scan chain [Schafer 92]
- Insert XOR gates into scan chain [Edirisooriya 95]
- Modify scan cell design [Narayanan 97][Wu 98]

😊 diagnosis quality can be guaranteed
😊 diagnosis process is time efficient

Software solutions
- Inject-and-Evaluate methods [Stanley 01][Guo 01][Li 05]
- Statistical method [Huang 03]
- IDDQ method [Hirase 99][Song 04]

😊 No area and routing overhead
Helix Scan

● Features
  ◆ Diagnose faulty scan chain precisely and efficiently
  ◆ Diagnose the combinational circuits with faulty scan chains

● Basic Flow
  ◆ Locate the faulty scan cell
  ◆ Transform diagnosis patterns according to faulty position
  ◆ Run load-capture-unload process by “+” and “-” operation
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### Terminology

**Upstream**

- **Cell 5, Cell 4**

**Downstream**

- **Cell 2, Cell 1, Cell 0**

**Even chain**

- **Cell 4, Cell 2, Cell 0**

**Odd chain**

- **Cell 5, Cell 3, Cell 1**

**EU/OU**

- **Cell 4/Cell 5**

**ED/OD**

- **Cell 2, Cell 0/Cell 1**

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**Good scan input**

- Index: 1 0 0 1 1 1 0

**Stuck -At 0 (SA0)**

- Index: 1 0 0 0 0 0 0

**Stuck -At 1 (SA1)**

- Index: 1 0 1 1 1 1 1
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  – Architecture of Helix Scan
  – Helix Scan chain fault diagnosis
  – Combinational circuit diagnosis with faulty Helix Scan chain
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Helix Scan Chain Fault Diagnosis

1. Loading all-0-pattern if SA1
2. Conducting “+” operation
3. Unloading and Observing
Combinational Circuit Diagnosis with Faulty Helix Scan Chain

- Objective Pattern: 0011, 1100

Clock:    1  2  3  4
Operation: +  +  -  +
Odd Chain: 1  0  1  0
EU:       x  x  x  x
ED:       x  x  0  0
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Experiment

- Evaluate the latency of HS cell in Function mode and Scan mode in 0.13um technology.
- Experiments are performed on ISCAS'89 to evaluate the area overhead.
- Experiments are performed on ISCAS'89 to evaluate the routing overhead.
latency of HS cell

- The HS cell is 20ps later than the DFF
  - the falling time of HS cell is about 60ps latter than traditional DFF
  - The rising time of HS cell is about 20ps later than traditional DFF

(a)  
(b)
Comparison of Routing Overhead

This Work

[16]
# Comparison Diagnosis Resolution with Software Solutions

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</table>

(Average/Worst)
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Conclusion

- **Helix Scan**
  - Proposed a novel scan architecture
  - Precisely diagnose the fault in scan chain
  - Diagnose the combinational circuit with faulty scan chains
  - Compatible with conventional scan-based design
Thank You !!!