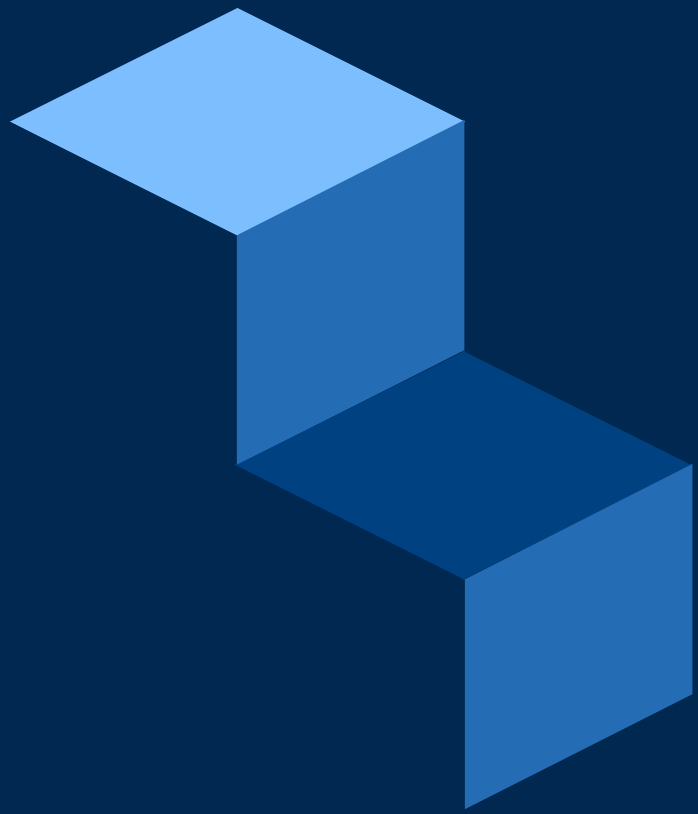
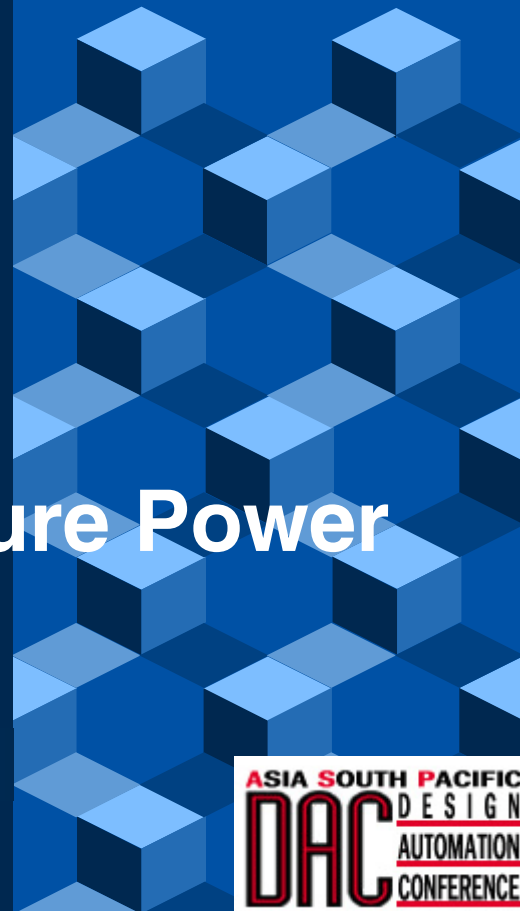


On Reducing Both Shift and Capture Power for Scan-Based Testing

Jia LI, Qiang XU, Yu HU, Xiaowei LI



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Outline

1. Introduction
2. Backgrounds
3. Proposed *LSC-filling* algorithm
4. Experimental Results
5. Conclusion

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Problems of High Test Power

Related to shift power

- **elevated average power consumption**
  - adds to the thermal load that must be transported away from the circuit under test (CUT).
  - can cause structural damage to the silicon, bonding wires, or the package.

Related to capture power

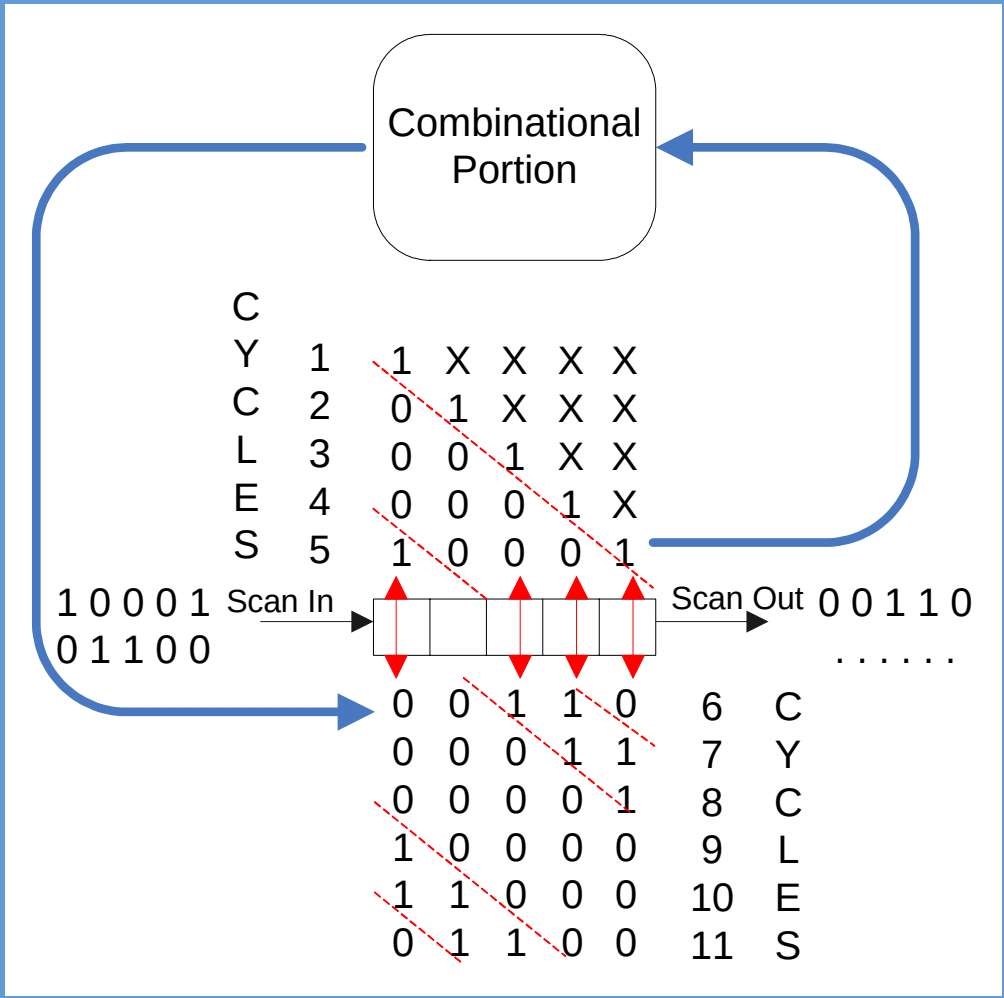
- **excessive peak power dissipation**
  - is likely to cause a large voltage drop
    —erroneous data transfer in the test mode only (invalidate the testing process and lead to yield loss).

Differences between shift and capture power

- **Source:**
  - Shift power: logic value differences between adjacent bits in test vectors
  - Capture power: logic value differences in each scan cell before and after the capture cycle
- **Optimization goal:**
  - Shift power: reduce it as much as possible
  - Capture power: keep it under a safe peak power limit
- **Basic idea of the proposed *LSC-filling*:**
  - Use as few as possible X-bits to keep the capture power under the peak power limit —*LC-filling*
  - Use the remaining X-bits to reduce the shift power —*LS-filling*

Outline

Shift and capture power consumption during scan tests



Prior works on low power testing

- **DFT (design-for-testability)-based solutions (high efficiency and overhead)**
  - Scan chain manipulation (shift)
  - Circuit modification (shift, capture)
- **Software-based solutions (no hardware overhead, limited efficiency)**
  - Low-power ATPG (shift, capture)
  - X-filling (shift, capture)

Low power X-filling problem

- **Test cubes may contain as much as 95-98% X bits (can be filled freely without affecting the fault coverage)**
- **X-filling for shift power reduction**
  - Reduce transitions in test vectors
- **X-filling for capture power reduction**
  - Reduce Hamming distances between the test stimuli and responses in every scan cell
- **Different optimizing approach, limited X bits —tradeoff solution needed**

Outline

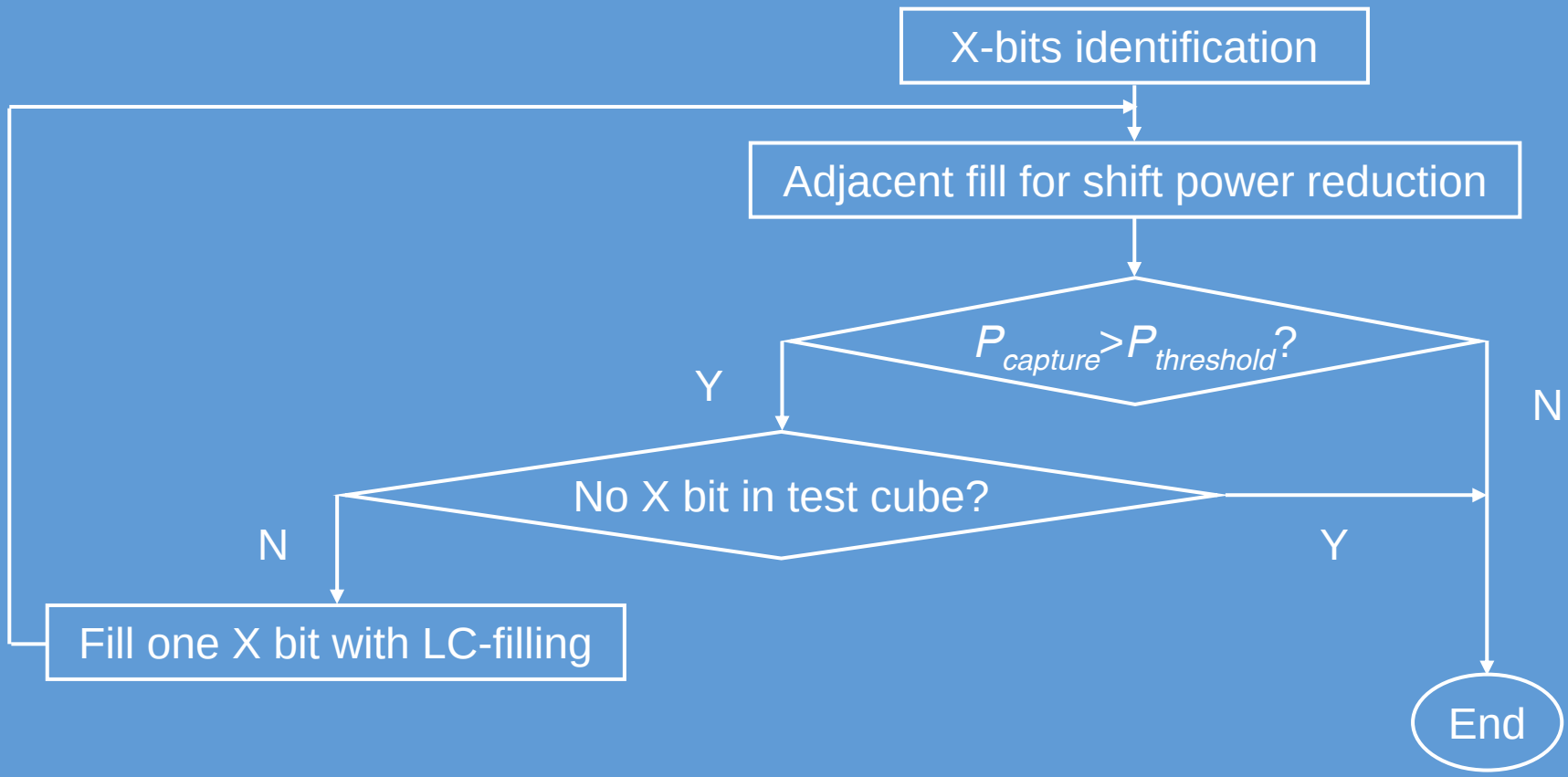
LC-filling for capture power reduction

- Impact of filling one X bit X_j of the i^{th} test stimuli vector with logic value v('1' / '0') on transitions of scan cells:

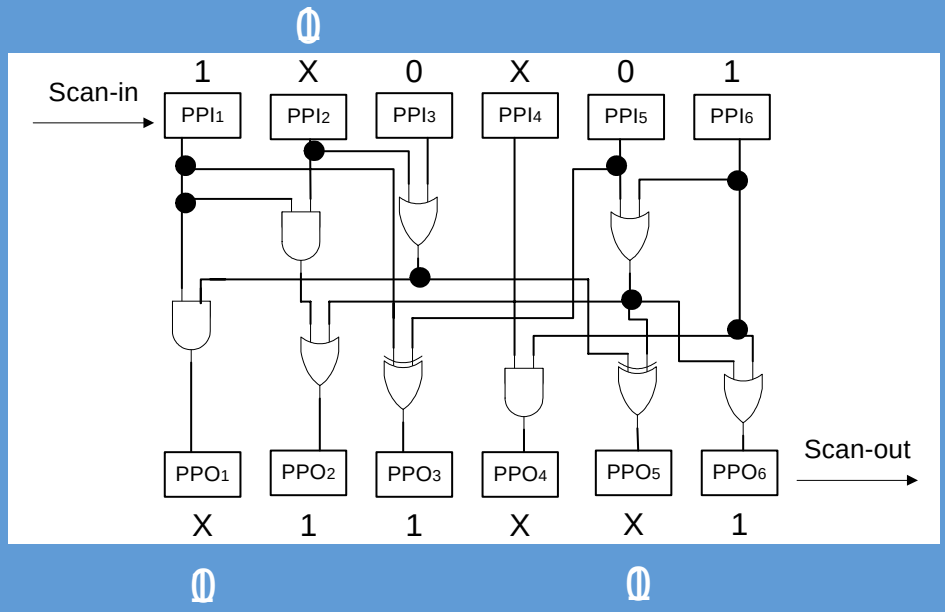
$$T_{capture}(i, j, v) = \sum_{k \in f(v)} R_{i,k} \oplus S_{i,k} - \sum_{k \in f(v)} \overline{R_{i,k} \oplus S_{i,k}}$$

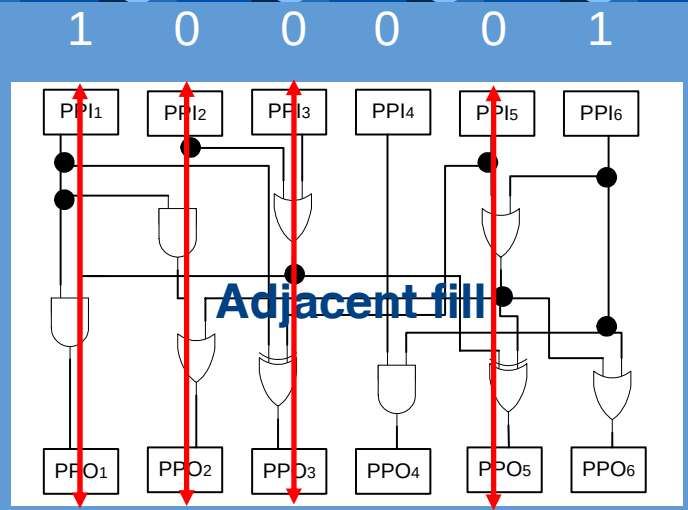
- $T_{capture}\downarrow$, capture transitions in scan cells $\downarrow$
- Therefore, X bits with lower $T_{capture}$ are filled earlier to reduce capture power faster.

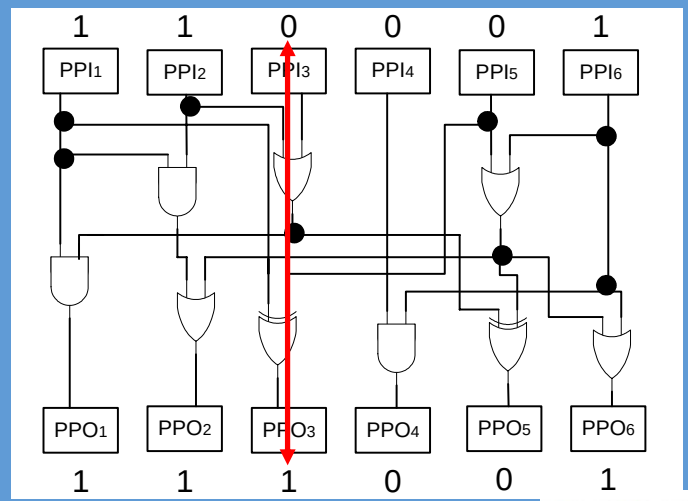
LSC-filling for shift and capture power reduction



An example







$T_{capture}(i,2,1) = -3;$
$T_{capture}(i,2,0) = 3;$
$T_{capture}(i,4,1) = 0;$
$T_{capture}(i,4,0) = -1$

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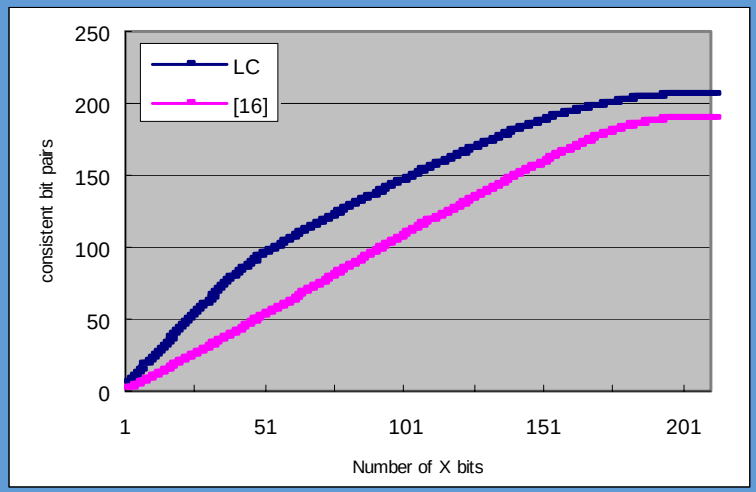
Experimental results for *LC-filling*

Circuits	# of Scan Cells	# of Patterns	LCP[16]	LC	reduction
s1196	18	139	1	1	0
s1238	18	152	1	1	0
s5378	179	111	26	26	0
s9234	211	159	26	19	26.92%
s13207	638	236	37	25	32.43%
s15850	534	126	31	22	29.03%
s38417	1636	99	185	136	26.49%
s38584	1426	136	152	130	14.47%

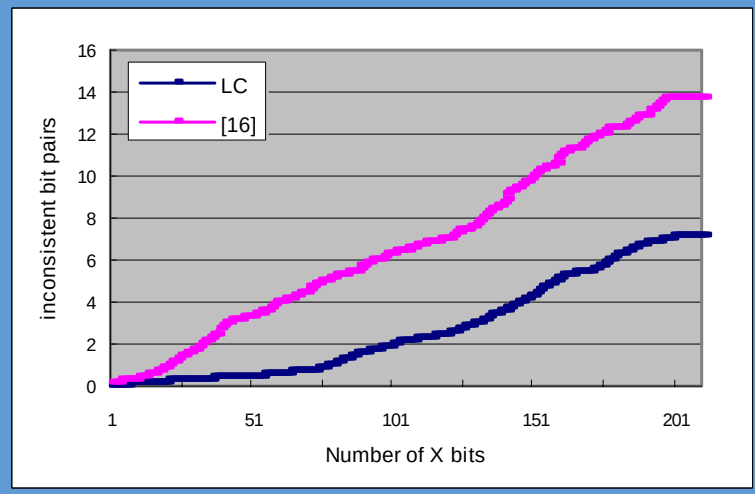
[16] X. Wen, et al., "Low-capture-power test generation for scan-based at-speed testing," *Proc. IEEE International Test Conference (ITC)*, 2005, pp. 1019-1028.

Growth of consistent and inconsistent bit pairs

Consistent bit pairs



Inconsistent bit pairs



***LC-filling* can reduce capture power more faster**

Experimental results for LSC-filling

Circuits	Ori.Vio.	Adjacent fill				LC-filling				LSC-filling			
		Ave. Shift	Ave. Cap.	Max. Cap.	# of Vio.	Ave. Shift	Ave. Cap.	Max. Cap.	# of Vio.	Ave. Shift	Ave. Cap.	Max. Cap.	# of Vio.
s1196	2	**69**	9	14	132	134	**1**	**8**	**2**	117	3	**8**	**2**
s1238	4	**70**	9	14	147	135	**1**	**7**	**4**	118	3	**7**	**4**
s5378	10	**5976**	87	119	111	11337	**26**	**93**	**15**	9761	51	**93**	**15**
s9234	0	**13537**	75	104	126	19660	**19**	**59**	**0**	14924	60	62	**0**
s13207	0	92235	214	289	178	147895	**25**	**184**	**0**	**84035**	168	190	**0**
s15850	0	63975	135	236	25	69734	**22**	**127**	**0**	**58481**	125	159	**0**
s38417	0	**391913**	334	541	7	677308	**136**	**350**	**0**	391989	330	489	**0**
s38584	0	**489613**	375	700	7	795848	**130**	**487**	**1**	492169	365	**487**	**1**

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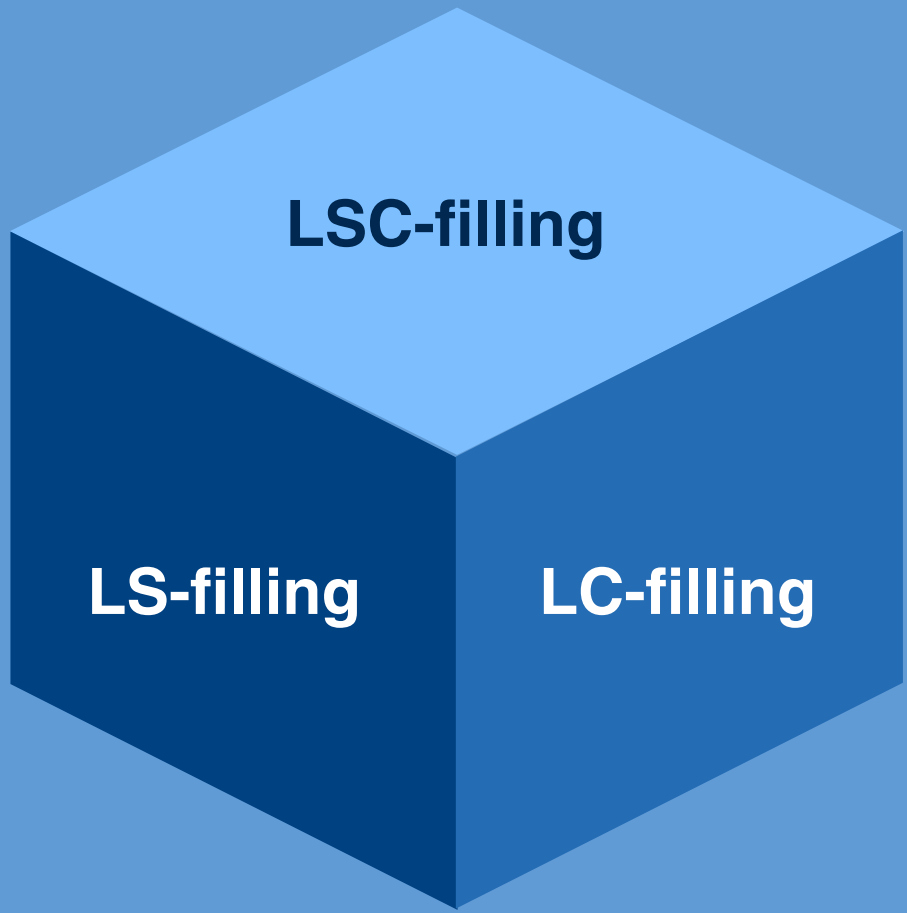
Conclusion

Can both guarantee peak power safety and achieve lower shift power

Adjacent filling is utilized in this paper



can reduce capture power more efficiently and faster

Thank you!