Robust Test Generation for Power Supply Noise induced Path Delay Faults

Xiang Fu[1,2], Huawei Li[1], Yu Hu[1], Xiaowei Li[1]

1 Key Laboratory of Computer System and Architecture,

Institute of Computing Technology, Chinese Academy of Sciences

2 Graduate School of Chinese Academy of Sciences

Outline

- Introduction
- Fault Model
- ATPG
- Experimental Results
- Conclusion

ΔI

Introduction

Two Parts of PSN

Our Main Concern

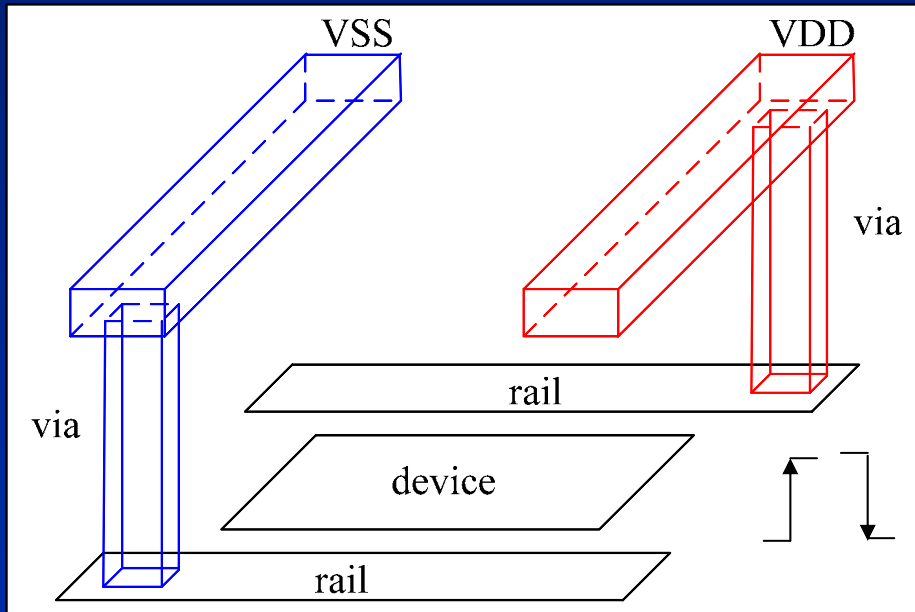
Inductive ΔI noise: $L*di/dt$

Power net resistance induced voltage variation

Parasitic inductance and change of current

Current though resistive power and ground stripes

Impact of PSN: performance degradation



Power Supply IR Drop

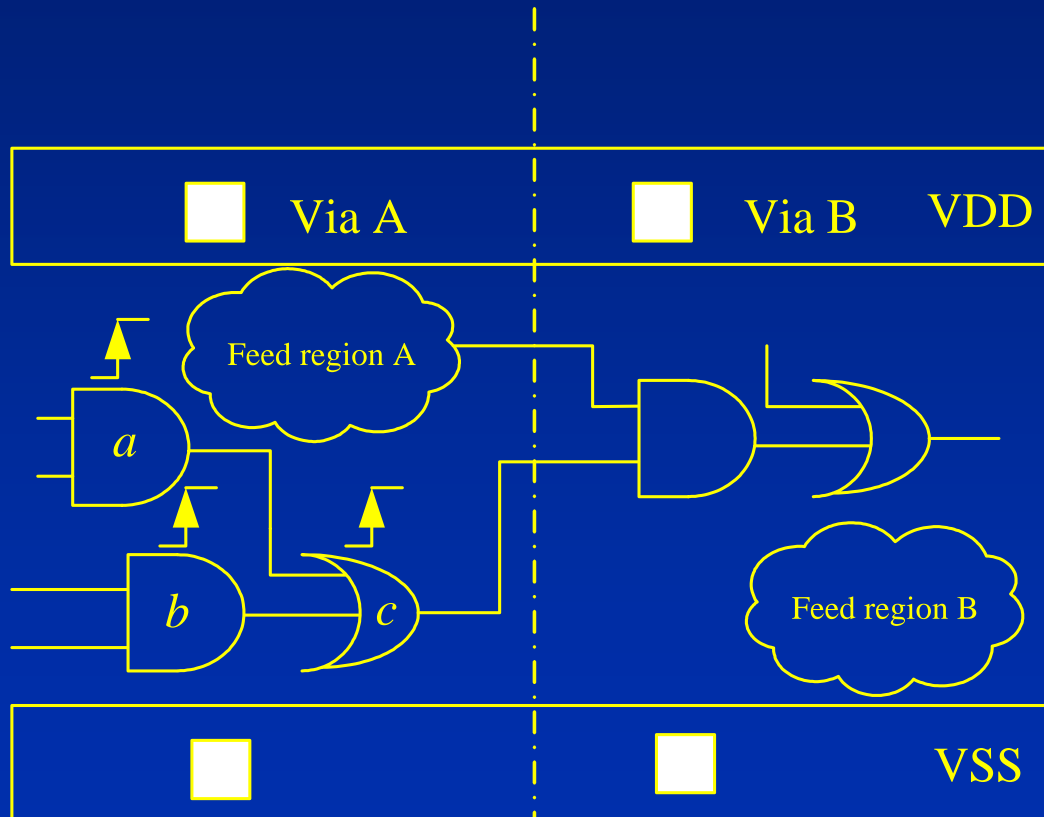
Ground Bounce

Cause voltage variation

Increase the delay

Characteristics of PSN

1. PSN is a local phenomenon.
2. PSN is highly pattern dependent.



Goal of ATPG Considering PSN

Designers' Perspective

- Design Phase: noise margin
- Test Phase: chips should be fully tested

Possible Solution

- Fault model that takes PSN into account

Goal

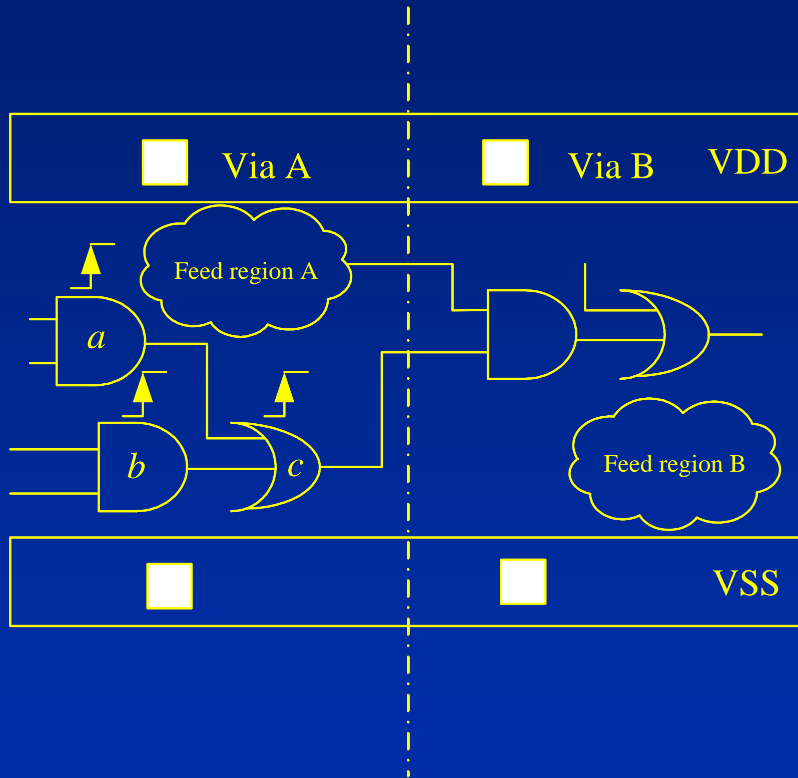
- Generate patterns that could maximize PSN induced delay

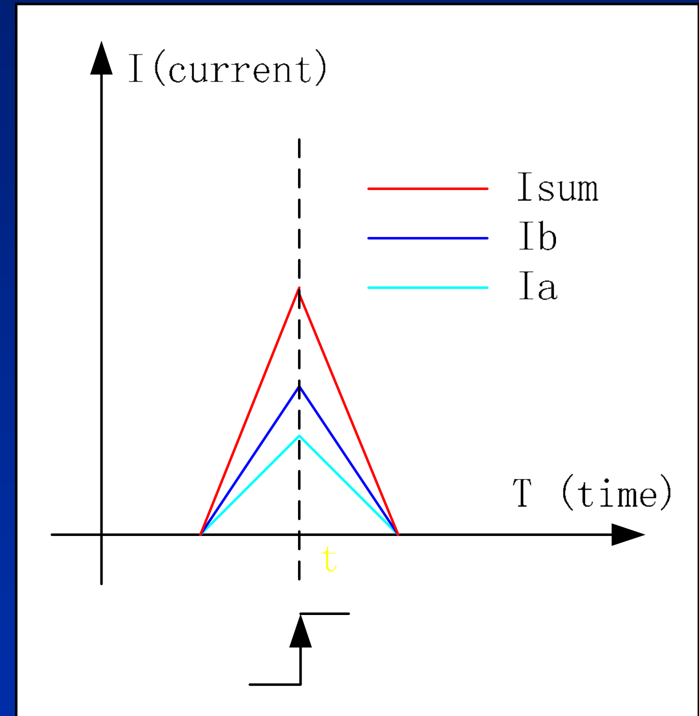
Outline

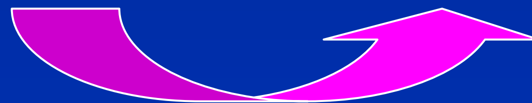
- Introduction
- Fault Model : PSNPDF
- ATPG
- Experimental Results
- Conclusion

PSN-induced path delay Fault (PSNPDF)

PSNPDF: Timing window is incorporated







PSN-induced path delay Fault (PSNPDF)

PSNPDF: Timing window is incorporated

PSNPDF: victim/aggressor model $F(LP, sp\text{-}a)$

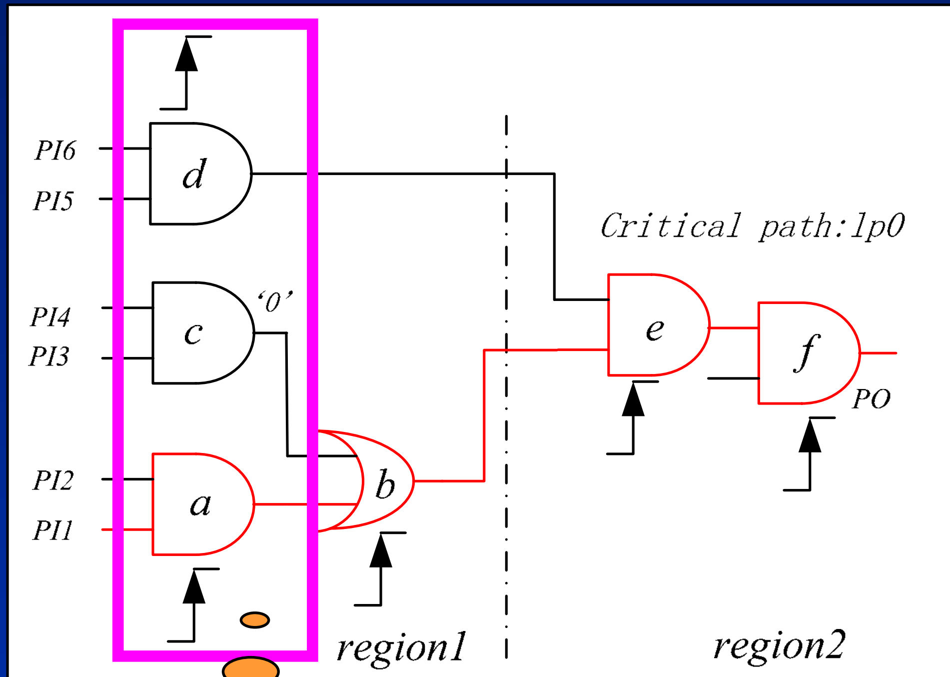
Victim: LP → ***Critical path of CUT, robustly testable***

- ***Gate v: an on-path gate of LP***

Aggressor: $sp\text{-}a$ → ***A sub-path ends at Gate a, also denoted as $sp(a, v)$***

- ***Gate a: an off-path gate in the same timing window and feed region of Gate v***

Example of Aggressor List Generation



Overlapped Timing Window

Victim: critical path *lp0*

Aggressor:

- *sp-d: sp(d, a)*
- *sp-c: sp(c, a)*

F(lp0, sp-d)

lp0 **should be robustly tested.**

Outline

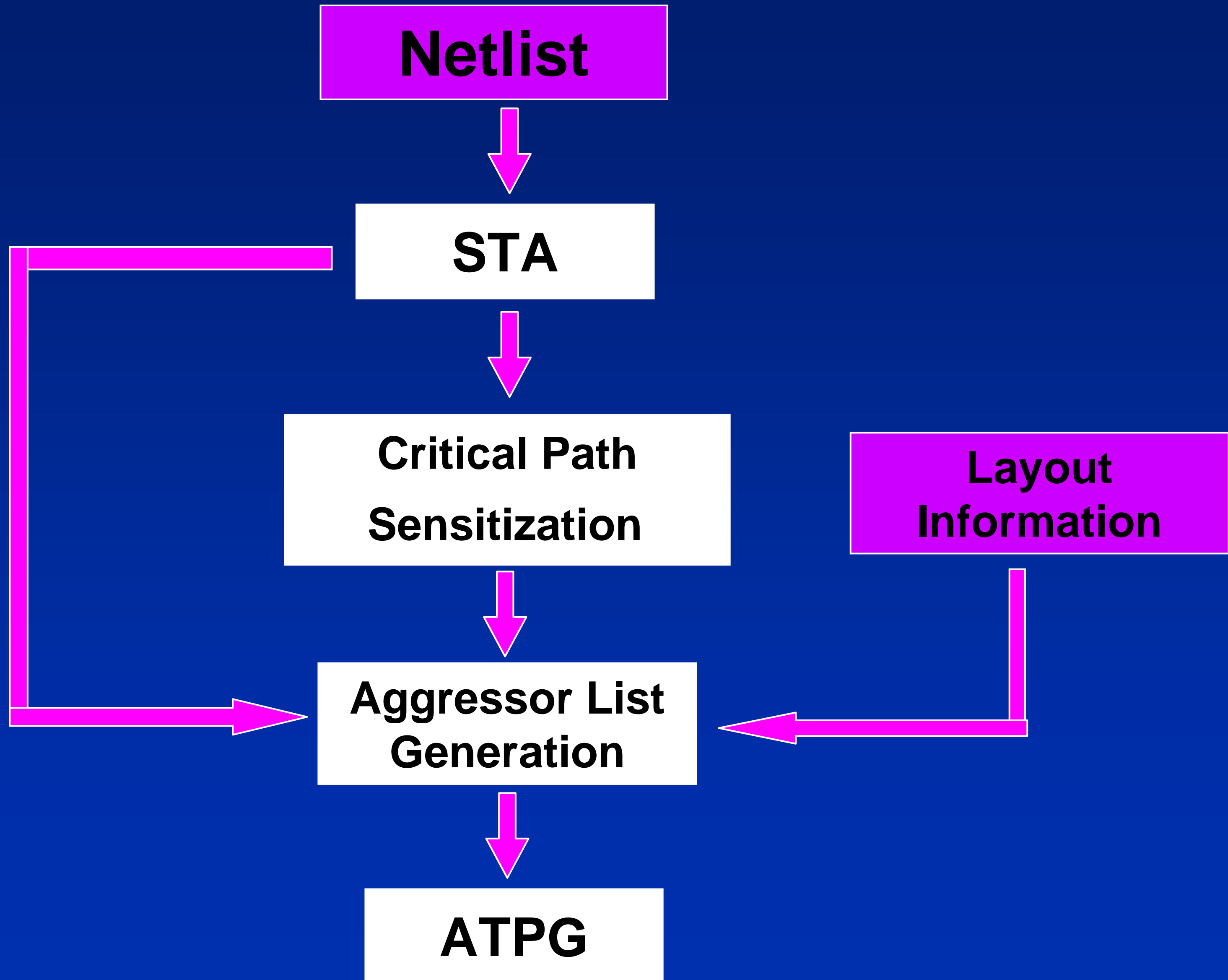
- Introduction
- Fault Model
- ATPG
- Experimental Results
- Conclusion

Path Sensitization

Two parts of ***F(LP, sp-a)***

- ***LP*****:** Robust path sensitization criterion
- Sub path *sp-a*: relaxed to functional sensitization criterion

ATPG Flow



Outline

- Introduction
- Fault Model
- ATPG
- Experimental Results
- Conclusion

Experimental Results

- Applied to ISCAS'89 circuits
- Fanout weighted delay model
- Feed region: devices selected randomly

Circuit Names	# of target faults	Testable Faults			Fault Efficiency (%)	Fault coverage (%)	CPU time (secs)
		#TFs	#UTF	#AFs			
s208	79	69	10	0	100.00	87.34	0.187
s386	454	219	235	0	100.00	48.24	0.296
s526	22	20	2	0	100.00	90.91	0.171
s820	187	101	82	4	97.86	54.01	0.281
s953	156	132	24	0	100.00	84.62	0.343
s1196	127	55	72	0	100.00	43.31	0.281
s1488	68	34	34	0	100.00	50.00	0.265
s1494	62	31	31	0	100.00	50.00	0.265
s5378	3103	2965	123	6	99.80	95.55	5.546

Outline

- Introduction
- Fault Model
- ATPG
- Experimental Results
- Conclusion

Conclusion

- PSNPDF is introduced
  - *A fault model considering PSN-induced delay*
- High coverage
  - *Almost 100%*
- Acceptable CPU run time
  - *In a few seconds*