Optimal Allocation and Placement of Thermal Sensors for Reconfigurable Systems and Its Practical Extension

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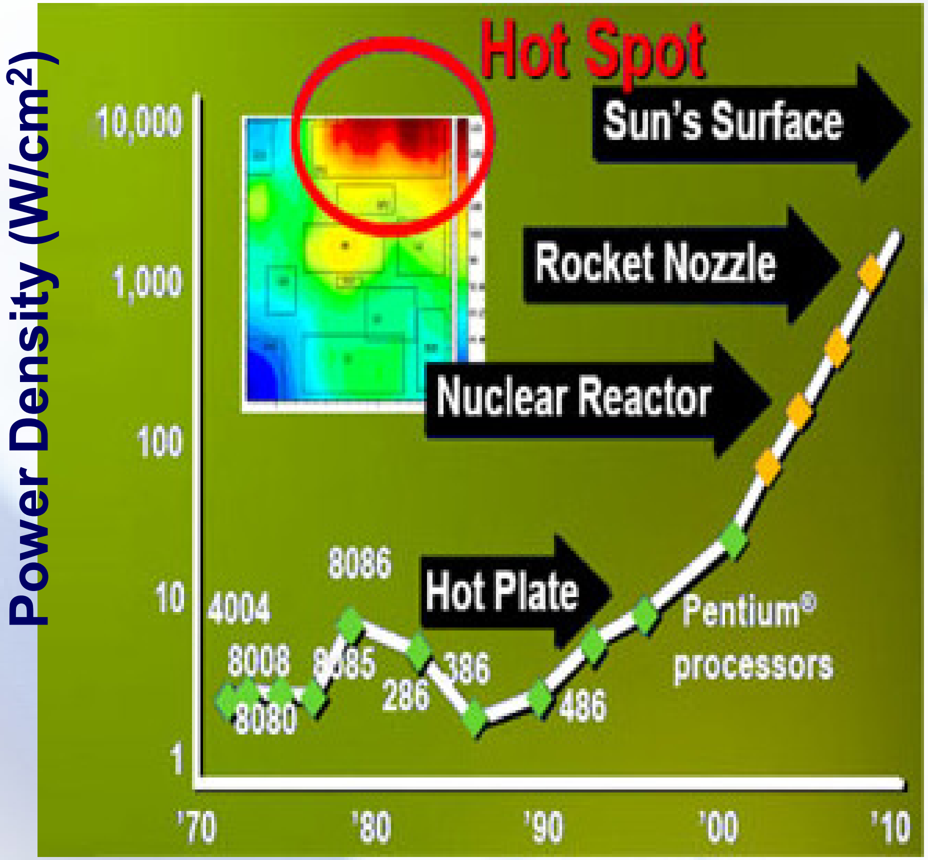
Outline

1. Introduction
2. Thermal Sensor Allocation and Placement
3. Experimental Result
4. Conclusion

Hotspot

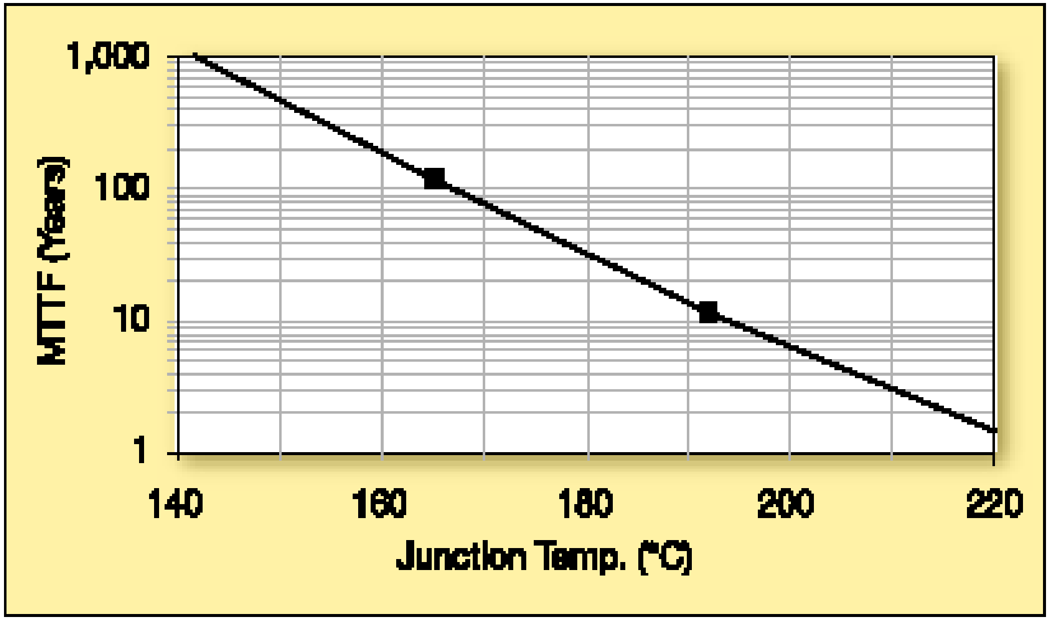


Source: Intel

- Aggressive technology scaling leads to higher power density
- higher power density
  → higher die temperature
- Hotspots :
  - Regions on chip that dissipate excessive heat
  - Uneven activity distribution
  - Slow lateral heat propagation in silicon

Effects of Die Temperature

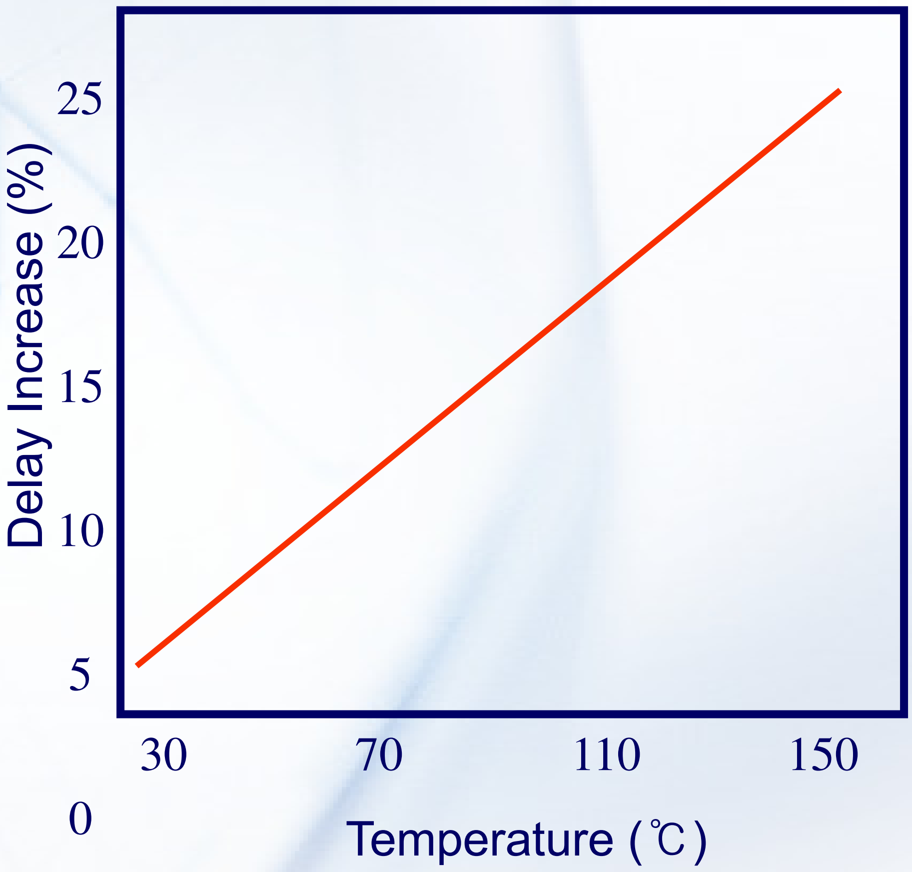
- **Lifetime**
  - Exponential degradation



MTTF Vs Junction Temperature

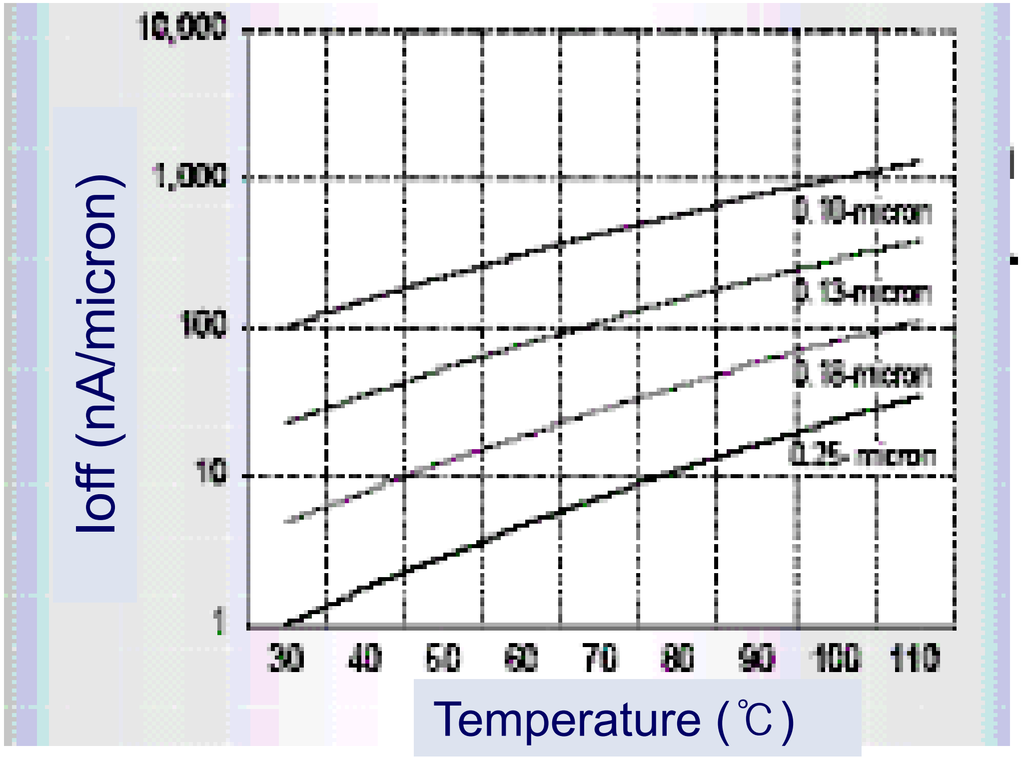
Effects of Die Temperature

- **Lifetime**
  - Exponential degradation
- **Circuit delay**
  - Linear increase



Effects of Die Temperature

- **Lifetime**
  - Exponential degradation
- **Circuit delay**
  - Linear increase
- **Static power**
  - Exponential increase



Temperature vs. Leakage

(Source: V. De, ISLPED 1999)

Thermal Monitoring

- **Detection of hotspots**
  - Power dissipation estimates not sufficient for thermal characterization
  - Correlates with power density and physical interaction
- **Runtime thermal management**
  - Microprocessors
  - Limited versions in FPGAs

Thermal sensor(1)

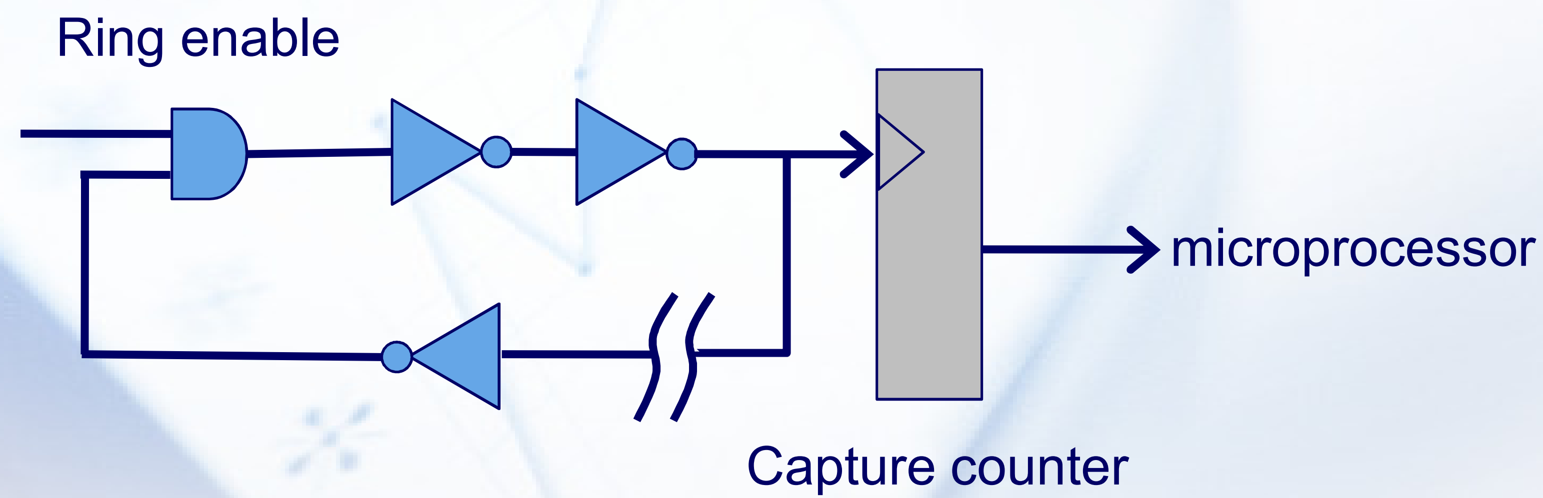
- **FPGAs are popular programmable logic devices**
- **Commercial FPGAs are now available at 65nm**
  - High logic density → High power density → High temperature
  - Maximum die temperature is 80°C w/o performance degradation
  - Over 125°C with excessively parallel execution
- **Pre-fabrication thermal sensor**
  - Single on-chip sensor is a poor representation
  - Multiple sensors are inefficient

  → Ring-oscillator based thermal sensor for FPGA

Thermal sensor(2)

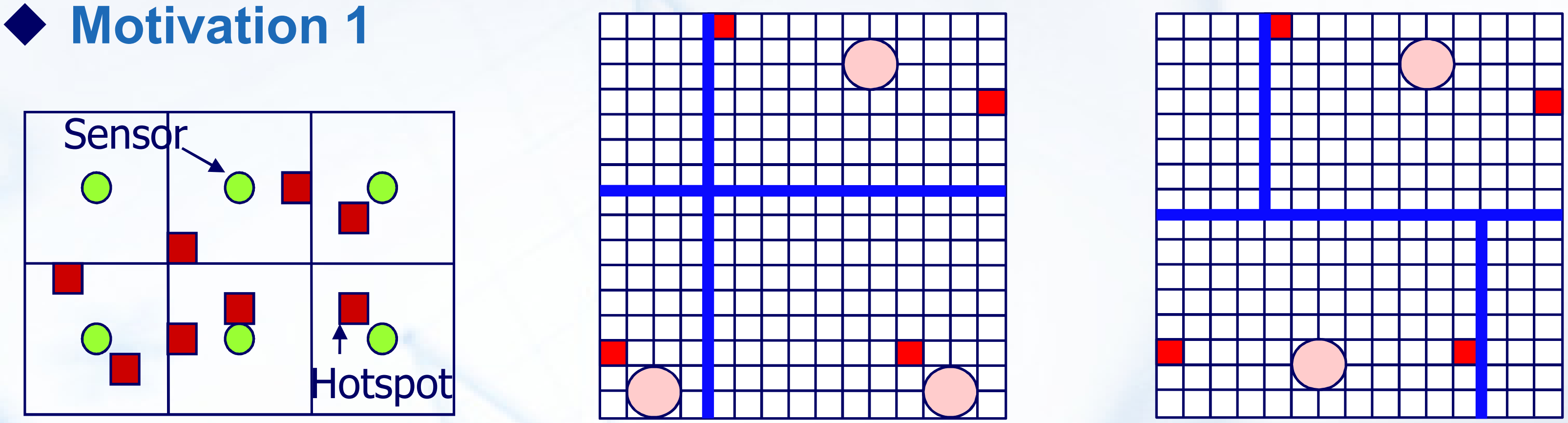
◆ Ring oscillator based thermal sensor

- Relation between transistor switching speed and temperature
- Lopez-Beudo et al. IEEE Design and Test'00
- Digital and more linear than diodes
- Dynamic configuration – inserted, moved, eliminated



Thermal Sensor Allocation and Placement

- **Related work**
  - Grid-based placement – Lopez-Beudo et al. FPGA'04
  - Bisection-based placement – R. Mukherjee et al. ICCAD'06
- **Motivation 1**



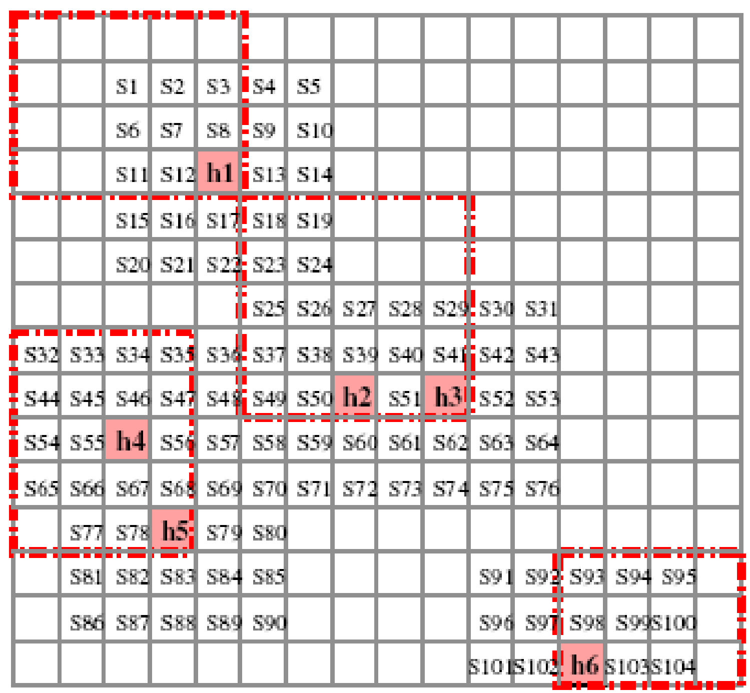
(a) Grid-based (b) bisection-based (c) Optimal partition

- **Motivation 2**
  - Sensor candidate CLBs may not be available
  - Need to be reconfigured to insert sensor
    → Change in hotspot map

Problem formulation

- **SAPP (Sensor Allocation and Placement Problem)**
  - Given
    - a $p \times q$ array of configurable logic blocks
    - A set H of hotspots on the FPGA
    - A sensor with covering range *l*
  - Find a set S of sensors and their locations on the FPGA
    - For each $h_i \in H$, there is $s_j \in S$ that covers hi by its covered region
    - |S| is minimum
- **SEN-opt**
  - Using unate covering problem, solves SAPP optimally.
  - Given a m*n matrix M, for which Mij is either 0 or 1
  - Finding a minimum cardinality column subset C

SEN-opt example



(a)Hotspots and sensor candidates (covering range : l=5)

	V						V				V				V
	S1	S2	......	S24	S25	S26	S27	......	S32	......	S55	......	S58	......	S104
h1	1	1		1											
h2					1	1	1						1		
h3							1								
h4									1		1				
h5											1		1		
h6															1

V : cover solution

(b) Constraint martix of (a)

Practical consideration

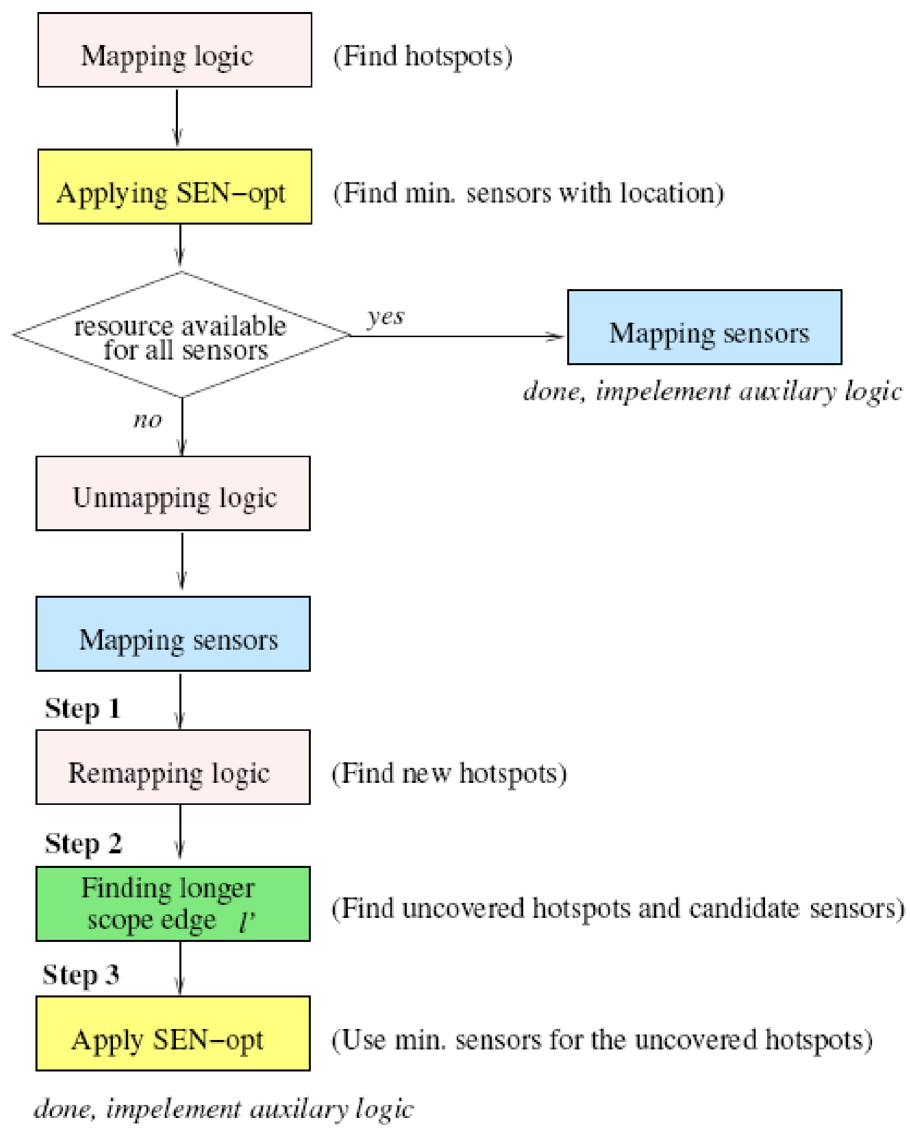
◆ Inserting thermal sensor, if resources for sensor are not enough

→ Need to move some existing logic

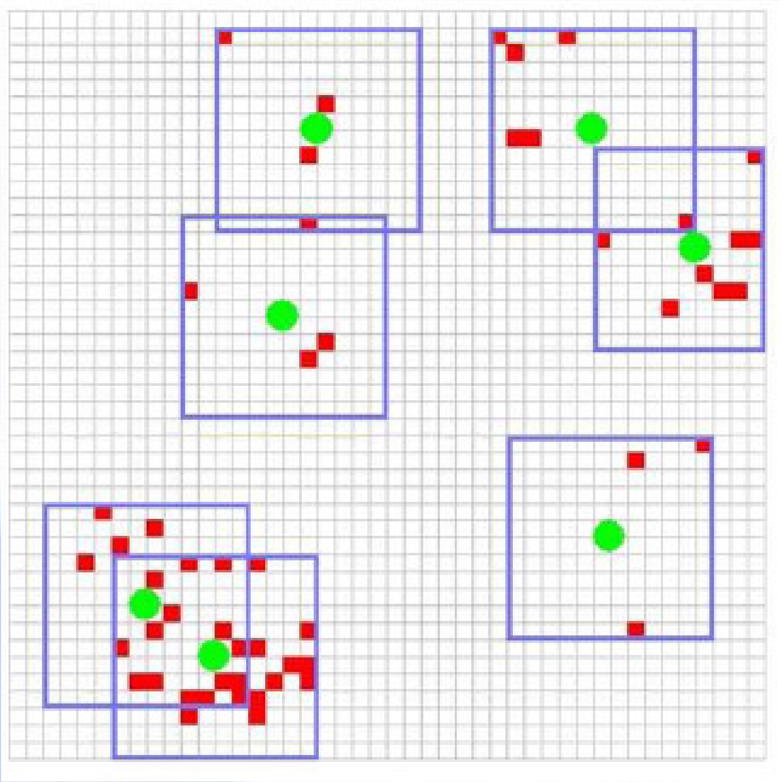
→Can affect the distribution of hotspot

◆ 3 steps (SEN-FLOW)

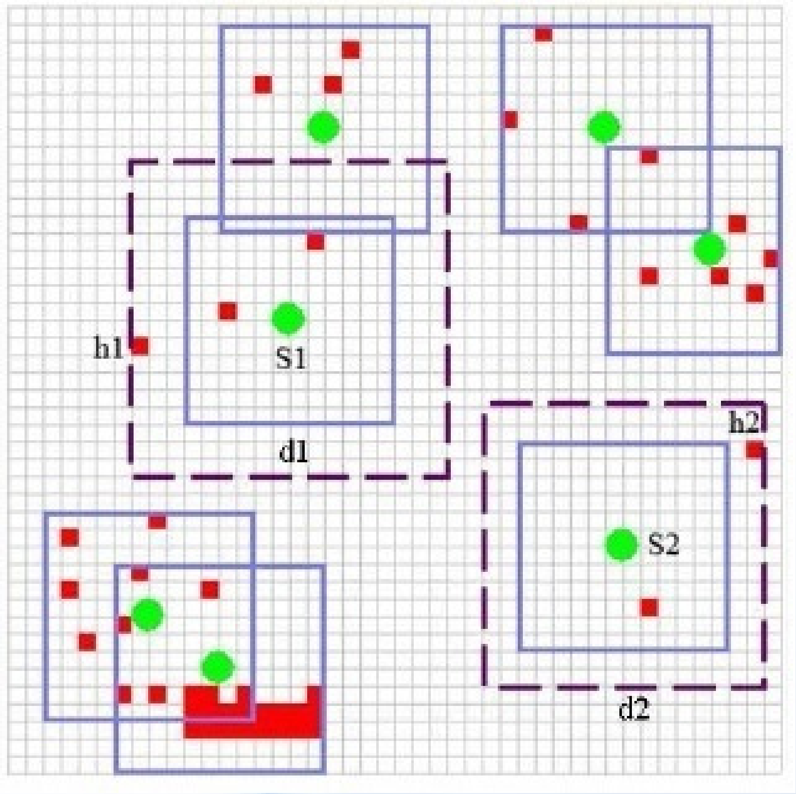
- 1st : Replacement and identification of new hotspot set
- 2nd : Extract uncovered hotspots
- 3rd : Find minimum sensors covering the uncovered hotspots with the covering range *l*'



Practical consideration example(1)



(a) Optimal sensor location by SEN-opt

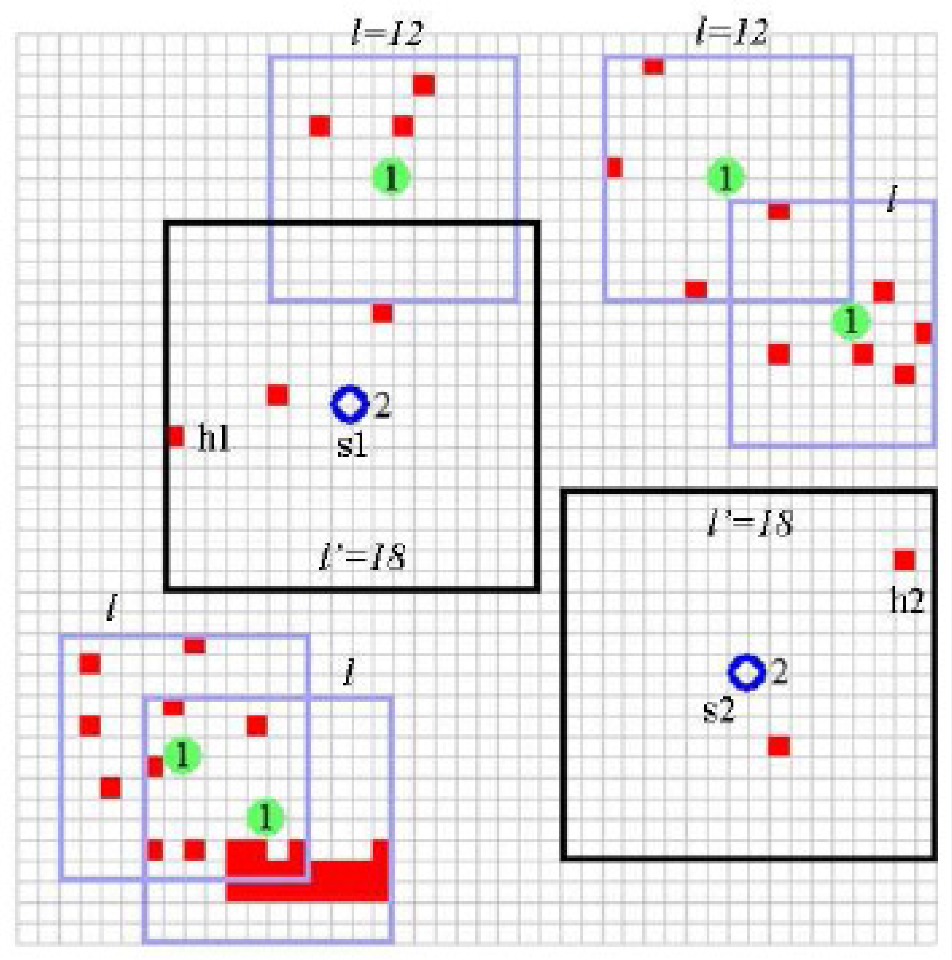


l'=max{d1,d2}=d1

(b) Logic remapping after sensor insertion

Practical consideration example(2)

(c) Covering h1, h2 using bigger covered region



Experimental result(1)

Experiment environment

- PC with 2GHz AMD processor
- Tested on a MCNC benchmark
- Tested on random generated designs
- Thermal simulation tool : Hotspot
- Power estimation tool : Power model for VPR

Experimental result(2)

- **Evaluate our techniques in three-fold**
  I. Checking the effectiveness of SEN-opt on a set of benchmarks over existing techniques
  II. Checking the efficiency of SEN-opt on a set of randomly generated designs
  III. Checking the effectiveness of SEN-FLOW on resolving the practical issue of the mapping conflict by the sensors and application logic

the effectiveness of SEN-opt (1)

Benchmarks	#hspot	number of sensors			red. Over Grid/Bisect
		Grid	Bisect	SEN-opt	
APEX2	20	6	4	3	50%/25%
DIFFEQ	6	6	3	2	67%/33%
CLMA	30	25	8	6	76%/25%
S38417	46	20	12	9	55%/25%
S38584.1	12	16	7	6	63%/14%
ELLIPTIC	12	9	3	3	67%/0%
EX1010	8	16	3	2	88%/33%
FRISC	38	9	8	6	33%/25%
PDC	17	12	4	4	67%/0%
SPLA	27	12	6	5	58%/17%
Avg.					62.4%/19.7%

the effectiveness of SEN-opt (2)

CLBs	96 x 64		128 x 86	
#hspots	# of sensors		# of sensors	
	Bisect	SEN-opt	Bisect	SEN-opt
30	16.5	15.8	19.0	18.4
35	19.1	17.6	22.6	20.9
40	19.8	18.1	24.2	22.8
45	22.6	20.6	26.1	24.3
50	23.3	19.8	28.3	25.7
55	22.5	20.3	30.7	27.5
60	25.7	21.9	32.8	29.8
65	27.0	22.8	34.5	30.2
70	27.6	23.4	35.5	31.2
75	28.9	24.3	37.4	31.7
Avg.	23.3	20.4	29.1	26.3
Red.		12.4%		9.8%

the effectiveness of SEN-FLOW

Benchmark	After SEN-opt #sensor	After remapping		After SEN-FLOW	
		#hspot (cov.)	#hspot (uncov.)	#sensor (*l*=12)	#sensor (*l*>12)
CLMA	6	10	7	3	3(l:20)
S38584.1	6	11	7	3	3(l:22)
S38417	9	17	8	7	2(l:20)
EX1010+SPLA	7	9	1	6	1(l:18)
FRISC+SPLA	8	43	8	5	3(l:28)
FRISC+EX1010	8	41	15	4	4(l:20)
COMPACT	7	43	2	5	2(l:18)

Conclusion

- **Proposing thermal sensor allocation and placement problem**
- **Proposing two solutions**
  - SEN-opt
    - Solution for SAPP
  - SEN-FLOW
    - Practical consideration

Thank You !