High Performance Current-Mode Differential Logic

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Outline

- Introduction
- Current-Mode Differential Logic (CMDL)
  - Basic Concepts
  - Structure of CMDL
  - Examples
- Design Cases
  - 32-bit Multiplexer
  - 8-bit shifter
  - 16-bit adder
- Performance comparison
- Conclusions and future work
Introduction

- Continuous scaling of semiconductor technology requires high performance circuit design:
  - Clock skew, wire delay and pipeline overhead increase:
    - Challenges on operation speed
  - Clock frequency becomes higher:
    - Challenges on power budgeting
  - Design that has lower delay*power is desired.
Previous works

- **Voltage-mode logic:**
  - Cascode Voltage Switch Logic (CVSL) [Heller et al. 1984]
  - Complementary Pass-transistor Logic (CPL) [Yano et al. 1990],
  - Low Voltage-Swing Logic (LVS) [Deleganes et al. 2004];

- **Current-mode logic:**
  - Dynamic Current-Mode Logic (DyCML) [Allam et al. 2001]

- **Properties:**
  - Differential logic: Common
  - Low swing vs. full swing output
    - Low swing output: LVS, CPL
    - Full swing output: DyCML, CVSL
  - Pre-charge/reset required vs. not required
    - Pre-charge/reset not required: CPL
    - Pre-charge/reset required: others
Cascode Voltage Switch Logic
[Heller et al. 1984]

- Introduced the concept of differential logic.
- Full swing outputs
- Outputs are pre-charged to low.
- Improvements:
  - SODS [Acosta et al. 1995]
  - DCSL [Somasekhar et al. 1996]
  - CSDL [Park et al. 1999]
Complementary Pass-transistor Logic
[Yano et al. 1990]

- Differential inputs and outputs.
- Drain and gate inputs
- Low swing outputs: extra inverters are needed.
- No pre-charge phase.
Low Voltage Swing logic [Deleganes et al. 2004]

- Differential inputs and outputs
- Low swing outputs: sense amplifier is needed
- Reset operation is needed.
  - Transistor count doubles.
  - Load on clock increases.
  - Need one extra stage of logic for thru-gate.
  - A reset phase is inserted to each clock cycle.
Dynamic Current-Mode Logic [Allam et al. 2001]

- Differential inputs and outputs
- Full swing outputs
- Pre-charged is required.
Current-mode differential logic

- Differential inputs and outputs
- Low swing outputs: sense amplifier is needed.
  - Fast operation speed
- Pre-charge/reset is not needed, only evaluation phase is needed.
  - Less number of transistors
  - No need for thru-gate: more headroom of logic depth
  - Low power consumption
- More reliable against noise effect
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Basic concepts of Current-mode logic

1. Fast operation speed
   - Reduced RC time constant

2. To maintain the low swing output
   - Current-mode logic inherently enables low swing operation.
   - For voltage-mode logic: reset operation is required.

3. To reduce the noise effect

\[
\tau_a = r_1 c_1 \\
\tau_b = \frac{r_2}{r_1 + r_2} r_1 c_1 \\
V_{1b} = \frac{r_2}{r_1 + r_2} V_{in}
\]
3. Immunity of noise in current-mode logic

- Current-mode loop in steady state can be approximated by a resistor loop.
- Node a1 has voltage V1, which is subjected to a noise $\Delta V$.
  - Noise in high-branch:
    \[
    \frac{\Delta V_{rs}}{\Delta V} = \frac{r_s}{r_{total} - r_1}
    \]
  - Noise in low-branch:
    \[
    \frac{\Delta V_{rs}}{\Delta V} = -\frac{r_s}{r'_{total} - r_1}
    \]
Basic Design blocks of CMDL

First stage

LVS:

Clock’

Thru-gate

LVSF

S0

CMDL:

a0

b0

a0’

b0’

To connect primary inputs

Middle stages

LVSG

Si

a0

b0

a0’

b0’

Si’

ai

bi

ai’

bi’

Last stage

LVSL

o

o’

Rs

CMDL

o

o’

To connect primary outputs
Design rules for CMDL

- The internal and output nodes are low swing, and the output must be greater than 0.1v (For Vdd=1.0v)
  - To guarantee the low swing outputs:
    - For any input pattern, the differential inputs must be connected through a shunt resistor or a closed transistor.
  - To guarantee the differential output is larger than 0.1v:
    - For each pair of differential output, there shall be no other shunt resistors or close transistors on the active path.
- The DCN can have multiple inputs and multiple outputs.
- Any path from the input to output has at most six stages of logic.
CMDL examples

2:1 multiplexer in CMDL

2-inputs NAND gate in CMDL
CMDL examples

2-inputs NOR gate in CMDL

2-inputs XOR gate in CMDL
CMDL examples

4:1 MUX in CMDL

When \( S_0 = 1 \), \( S_1 = 1 \), shunt transistor is needed to maintain the low swing at \( b_1, b_1' \).
CMDL examples

2-bit adder in CMDL

Controlled shunt resistor is used to avoid multiple shunts along $C_{in} \rightarrow C_{out}$ path
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32-bit Multiplexer

- Use 4:1 MUX as building block.
- Build 16:1 MUX with five 4:1 MUX.
- Build 32:1 MUX with two 16:1 MUX and one 2:1 MUX.
- Maximal logic depth is five.
8-bit rotator/shifter

- Adopt the barrel shifter structure proposed in [Pereira et al. 1995].
- Can left rotate or shift the operand by 0 to 7 bits.
- Maximal logic depth is 4.
- Function correctness:
  - proper input pattern

<table>
<thead>
<tr>
<th>Is</th>
<th>Ir</th>
<th>c1</th>
<th>c2</th>
<th>Out</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>In1</td>
<td>No shift</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>In2</td>
<td>rotate</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Padding 0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>Not allowed</td>
</tr>
</tbody>
</table>

Function table for RO/PA

2008-1-17
16-bit carry-skip adder

- Two kinds of cells:
  - Carry-skip cell (CS)
  - Full adder cell (FA)

- Primary inputs:
  - Carry propagation signal: Pi
  - Carry generation signal: Gi
  - Carry kill signal: Ki
  - Carry-skip control signal: Pij

- Maximal logic depth is six.
Sense amplifier

- A traditional sense amplifier from textbooks
- When En signal is high, sense amp is pre-charged to low.
- The cross-coupled PMOS and NMOS pair provide positive feedback loop for quick restoring.
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- **Conclusions and future work**
Experiment settings

- Three different logics are compared:
  - CMOS logic (standard cell),
  - LVS logic
  - CMDL.
- Three design cases are compared:
  - 32-bit MUX, 8-bit shifter and 16-bit adder
- Simulation tool: Hspice
- Library: TSMC-90nm technology
- Inputs and outputs:
  - inverters are used as inputs drivers and loads.
- Cycle time for each logic:
  - determined by the worst case delay.
- Sense amp outputs:
  - The high voltage of sense amp is greater than 0.8v.
- Power measurements:
  - 100 randomly generated input patterns are used.
Performance comparison

<table>
<thead>
<tr>
<th></th>
<th>32-bit MUX</th>
<th></th>
<th>8-bit Shifter</th>
<th></th>
<th>16-bit Adder</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CMOS</td>
<td>LVS</td>
<td>CMDL</td>
<td>CMOS</td>
<td>LVS</td>
<td>CMDL</td>
</tr>
<tr>
<td>Cycle time (ps)</td>
<td>200</td>
<td>215</td>
<td>180</td>
<td>200</td>
<td>210</td>
<td>180</td>
</tr>
<tr>
<td>Delay (ps)</td>
<td>195.6</td>
<td>153.8</td>
<td>118.7</td>
<td>165.3</td>
<td>148.4</td>
<td>120.7</td>
</tr>
<tr>
<td>Norm. Delay</td>
<td>1.00</td>
<td>0.79</td>
<td>0.61</td>
<td>1.00</td>
<td>0.90</td>
<td>0.73</td>
</tr>
</tbody>
</table>

- CMDL operates faster than CMOS
  - Differential small signal.
  - Diffusion Connected Network
- The speed of CMDL is comparable to LVS
  - Slower in adder case by 9%.
  - With the elimination of reset stage, the differential output needs to be charged from the opposite voltage level instead of zero.
Performance comparison

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<tr>
<td></td>
<td>CMOS</td>
<td>LVS</td>
<td>CMDL</td>
</tr>
<tr>
<td>Avg/Peak power(mW)</td>
<td>0.38/5.69</td>
<td>0.45/3.63</td>
<td>0.38/3.10</td>
</tr>
<tr>
<td>Norm. Avg Power</td>
<td>1.00</td>
<td>1.18</td>
<td>1.00</td>
</tr>
<tr>
<td>Input Power(mW)</td>
<td>0.15</td>
<td>0.17</td>
<td>0.16</td>
</tr>
<tr>
<td>Load Power(mW)</td>
<td>0.004</td>
<td>0.001</td>
<td>0.004</td>
</tr>
<tr>
<td>Sense Amp Power(mW)</td>
<td>-</td>
<td>0</td>
<td>0.002</td>
</tr>
<tr>
<td>Logic Power(mW)</td>
<td>0.23</td>
<td>0.28</td>
<td>0.21</td>
</tr>
</tbody>
</table>

- **CMDL is more power efficient than LVS**
  - Power saving: 15%, 14% and 40% for three cases.
  - Due to the elimination of reset network
- **CMDL dissipates more power than CMOS**
  - Power increase: 14% and 23% for shifter and adder.
  - Static current: ~10uA
  - More overhead comes from inputs, loads and sense amps.
Performance comparison

CMDL has the best delay*power metric.
- The reduction is up to 50%.
- The delay^2*power is also reduced by up to 80%.

CMDL has the smallest number of transistors.
- Usage of Diffusion Connected Network
- Elimination of the reset network

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<td>LVS</td>
<td>CMDL</td>
<td>CMOS</td>
<td>LVS</td>
</tr>
<tr>
<td>Delay × Power (fJ)</td>
<td>74.33</td>
<td>69.21</td>
<td>45.11</td>
<td>59.51</td>
<td>71.23</td>
</tr>
<tr>
<td>Norm. Delay × Power</td>
<td>1.00</td>
<td>0.93</td>
<td>0.61</td>
<td>1.00</td>
<td>1.20</td>
</tr>
<tr>
<td>Delay^2 × Power (pJ×ps)</td>
<td>14.54</td>
<td>10.64</td>
<td>5.35</td>
<td>9.84</td>
<td>10.57</td>
</tr>
<tr>
<td>Norm. Delay^2 × Power</td>
<td>1.00</td>
<td>0.73</td>
<td>0.37</td>
<td>1.00</td>
<td>1.07</td>
</tr>
<tr>
<td>Total Transistor Count</td>
<td>312</td>
<td>322</td>
<td>162</td>
<td>392</td>
<td>316</td>
</tr>
<tr>
<td>Transistor Overhead</td>
<td>0</td>
<td>145.8%</td>
<td>23.7%</td>
<td>0</td>
<td>49.1%</td>
</tr>
</tbody>
</table>

2008-1-17
Waveforms of different logics

**CMDL waveform**

- (1.2689n, 0.50055)
- (1.5553n, 0.49982)

**LVS waveform**

- (1.1652n, 0.49977)
- (1.4168n, 0.50066)

**CMOS waveform**

- (933.84p, 0.50167)
- (1.6433n, 0.50053)
Conclusions and future work

- The effectiveness of CMDL is demonstrated by three design cases.

- Simulation results show that:
  - CMDL can achieve much better delay*power and delay²*power.

- Next steps:
  - Detailed experiments of energy overhead of CMDL on small circuit
  - Noise test of CMDL
  - Technology scaling
  - Other possible alternative architectures
Thank you