ECE Illinois

UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN | COLLEGE OF ENGINEERING

Variation and Error-Aware Design for Billions of Devices on a Chip

ASPDAC'08 Panel
Best Ways to Use Billions of Devices on a Chip

Deming Chen

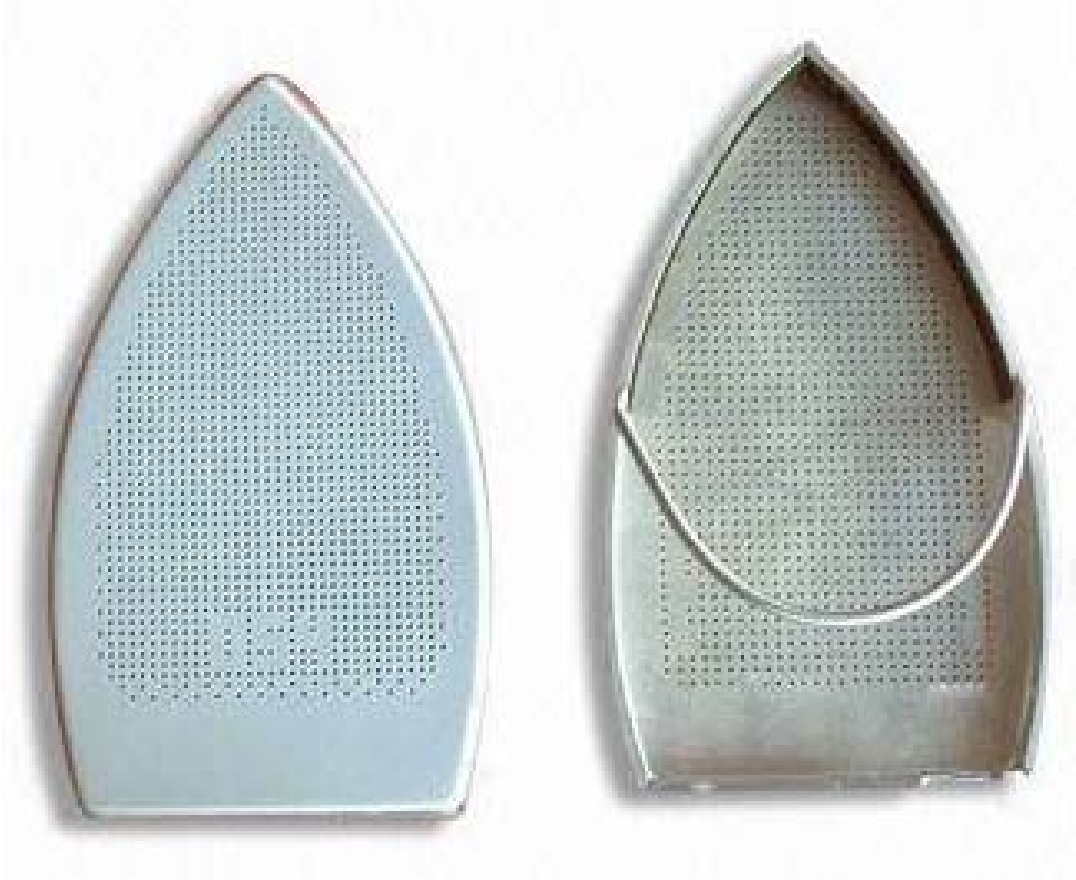
COORDINATED SCIENCE LABORATORY

- Great power comes with great risks

Reliability

Complexity

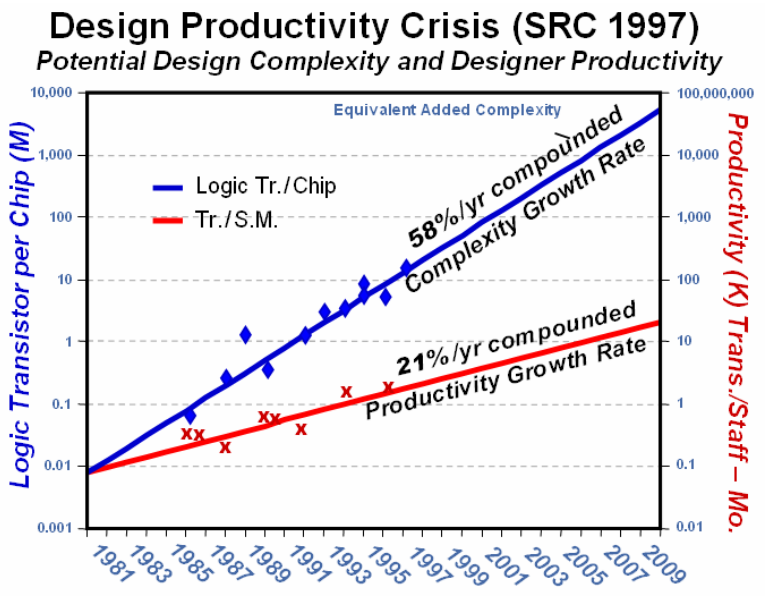
Iron Shoes



Deep Submicron Non-Idealities

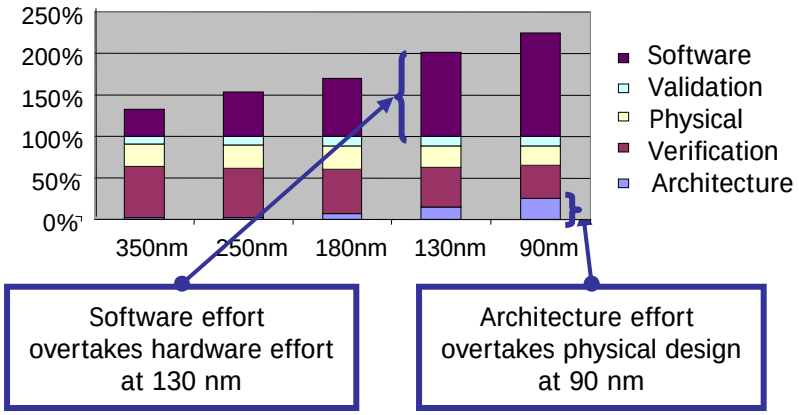
- Parameter variation
  - Deviation of process, voltage, and temperature (PVT) parameters from nominal values
  - Can cause timing errors and power violations
- Soft errors
  - Cosmic particle, such as a neutron, strikes close to a reverse-biased drain junction causing a voltage glitch
- Wear-out
  - Gate oxide breakdown (OBD)
  - Electromigration (EM)
  - Negative bias temperature instability (NBTI)
  - Hot carrier injection (HCI)
- Manufacturing defects
  - Stuck-at and bridging faults
  - Faults due to antenna, thermal and inductive effects, as well as diffraction patterns

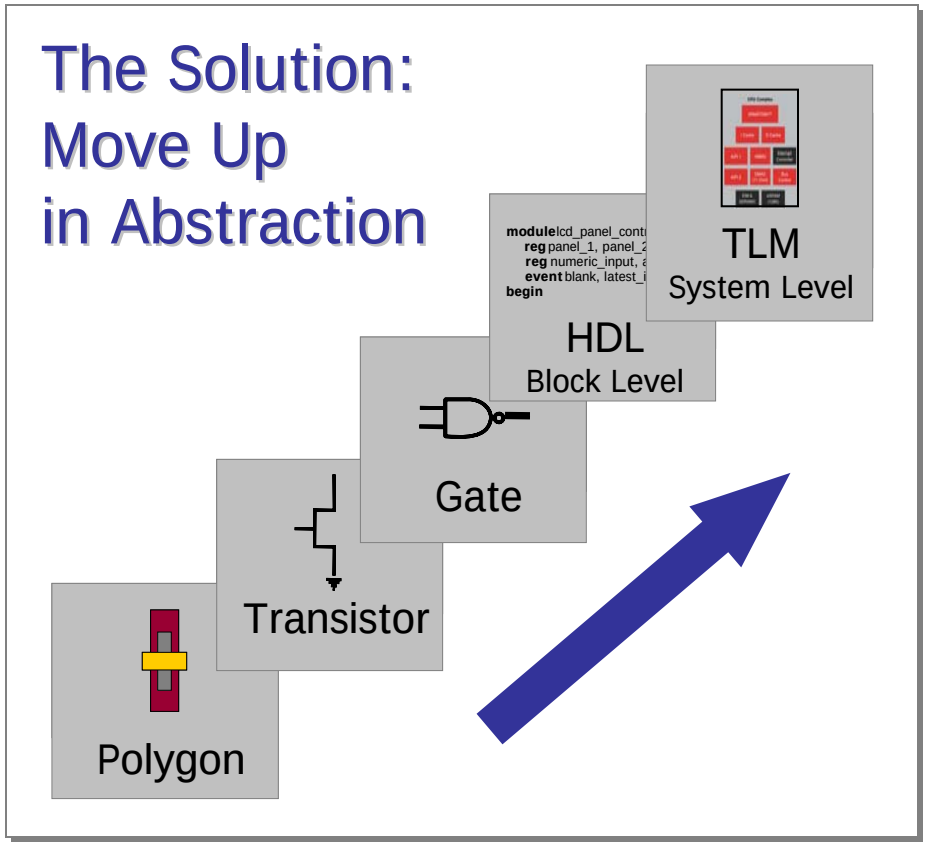
Complexity and Productivity



Relative Effort by Designer Role

IBS

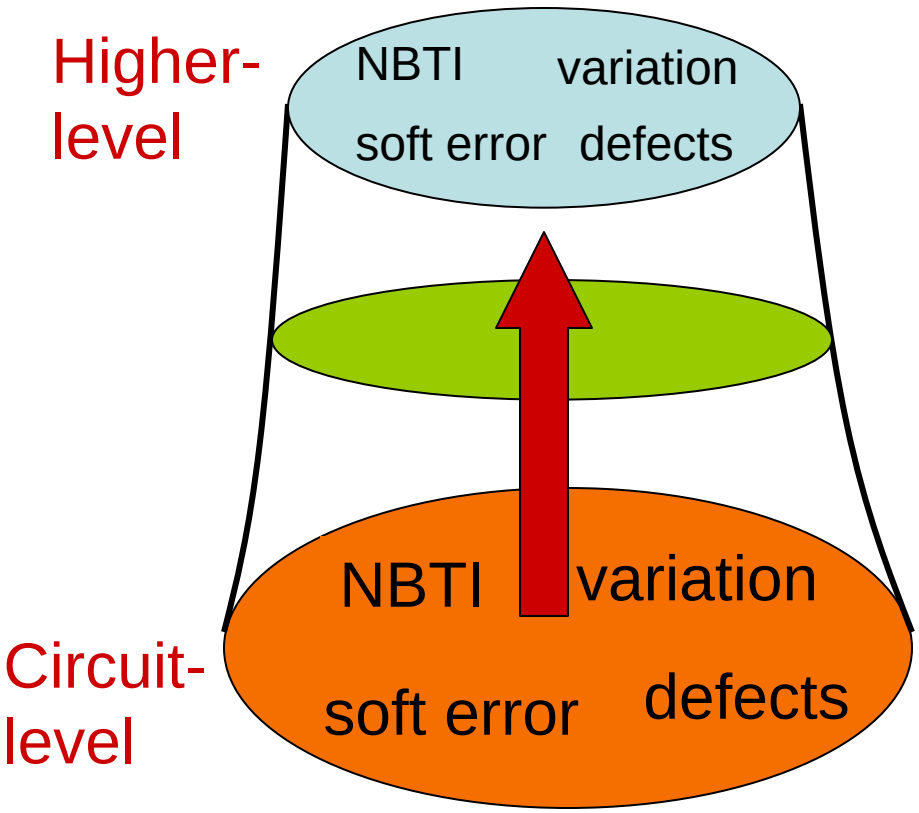




Source: CoWare

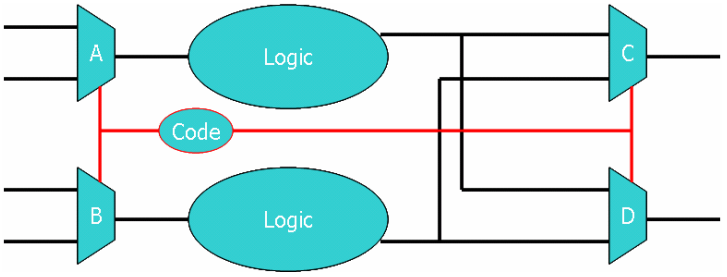
Solutions (1)

- Modeling
  - Comprehensive reliability models considering the combined effects of the non-ideality sources
  - Capture low-level non-idealities in system level

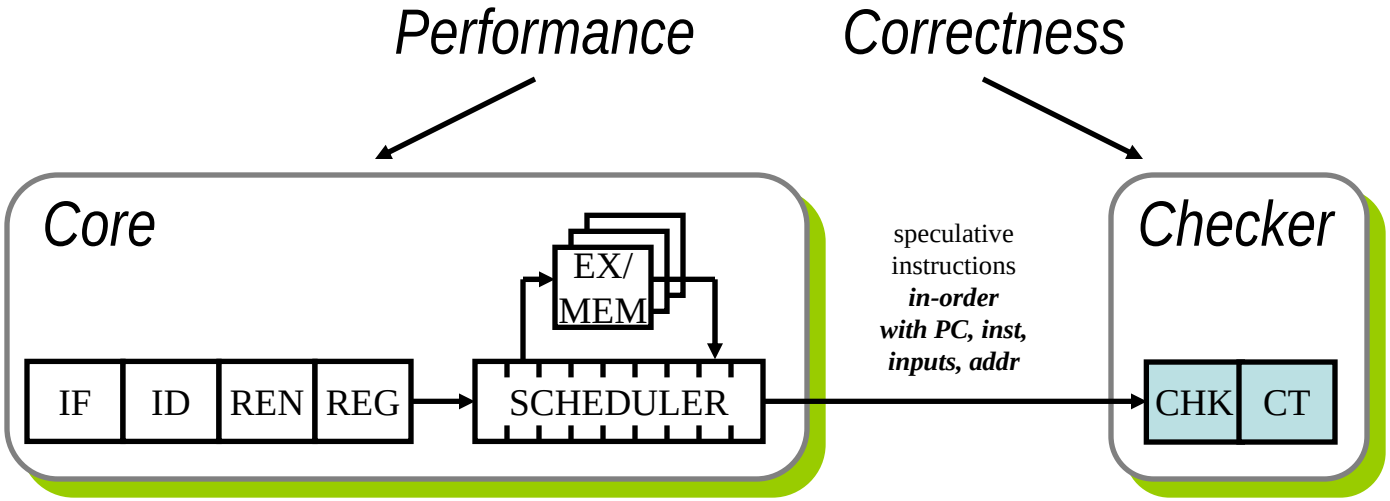


Solutions (2)

- Design
  - New circuit, logic and architectural techniques with high reliability and low area/power overhead



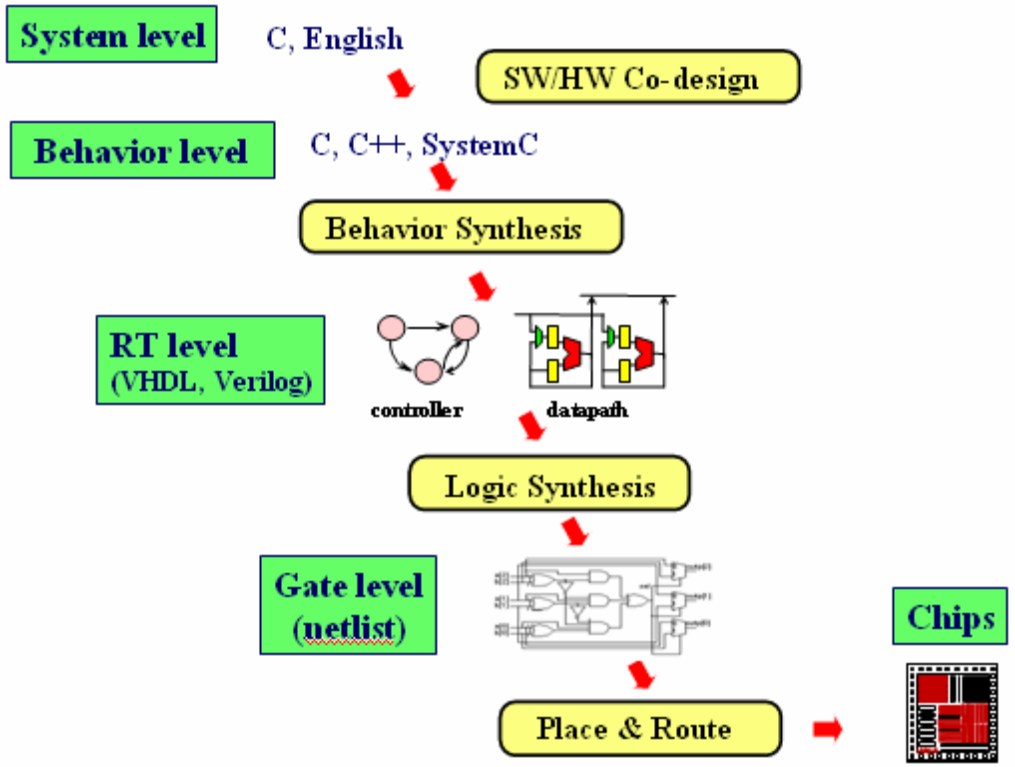
Pair modular redundancy



DIVA checker (source: T. Austin)

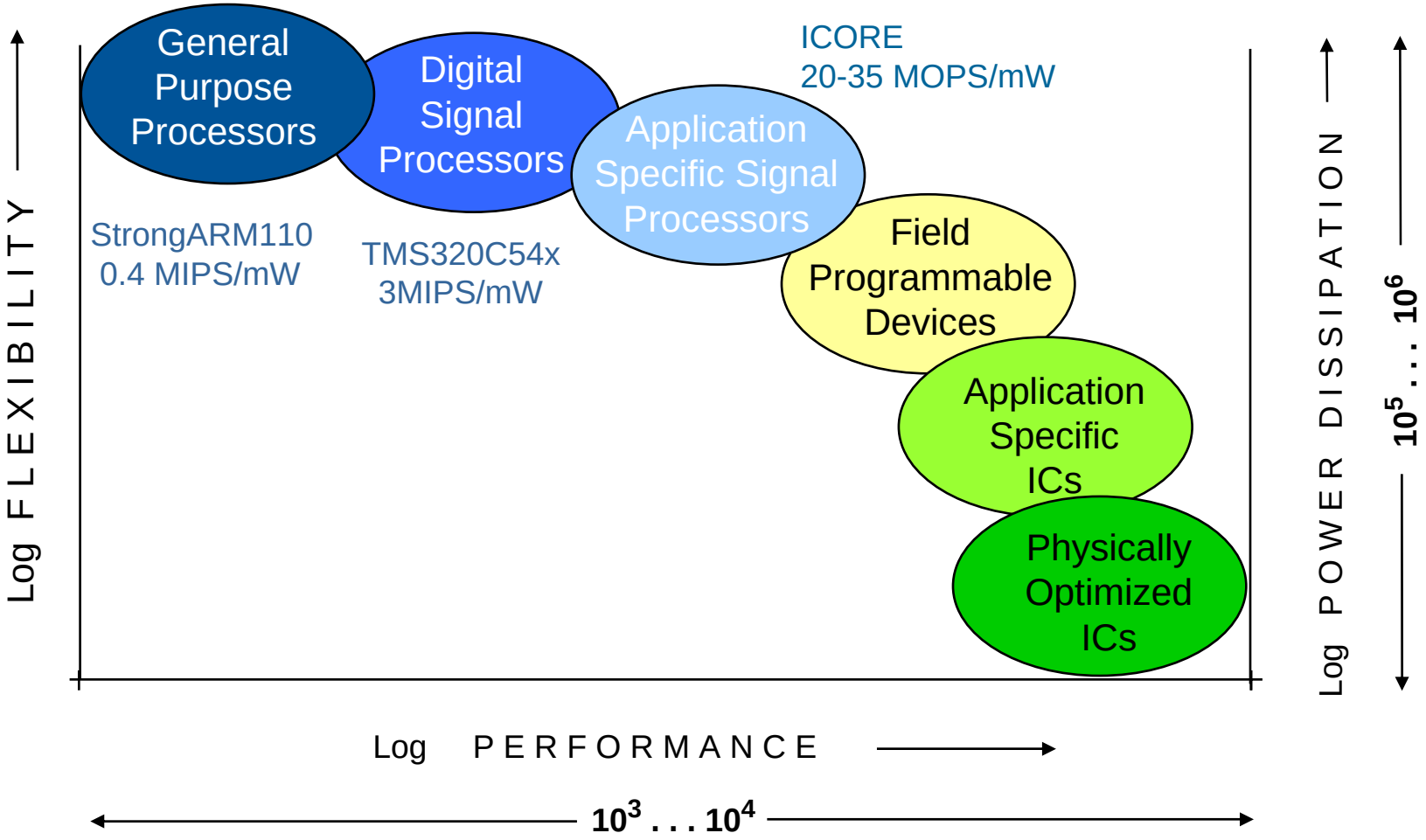
Solutions (3)

- Synthesis
  - Variation and error-aware synthesis crossing all the design levels
  - Guided by the corresponding models



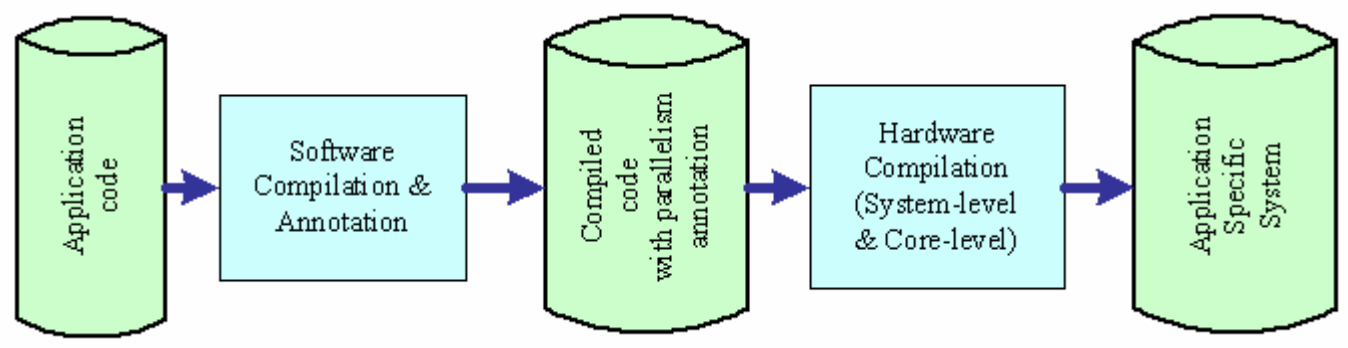
- New ways to best-use these devices

Energy/Performance/Flexibility



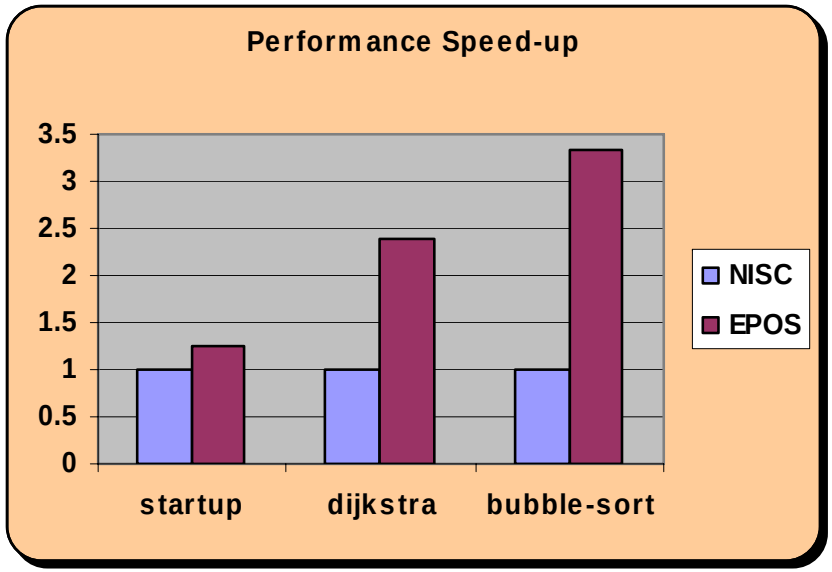
Source: T.Noll, RWTH Aachen

ASM: Application-Specific Multicores

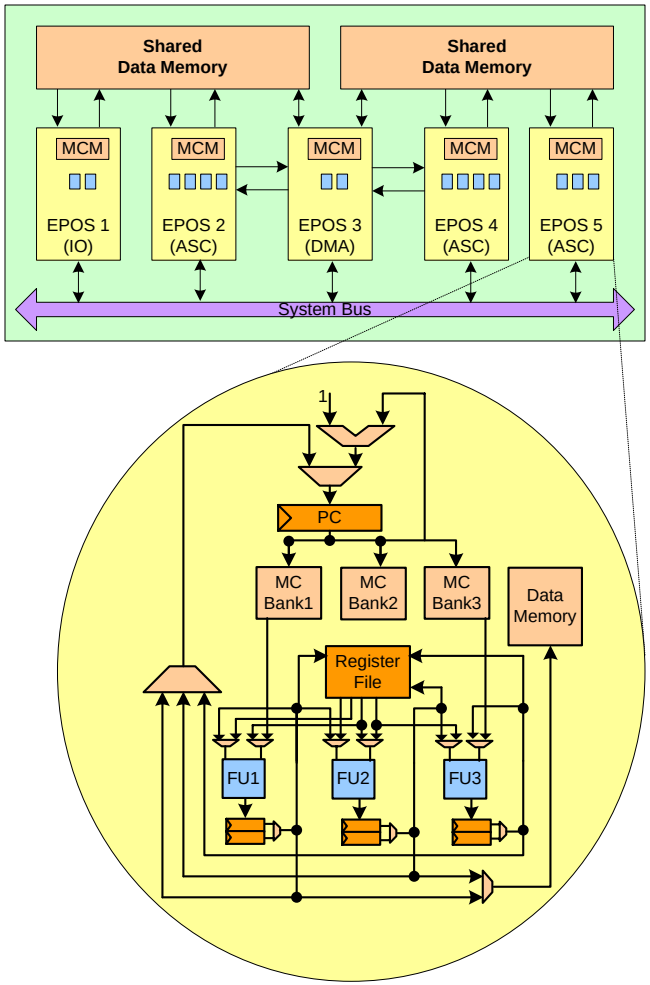


- An advanced software compiler for extracting both the fine-grain and coarse-grain parallelism available in the application
- A custom instruction-less processor which is built to fit the tasks it is assigned to
- A hardware compiler which combines the parallelism information extracted by the software compiler and the customization flexibility of the instruction-less processor to build an efficient multicore system for the application

System Synthesis for ASM



- Performance gain of a single EPOS core (Explicitly Parallel Operations System)



- A multi-core system