ASP-DAC 2008 Designer's Forum Panel

Best Ways to use Billions of Devices on a Chip

Thursday 24 January 2008: 1550-1755

Moderator:

Grant Martin, Tensilica

Theme of Panel

- What are the “Best” ways to use the billions of transistors we can build at 45, 32, 22, 16 nm?
  - More processors?
  - More memory?
  - More elaborate on-chip interconnect and networks?
  - More redundancy for defect tolerance?
  - More structures for dynamic error recovery?
  - More of everything needed to reduce power and energy?
- At the same time, what are some of the “Worst Ways”?
  - Architectural deadends?

Panelists

- Nikil Dutt, UC Irvine
- Deming Chen, UIUC
- KyungHo Kim, Samsung
- Jörg Henkel, University of Karlsruhe
- Kazutoshi Kobayashi, Kyoto University