

Designer's Forum at ASP-DAC

Best Ways to use Billions of Devices on a Chip

Panel presentation by

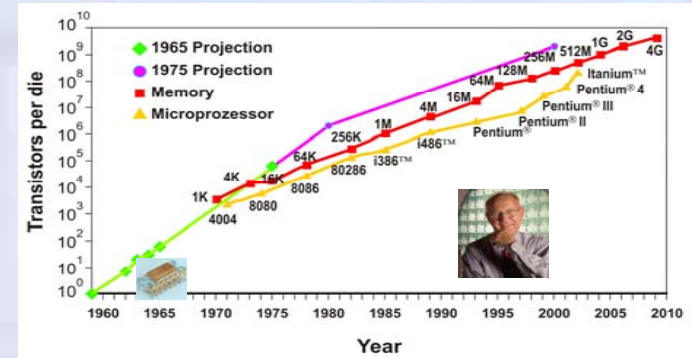
J. Henkel, Univ. Karlsruhe

Seoul, Jan. 25th 2008

In the past ...

□ ... Moore's Law provided a win-win- situation:

- Smaller feature size
- Higher integration density
- Lower power consumption
- Higher speed (performance)
- Less cost (per-transistor costs)
- ...



ITRS

Scalability, as we experienced for the last four decades is at its end as we enter the Nano Era!

In the future ...

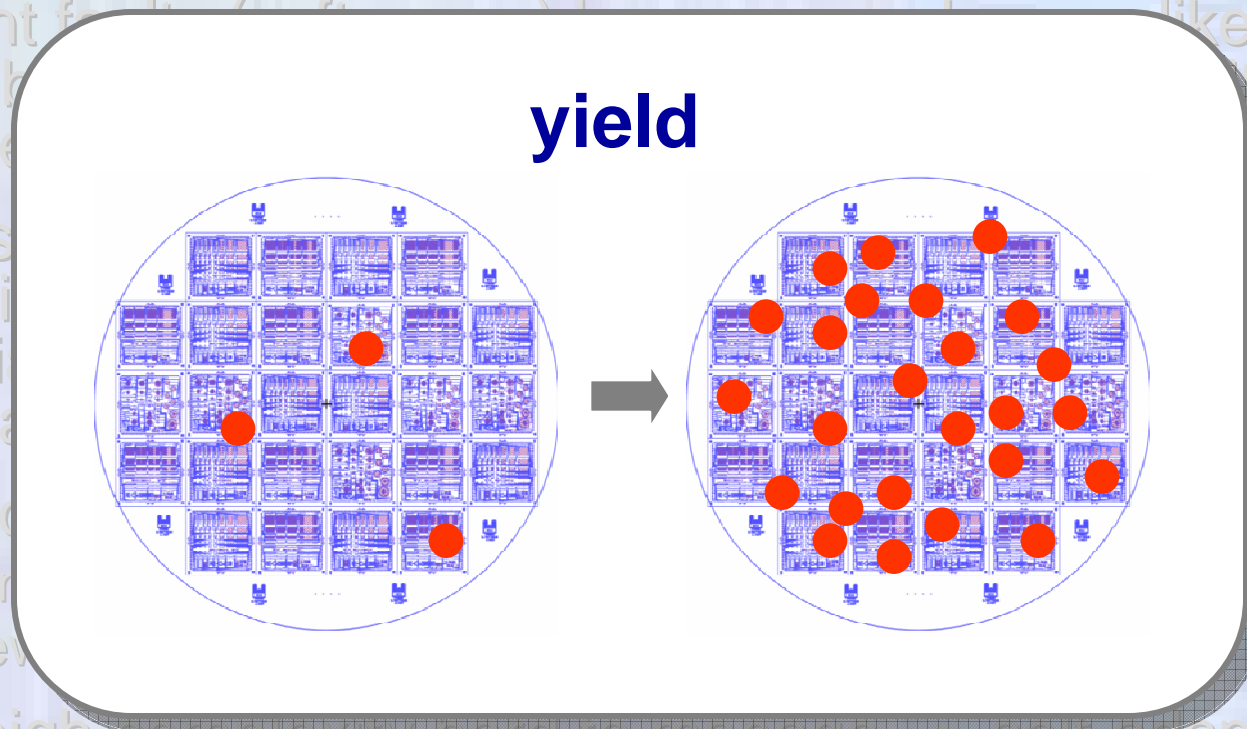
- ❑ New structures will be hard to integrate => **yield decreases drastically** => “live” with faults rather than avoiding them (expensive and/or impossible)

- ❑ Transient faults (soft errors) likely => need to be tolerated

- ❑ Errors (soft errors) abstractly appropriate configurations

- ❑ 3-D structures
 - ❑ Routing
 - ❑ => new

- ❑ Future high complexity hard to manage => self-adaptation and self-organization is needed



In the future ...

- ❑ New structures will be hard to integrate => yield decreases drastically => “live” with faults rather than avoiding them (expensive and/or impossible)
- ❑ **Transient faults** (soft errors) become much more likely => need to be considered in the design process => fault tolerance plays a key role

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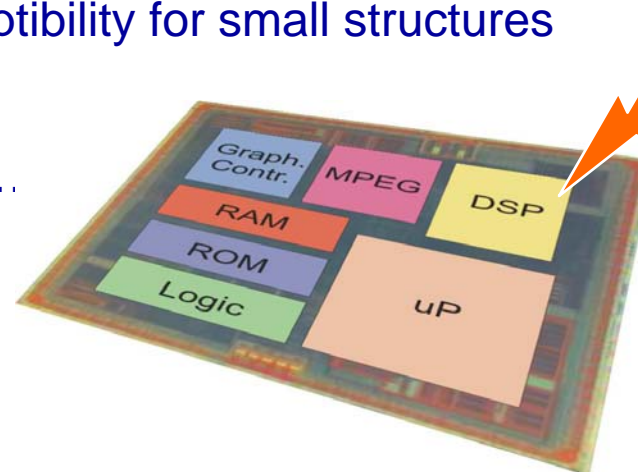
- ❑ 3-D structures
 - ❑ Routing, ...
 - ❑ => new design

- ❑ Future high performance and self-organizing

Soft errors

- cause: e.g. through cosmic rays (neutron strike)
- high susceptibility for small structures widths

=> bit flips, ...



In the future ...

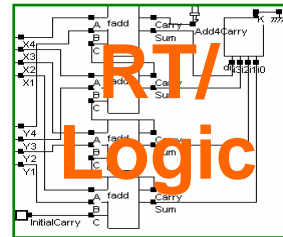
- ❑ New structures drastically (expensive)
- ❑ Transient faults need to be tolerance p
- ❑ **Errors** (soft abstraction appropriate configurabi
- ❑ 3-D structures
 - ❑ Routing,
 - ❑ => new c
- ❑ Future high and self-org

```

PROCEDURE DoPegModel1
CONST
  h = 3; d = 1; rat = 2; q = 4; nq = 5
BEGIN
  IF P1 == 0
  BEGIN
    Score(q, 1);
    Score(r, 1);
  END ELSE
  IF Fall(h) THEN
  BEGIN
    Score(r, Fall(h));
  END
END
  
```

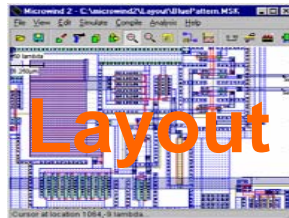
SW

Errors

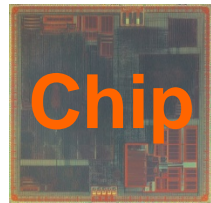


**RT/
Logic**

**address at
all levels
of abstraction !**



Layout



Chip

> yield decreases
avoiding them

more likely =>
SS => fault

at all levels of
are to designing
=> re-

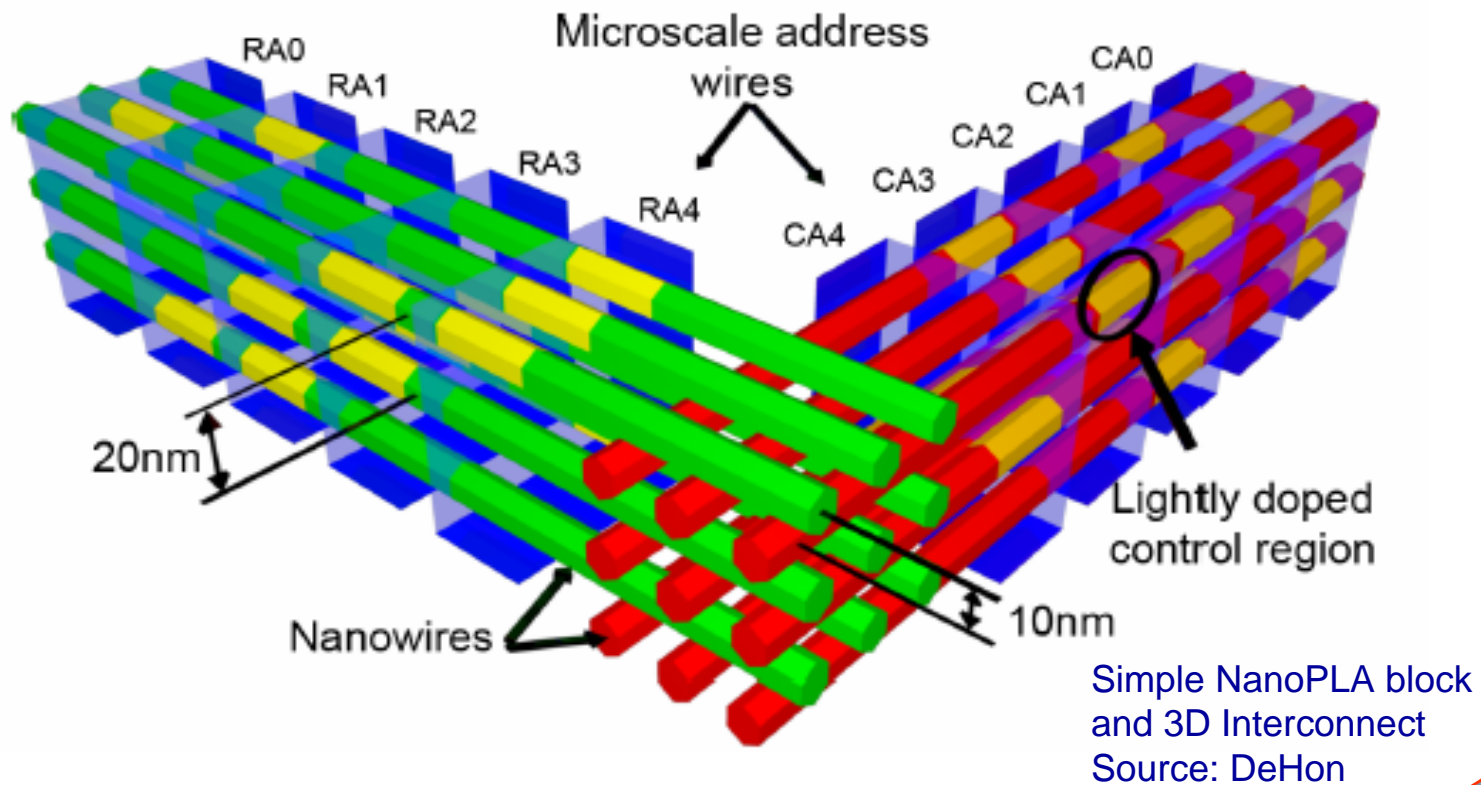
ity etc

> self-adaptation

In the future ...

Reconfigurability as a means to address errors

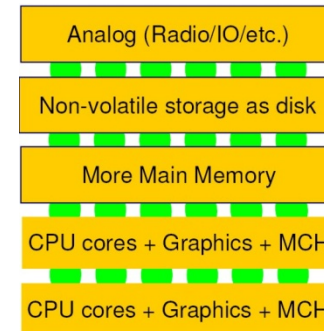
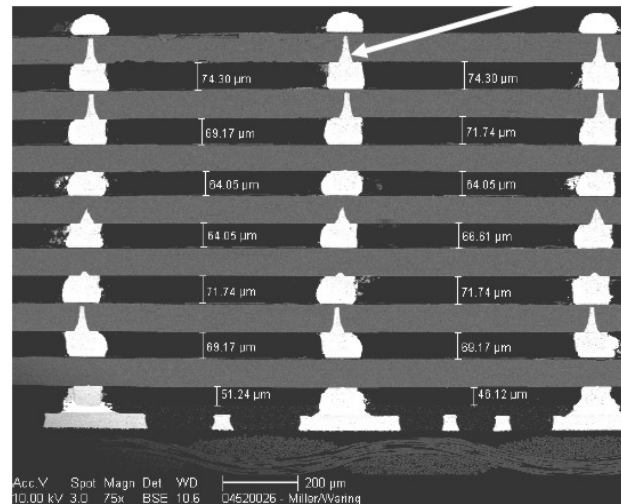
Shown: 3-D PLA



In the future ...

- New s
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- Transi
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- Errors
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3-D structures



(src: Yuan Xie)

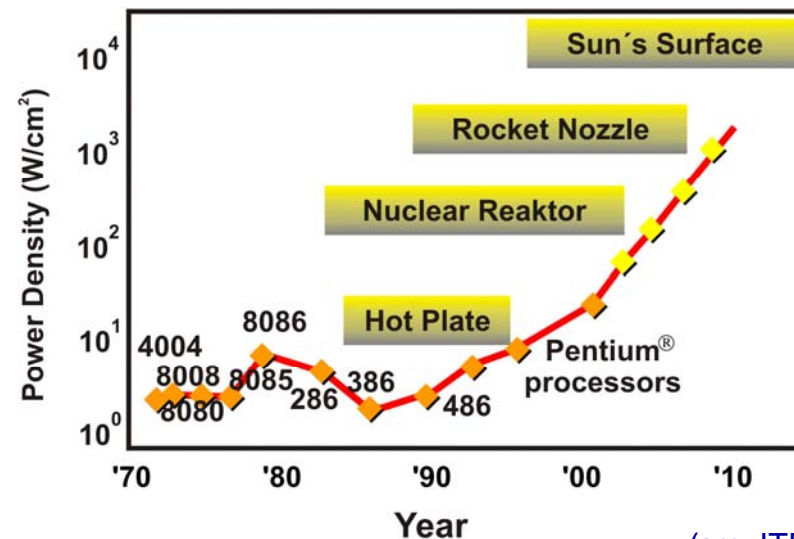
- **3-D structures** imply new problems in
 - Routing, placement, heat, electrical compatibility etc
 - => new design/synthesis methods are needed
- Future high complexity hard to manage => self-adaptation and self-organization is needed

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In the future ...

- New structures drastically (expensive)
- Transient need to be tolerance
- Errors (so abstraction appropriate configurability)

3-D structures: problems



(src: ITRS)

- **3-D structures** imply new problems in
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In the future ...

- ❑ New structures will be hard to integrate => yield decreases drastically => “live” with faults rather than avoiding them (expensive and/or impossible)
- ❑ Transient faults (soft errors) become much more likely => need to be considered in the design process => fault tolerance plays a key role
- ❑ Errors (soft or hard) need be considered at all levels of abstraction from manufacturing the hardware to designing appropriate software => higher flexibility => re-configurability
- ❑ 3-D structures imply new problems in
 - ❑ Routing, placement, heat, electrical compatibility etc
 - ❑ => new design/synthesis methods are needed
- ❑ Future **high complexity** hard to manage => **self-adaptation and self-organization is needed**

Summary Problems

- ❑ Power (Reduction, Delivery, Distribution)
- ❑ Heat (Reduction, Removal, Dealing with hot spots)
- ❑ Interconnects (Reduce length/delay, Reduce number)
- ❑ Testability / Verification (Reducing associated costs)
- ❑ Reliability (Economical redundancy factors, Reconfiguration, Adaptive)
- ❑ Communication (Low-power, Non-flooding, Reliable)
- ❑ Hybrid integration (Mixed design, Interfacing)
- ❑ Logic and coding (Non-Boolean(?), Error correction, Spikes)
- ❑ Algorithms (Stochastic / Probabilistic)
- ❑ Design complexity (Reduce associated cost by reuse)

Solutions

❑ Near term solutions:

- ❑ Massively parallel, modularity (cells, blocks)
- ❑ Regularity (grid processing, cellular arrays)
- ❑ Locally connected (near-neighbor connections, crossbar)
- ❑ Higher functionality (multiple valued logic, threshold logic)
- ❑ Reconfigurability (self-mapping)

❑ Medium term solutions:

- ❑ Asynchronous (including GALS)
- ❑ Fault-tolerance (noise immune, redundant, self-testing, self-correcting)

❑ **Defect-tolerant (adaptable/reconfigurable)**

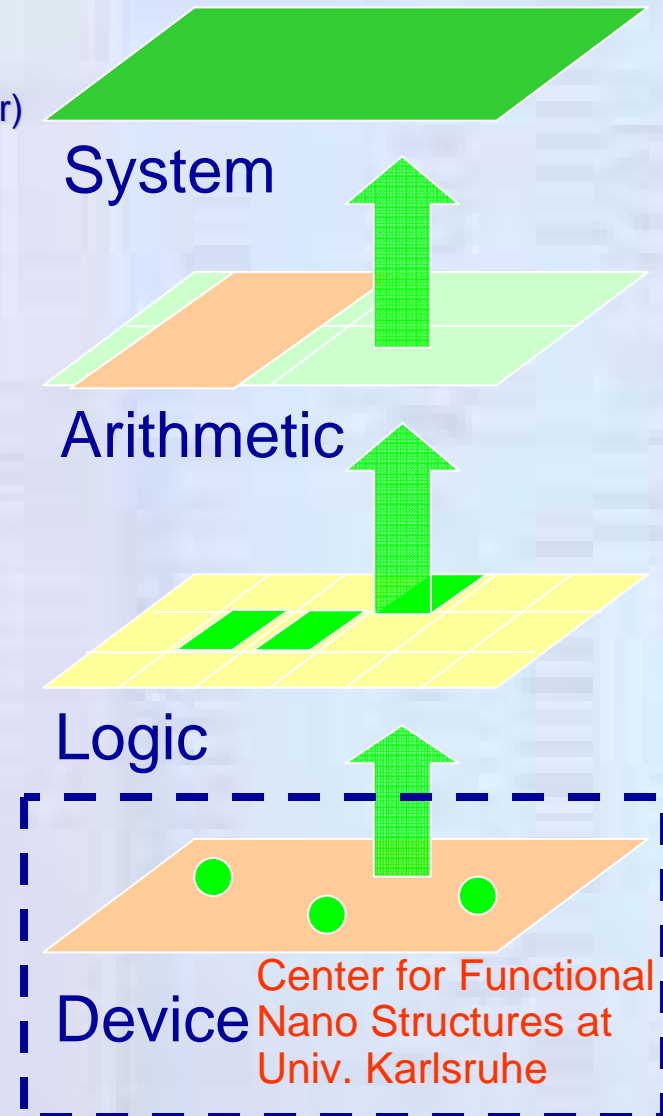
- ❑ Redundant, adaptive (self-adaptive, self-organizing, evolvable)

❑ **Bio-inspired (complex functions, self-organizing, self-healing)**

- ❑ Nanophotonic (optical communication, GOLE)
- ❑ Nanofluidic
- ❑ 3D interconnects
- ❑ Probabilistic (algorithms, encoding, communication)

❑ Long term solutions:

- ❑ molecular, quantum
- ❑ quantum-dot cellular automata
- ❑ Adiabatic / reversible
- ❑ Bio-compatible



Multidisciplinary Research Effort at Univ. Karlsruhe

- ❑ Creation of a NEW FIELD GROUP (est. 2007) to address the high-lighted problems
- ❑ Multidisciplinary Research
 - ❑ Computer Science
 - ❑ J. Henkel, W. Karl, ...
 - ❑ Electrical Engineering
 - ❑ J. Becker, J. Leuthold, ...
 - ❑ Physics
 - ❑ G. Schoen, H. Hahn, ...

We do not have as many devices available for computation/communication as we may think we have!

Devices from CFN Karlsruhe

