The Future of Semiconductor Industry – A Foundry's Perspective –

Dr. F.C. Tseng
Vice Chairman
TSMC
January 24, 2008
Outline

- Semiconductor Market Outlook
- Challenges and Solutions
  - Economic
  - Technology
- Summary
Semiconductor Market Will Continue to Grow

Source: SIA

<table>
<thead>
<tr>
<th>Year</th>
<th>Growth</th>
</tr>
</thead>
<tbody>
<tr>
<td>'02</td>
<td>+1%</td>
</tr>
<tr>
<td>'03</td>
<td>+18%</td>
</tr>
<tr>
<td>'04</td>
<td>+28%</td>
</tr>
<tr>
<td>'05</td>
<td>+7%</td>
</tr>
<tr>
<td>'06</td>
<td>+9%</td>
</tr>
<tr>
<td>'07</td>
<td>+4%</td>
</tr>
<tr>
<td>'08E</td>
<td>+7~9%</td>
</tr>
</tbody>
</table>
Steady Market Expansion

Increasing semiconductor penetration in electronics

<table>
<thead>
<tr>
<th>Category</th>
<th>'01</th>
<th>'05</th>
<th>'10E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Processing</td>
<td>20.9%</td>
<td>27.2%</td>
<td>28.8%</td>
</tr>
<tr>
<td>Communications</td>
<td>13.5%</td>
<td>16.4%</td>
<td>18.8%</td>
</tr>
<tr>
<td>Consumer Electronics</td>
<td>12.6%</td>
<td>16.3%</td>
<td>19.5%</td>
</tr>
</tbody>
</table>

Source: WSTS, IC Insights, TSMC estimates
Increasing Semiconductor Content in Systems
– Functionalities and performance

Source: Gartner, iSuppli, Strategy Analytics
New Applications as Growth Drivers

<table>
<thead>
<tr>
<th>Units / End User</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/10000</td>
<td>'70</td>
</tr>
<tr>
<td>1/100</td>
<td>'80</td>
</tr>
<tr>
<td>1/1000</td>
<td>'90</td>
</tr>
<tr>
<td>1</td>
<td>'00</td>
</tr>
<tr>
<td>100</td>
<td>'10</td>
</tr>
</tbody>
</table>

- Mainframe
- Minicomputer
- PC
- Consumer Electronics (3C Convergence)
Demand from High-end and Low-end Markets

More Functionality
- Voice
- Video
- Messenger
- GPS
- Wi-Fi
- Camera
- PDA
- MP3

Lower Price

Year

'90

'00

'05

Price

Functionality

✓ Voice
✓ SMS
✓ WAP

✓ Voice

✓ Voice
In Search of A PC to Serve “The Next Billion”

- The low-cost PCs for the developing nations:

  - INTEL “ClassMate”
  - ASUS “Eee”
  - One Laptop Per Child “XO”
Growth Opportunities are Global

Source: “The fortune at the bottom of the pyramid” by C. K. Prahalad, and IMF
Plenty of Opportunity Ahead

Source: US Census Bureau; IC-Insights; TSMC estimates
Outline

- Semiconductor Market Outlook
- Challenges and Solutions
  - Economic
  - Technology
- Summary
Challenges

**Economic**

1. Huge CapEx
2. ROI Risk – Process
3. ROI Risk – Product

**Technology**

4. Nanometer Manufacturing
5. Nanometer Design
6. Design Complexity
1. Huge CapEx

- Capital expenditure for constructing a new fab is rapidly increasing
  - Major factor for financing and future profit

<table>
<thead>
<tr>
<th>Size</th>
<th>Capital Cost (B$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6-inch</td>
<td>$0.4B (20K WPM)</td>
</tr>
<tr>
<td>8-inch</td>
<td>$1B (20K WPM)</td>
</tr>
<tr>
<td>12-inch</td>
<td>$3B (30K WPM)</td>
</tr>
<tr>
<td>18-inch</td>
<td>$8B (GigaFab with 100K WPM)</td>
</tr>
</tbody>
</table>
Solution – Foundry Based Business Model

- Many IDMs are changing to either fab-lite or fabless
- A wide variety of consolidation and collaboration are inevitable

<table>
<thead>
<tr>
<th>Past</th>
<th>Present</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design</td>
<td>Product Focused IDM</td>
<td>IP Vendor</td>
</tr>
<tr>
<td>Product</td>
<td>IDM Getting Fab-lite</td>
<td>Fabless</td>
</tr>
<tr>
<td>Manufacturer</td>
<td>Assembly &amp; Test</td>
<td>Foundry</td>
</tr>
<tr>
<td>Distribution</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OEM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Vertically Integrated | IDMs in Transition, Fabless Getting Bigger | Few IDMs & Foundries, Many Fabless
2. ROI Risk – Process

- Incremental challenges in developing next generation processes
- Process technology development costs are continuously increasing

<table>
<thead>
<tr>
<th>Technology</th>
<th>Development Cost</th>
<th>Ramp-up Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.13um</td>
<td>$0.5B</td>
<td></td>
</tr>
<tr>
<td>90nm</td>
<td>$0.7B</td>
<td></td>
</tr>
<tr>
<td>65nm</td>
<td>$0.9B</td>
<td></td>
</tr>
<tr>
<td>45nm</td>
<td>$1.1B</td>
<td></td>
</tr>
<tr>
<td>32nm</td>
<td>$1.4B</td>
<td></td>
</tr>
<tr>
<td>22nm</td>
<td></td>
<td>$0.5B</td>
</tr>
</tbody>
</table>
2. ROI Risk – Process (Cont’d)

- Yield ramp-up requires significant time and investment

In-house manufacturing with limited products

Foundry has the economy of scale

- 25% Q-to-Q Improvement
Solution I – Technology Alliance

- Collaboration is required to overcome ever-increasing financial as well as technical challenges
Solution II – Collaboration among Foundry, IP/EDA Vendors, And Design Service Suppliers

- Standardization of IP & EDA tools
3. ROI Risks - Product

- Design complexity and cost increase rapidly
- Short time to market
Solution - Product

- Optimal system partition
- Foundry
  - Design Infrastructure
    - SPICE
    - PDK
    - Foundation IP
  - Prototyping
    - Cybershuttle
    - MLM

Minimize the product risk and NRE
4. Nanometer Manufacturing

- New materials and device structure
  - High-K gate dielectric
  - Metal gate
  - 3D FINFET
  - Low-K Interconnect

- New EDA solutions for technology modeling and advanced lithography
Solution – Technology Modeling / Advanced Lithography

- Secure accurate SPICE modeling
  - Systematic effect
    - STI
    - WPE
    - Strained silicon effect
    - OPC
  - Random effect
    - Corner model
    - Statistical model

- Modeling in new material, 3D device and equipment / topography

- Polarization, OPC, double exposure and mask 3D effects

Collaborate with EDA vendors to achieve seamless interfacing hierarchy
5. Design for Nanometer

- Increasing systematic / parameter / random yield loss due to process variation
  - Physical patterning effects, open and short, etc.
  - Chemical and mechanical impact, planarity, antenna effect, and via opens, etc.
  - Timing, signal integrity and voltage drop

- Increasing leakage (quantity, source, variation)
Solution – Accurate DFM

- Model & simulation-based approach for physical and electrical DFM that represents Manufacturing accurately
  - Physical DFM
    - Identify hot spot, fix it and improve geometric yield.
  - Electrical DFM
    - Identify electrical performance deviation, correct it and improve paramedic yield

Set-up standard interface between phase and design which is design and layout phase
Solution – DFM Ecosystem

- Foundry to set up DFM ecosystem and open license DUF to reduce cost
- Standard interface between the design infrastructure and manufacturing

Example:

- EDA Alliance
- IP/Lib Alliance
- TSMC
- TSMC/GUC + DCA Alliance

TSMC DFM Compliance Initiative
Solution – Low Power

- Aggressively develop integrated low power solutions for dynamic and leakage power reduction
  - **Low power process**
    - Advanced processes with ELK/XLK dielectric: lower voltage, smaller geometry and capacitance for dynamic power reduction
    - HK/MG and gate CD bias for leakage reduction
  - **Low power IP**
    - Full set of low power foundation IP, dual power SRAM
  - **Low power design Reference Flow**
    - Silicon proven design methodologies for TSMC IP and processes
    - Voltage scaling (DVFS, AVS), power gating with data retention
    - Low power design automation enabling

Develop vertically integrated solution from system-level to layout and to process
6. Design Complexity

- Increased design complexity causes longer time-to-market and requires significant effort for verification and software design.

![Graph showing the evolution of design complexity from 1995 to 2020. The graph compares different device types: 2G, 3G, D1, HD, Full HD, 4G, Mobile Multimedia Device, Communication Device. It also shows the current design productivity and Moore's Law trend.]
Main Stream vs. ESL Co-development Environment

Electronic System Level (ESL)

- Architecture Exploration
- Software Profiling
- Hardware Profiling
- Power Estimation
Solution – ESL

- New ESL design technology to address design complexity, and to provide massively parallel heterogeneous MPSOC design
- SIP and 3D packaging can integrate large capacity memory and analog circuit with short time to market and low cost
- Develop product with chip and PC board at same time to improve success rate

Collaborate with EDA vendors
Summary

- Semiconductor market growth will continue but moderate
- Future growth opportunities will be global but bifurcate
- High ROI risks in design, fab, and technology could be alleviated with the integrated foundry model
- Close collaboration is required between EDA vendors, foundry and IC companies
Thank You

www.tsmc.com