Temperature-Aware Dynamic Frequency and Voltage Scaling for Reliability and Yield Enhancement

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Outline

- Introduction
- Global Architecture
- Thermal Sensor Design
- Experimental Results
- Conclusion

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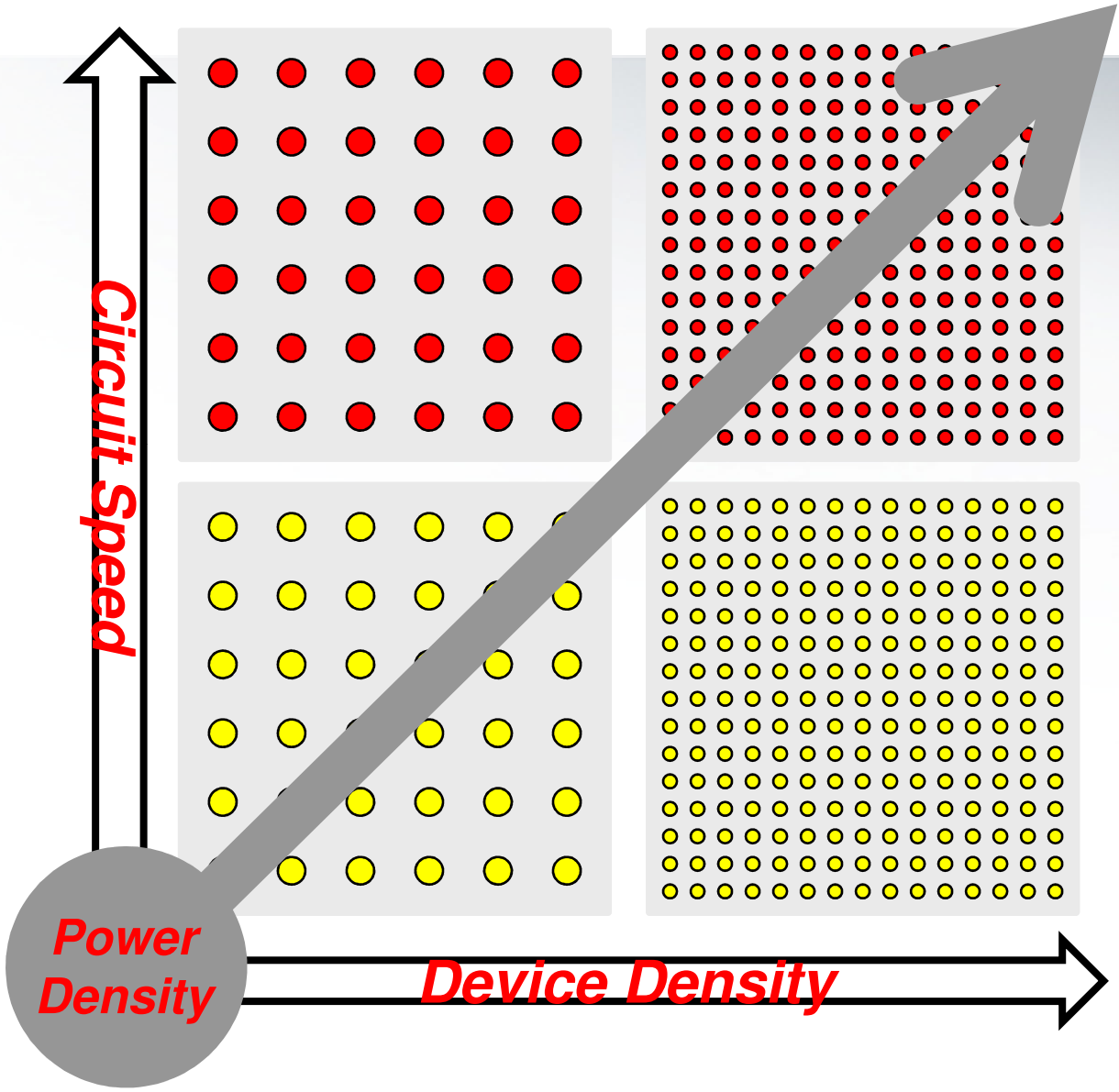
Technology Scaling Down



Introduction

$$P_{static} \downarrow = I_{leakage} \times V_{DD} \downarrow$$

$$P_{dynamic} \downarrow = C_L \times V_{DD}^{\,2} \downarrow \times f_p \downarrow$$

Introduction

- Propose a temperature-aware dynamic scaling framework in SoC
- Propose an on-chip thermal sensing mechanism

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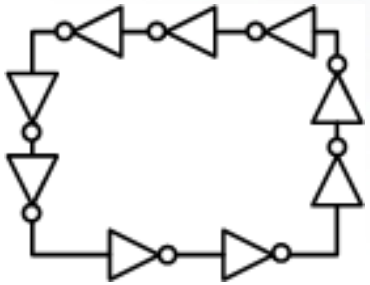
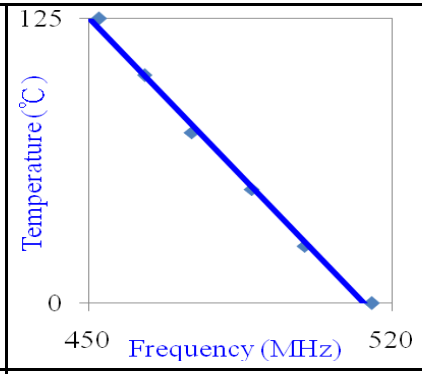
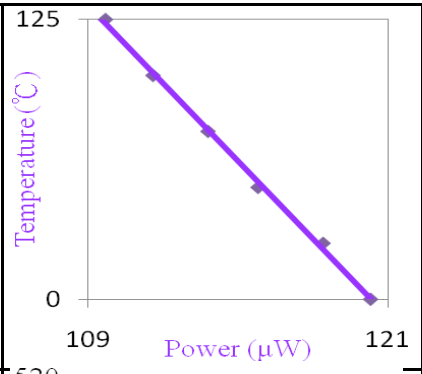
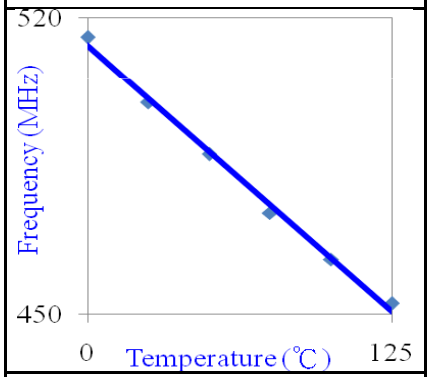
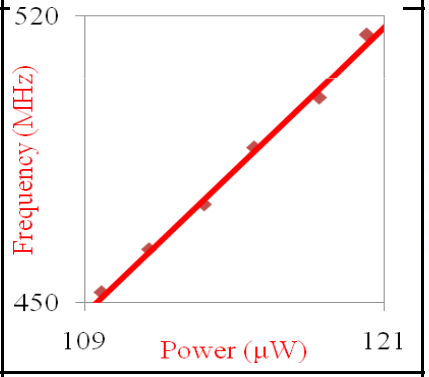
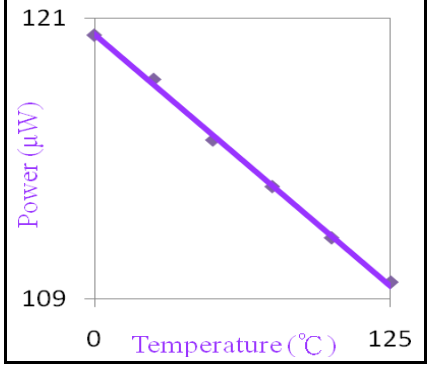
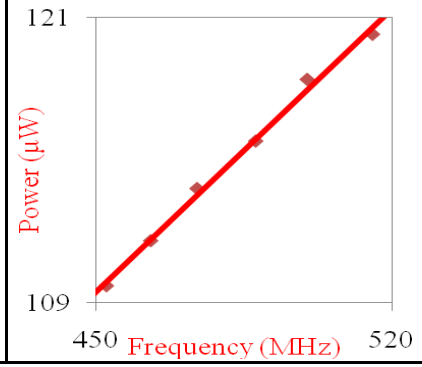
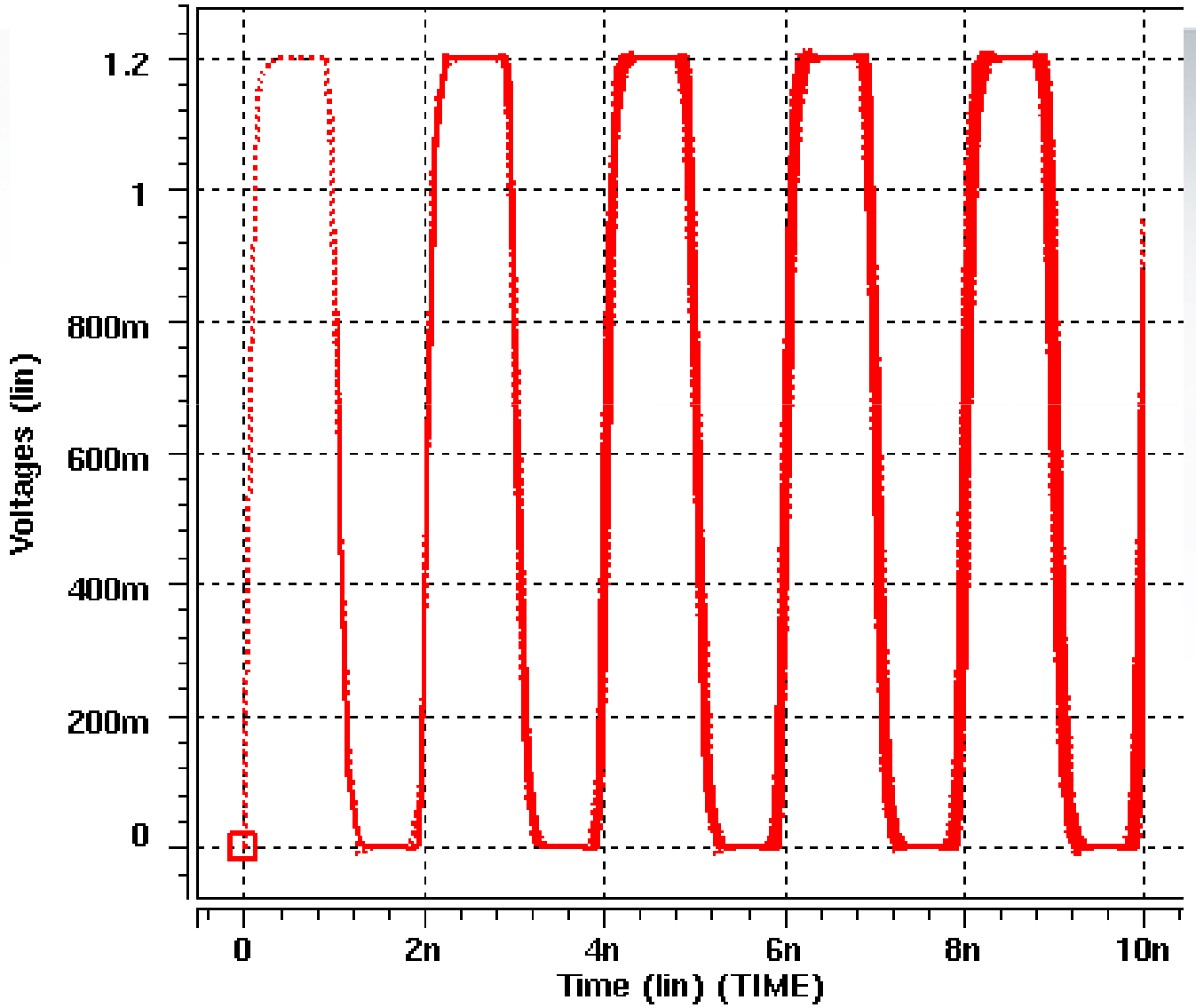
Linearity Among *Temperature*, *Frequency* and *Power*

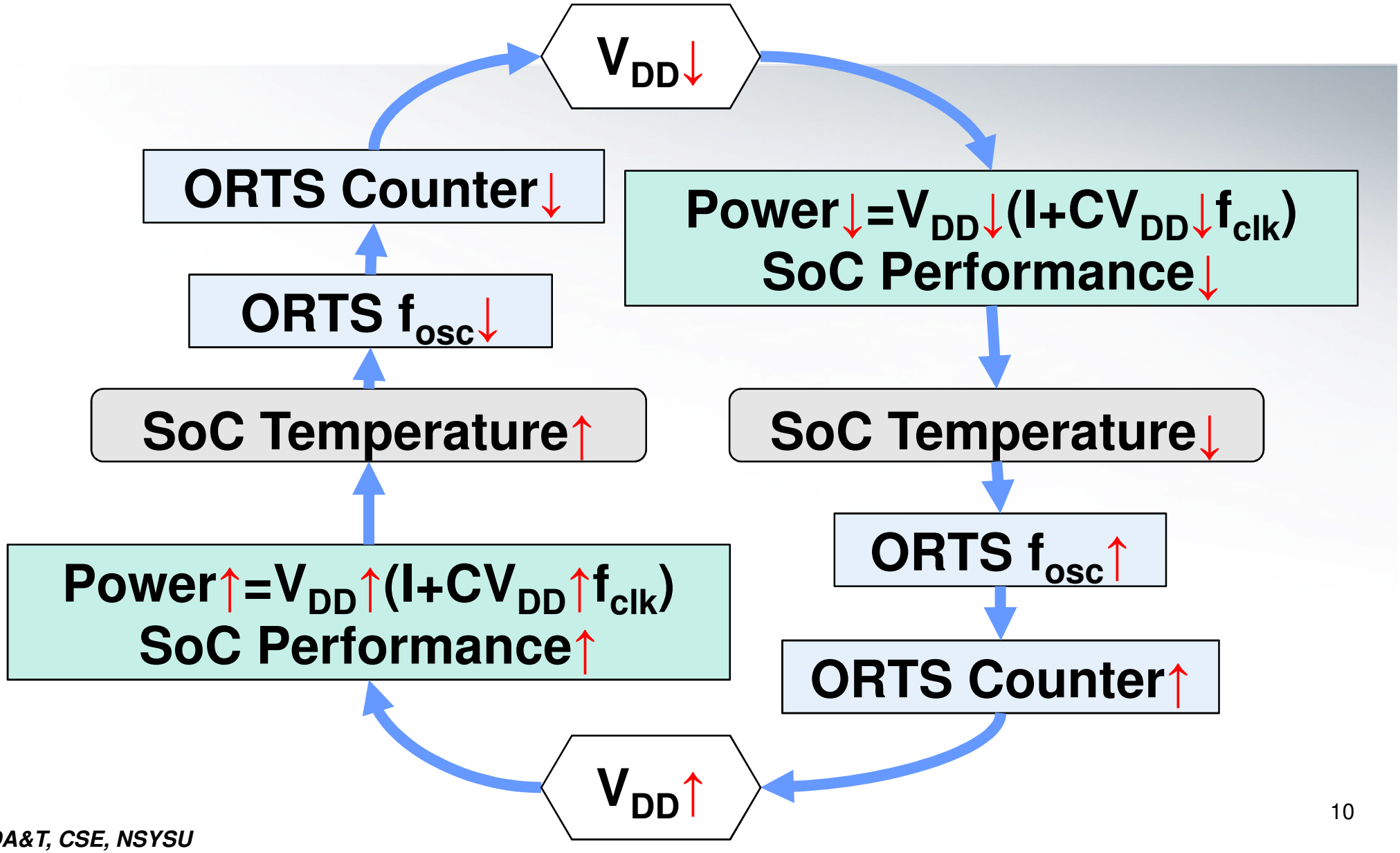


Temperature (℃)		
	**Frequency (MHz)**	
		**Power (μW)**

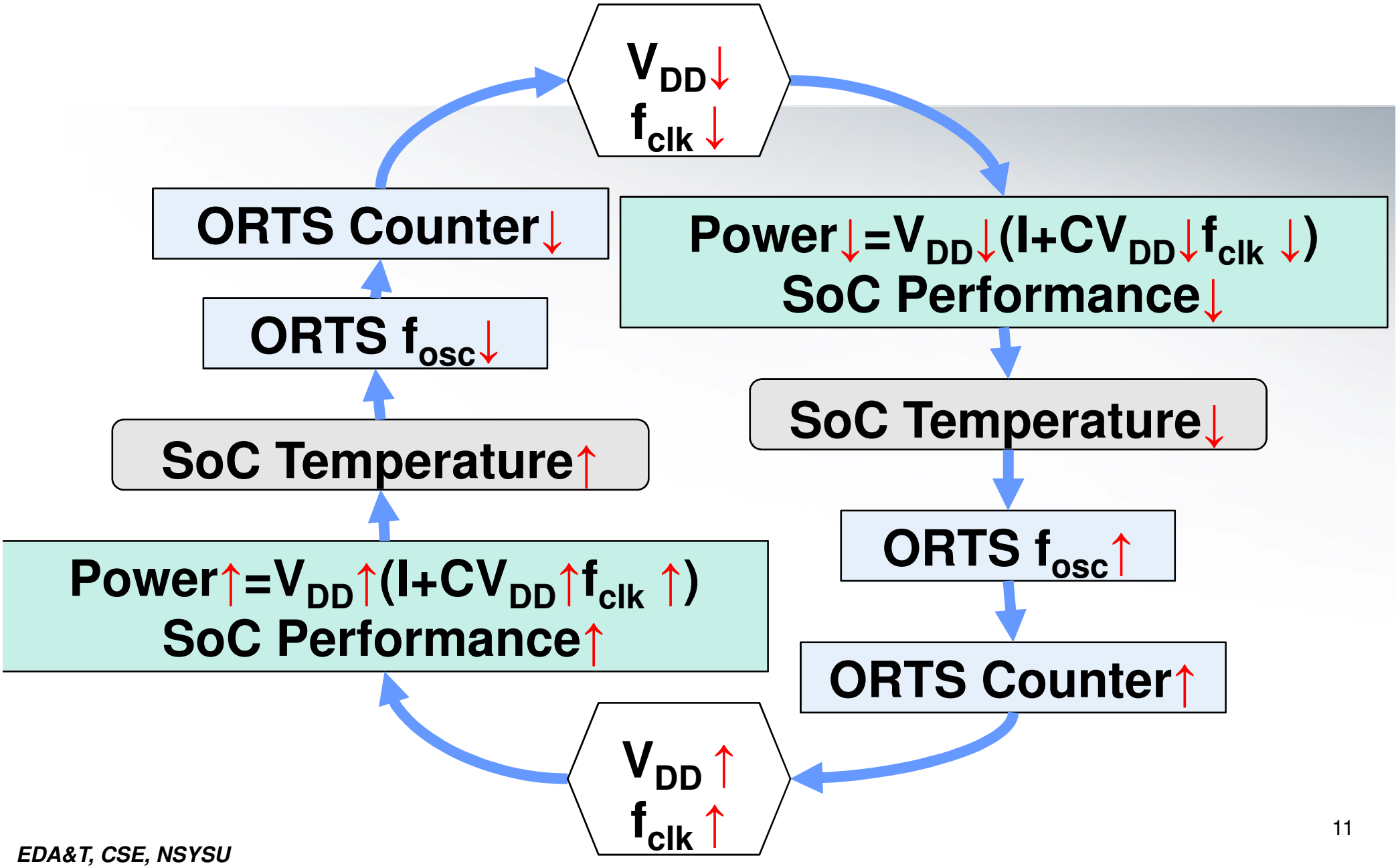
Feasibility of ORTS



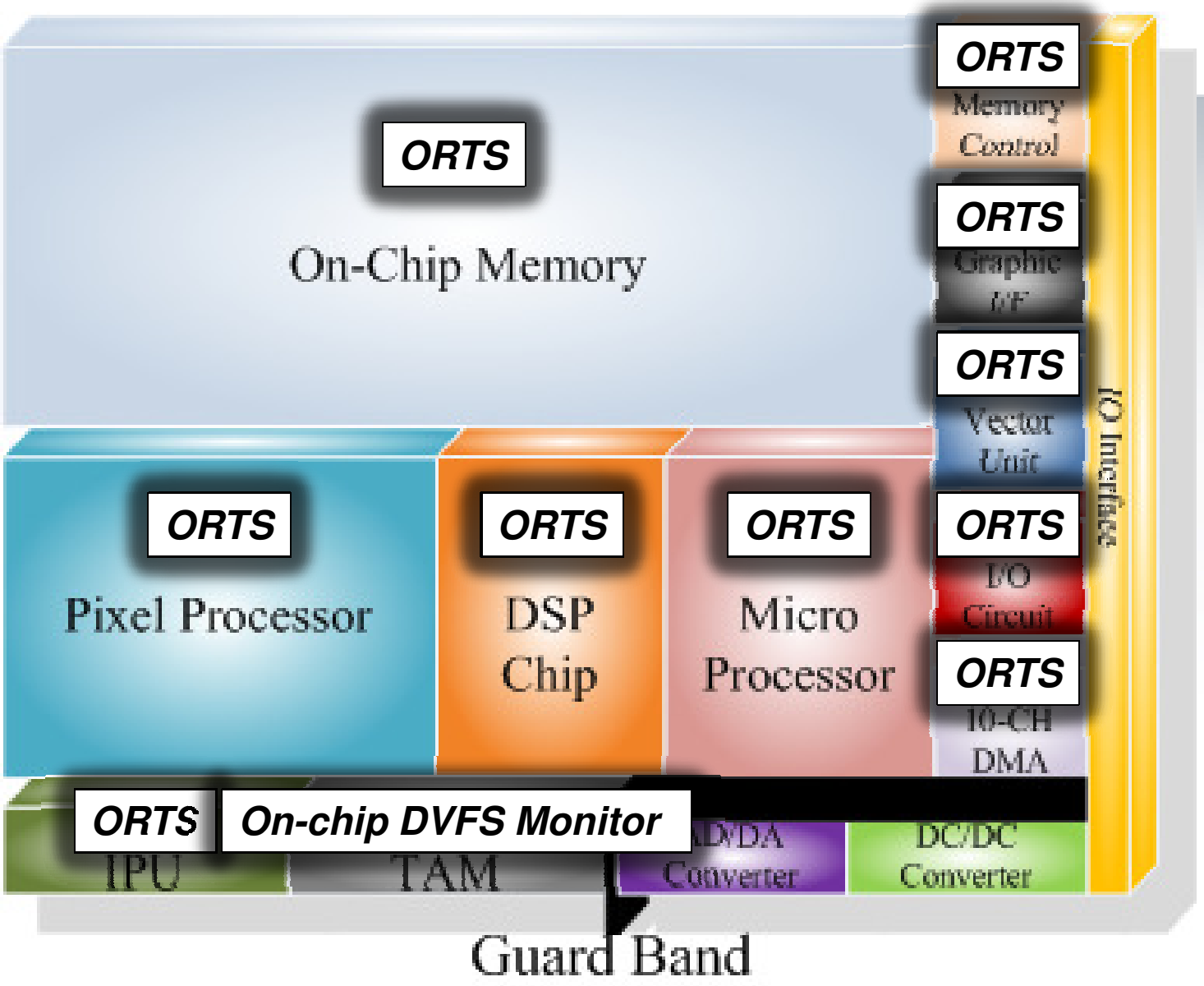
Dynamic Voltage Scaling



Dynamic Voltage & Frequency Scaling



System Architecture



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Basic Assumptions

(1) Three supply voltage levels are used:

$V_{DDL} < V_{DDS} < V_{DDH}$

(2) The corresponding clock frequencies:

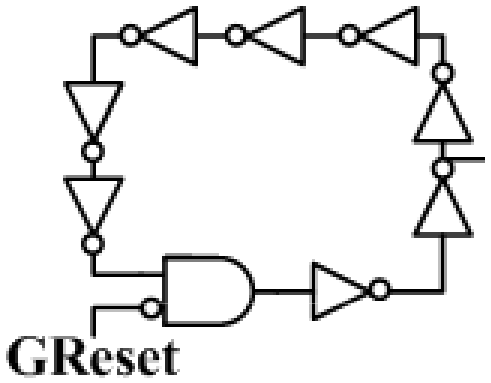
$f_{clkL} < f_{clkS} < f_{clkH}$

(3) Oscillation frequency: f_{osc}

(4) Two threshold frequencies: f_{oscL} and f_{oscH}

- $f_{osc} < f_{oscL}$
- $f_{oscL} < f_{osc} < f_{oscH}$
- $f_{oscH} < f_{osc}$

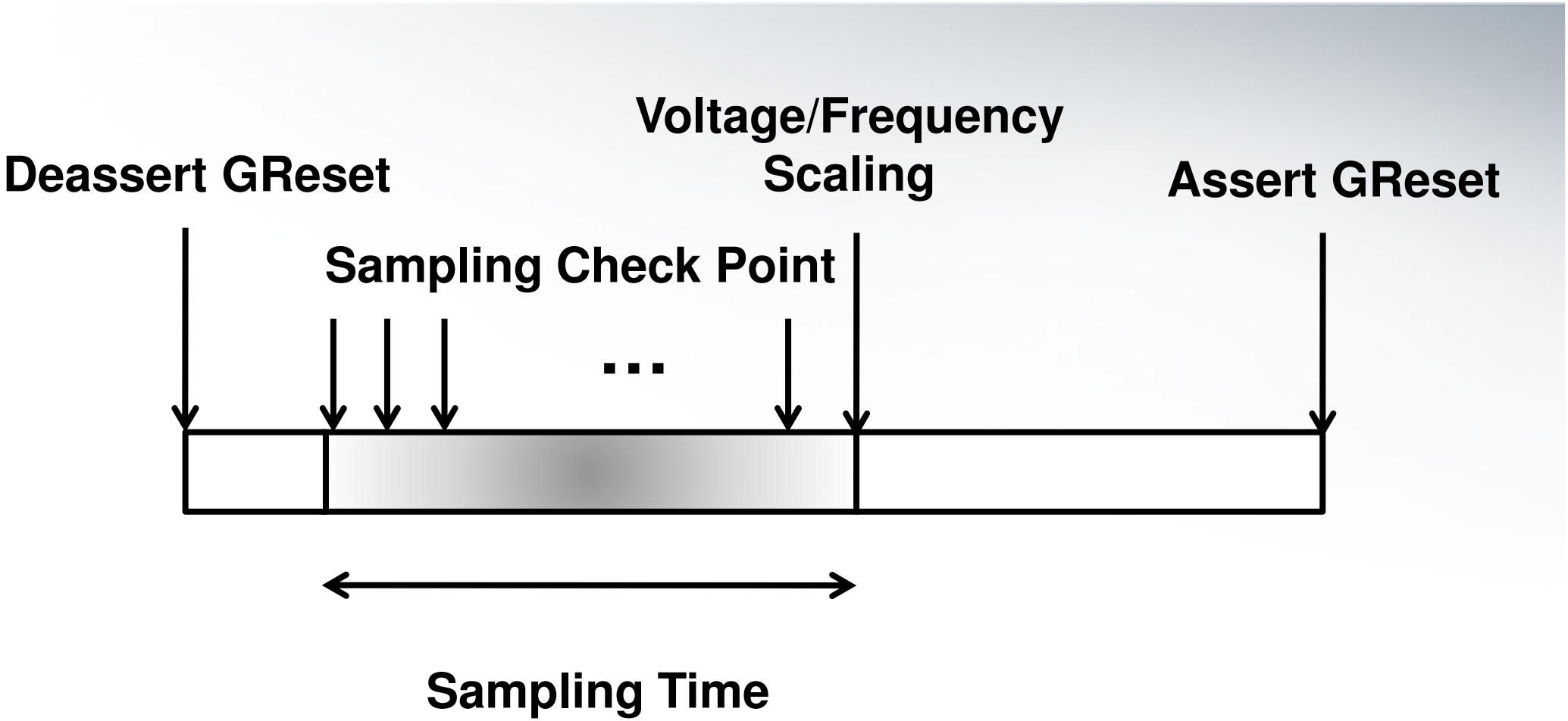
Oscillation-Ring Based Thermal Sensor



1 0 1 1

0	V_{DDL} f_{clkL}
0	V_{DDS} f_{clkS}
1	V_{DDH} f_{clkH}

DVS/DVFS Sampling Process



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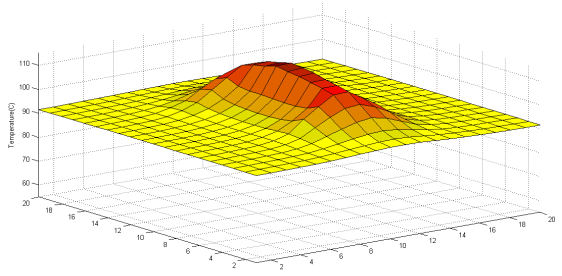
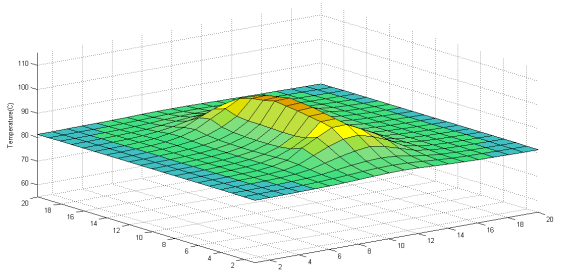
Thermal Profile of DVS Scheme

V_{DDH}



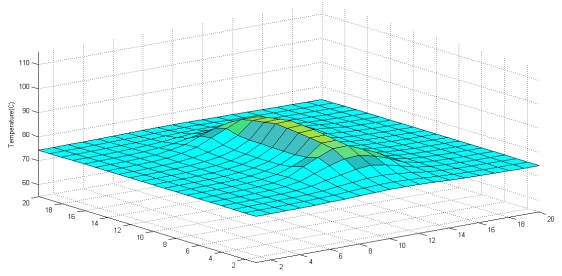
91.3°C ~ 112.7°C



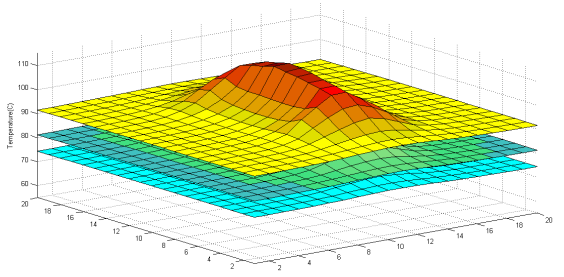
81°C ~ 98.1°C

V_{DDS}

V_{DDL}

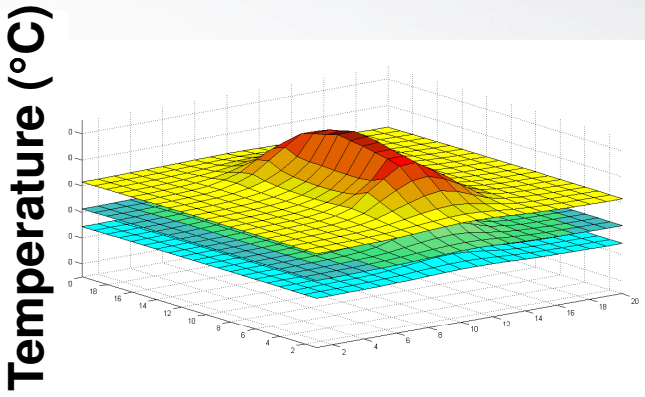


74.2°C ~ 88.4°C

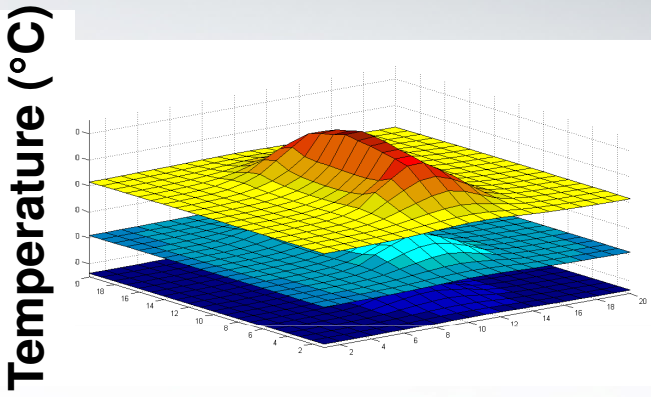


V_{DDH} / V_{DDS} / V_{DDL}

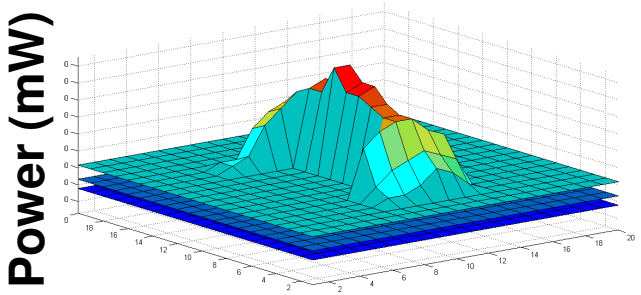
Temperature/Power Profile of DVS/DVFS Scheme



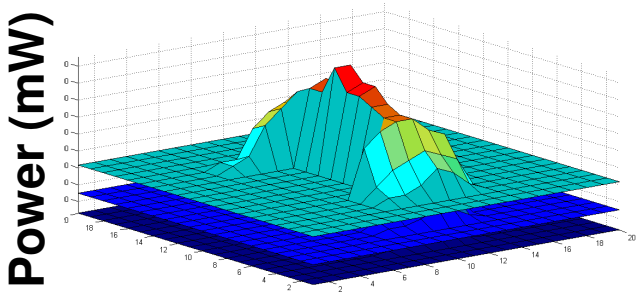
DVS



DVFS



DVS



DVFS

Experimental Results

- DVS Scheme

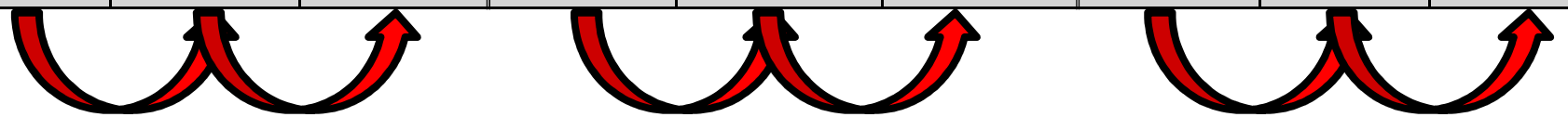
Circuit	Average Temperature (°C)			Average Core Power (mW)			Critical Delay (ns)		
	V_{DDH}	V_{DDS}	V_{DDL}	V_{DDH}	V_{DDS}	V_{DDL}	V_{DDH}	V_{DDS}	V_{DDL}
SoC1	100.49	88.34	80.33	417.12	333.14	277.71	2.20	2.99	5.04
SoC2	94.25	83.35	76.17	449.45	358.97	299.24	2.20	2.99	5.04
SoC3	56.78	53.44	51.13	11.05	8.82	7.30	9.26	9.86	11.17
SoC4	60.92	56.41	54.00	41.38	32.39	27.59	2.31	3.02	5.32
SoC5	95.43	83.81	76.32	102.13	80.66	66.82	1.67	2.40	3.98
Comp.	81.57	73.07	67.59	204.23	162.80	135.73	3.53	4.25	6.11
	1.21	1.08	1.00	1.50	1.20	1.00	1.00	1.21	1.73

12% 8% 25% 20% 21% 43%

Experimental Results

- DVFS Scheme

Circuit	Average Temperature (°C)			Average Core Power (mW)			Critical Delay (ns)		
	V_{DDH} f_{clkH}	V_{DDS} f_{clkS}	V_{DDL} f_{clkL}	V_{DDH} f_{clkH}	V_{DDS} f_{clkS}	V_{DDL} f_{clkL}	V_{DDH} f_{clkH}	V_{DDS} f_{clkS}	V_{DDL} f_{clkL}
SoC1	100.49	76.31	59.17	417.12	249.95	131.54	2.20	2.99	5.04
SoC2	94.25	72.56	57.21	449.45	269.32	141.73	2.20	2.99	5.04
SoC3	56.78	52.56	47.67	11.05	8.25	5.01	9.26	9.86	11.17
SoC4	60.92	53.51	46.85	41.38	26.61	13.36	2.31	3.02	5.32
SoC5	95.43	70.61	55.41	102.13	56.27	28.19	1.67	2.40	3.98
Comp.	81.57	65.11	53.26	204.23	122.08	63.97	3.53	4.25	6.11
	1.53	1.22	1.00	3.19	1.91	1.00	1.00	1.21	1.73



25% 22% 67% 91% 21% 43%

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Conclusion

- Propose a novel oscillation-ring based on-chip thermal sensing architecture for dynamically adjusting supply voltage and clock frequency in SoC
- Achieve averagely about 10% and 24% temperature reduction in DVS and DVFS scheme
- Achieve averagely about 23% and 79% power reduction in DVS and DVFS scheme


Thank You for Your Participation!
EDA&Testing Laboratory
Dept. of Computer Science and Engineering
National Sun Yat-sen University